National Semiconductor

74BCT373
Octal Transparent Latch with TRI-STATE® Outputs

General Description

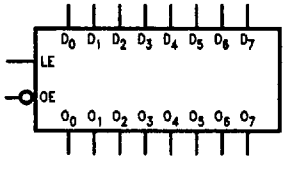
The 'BCT373 consists of eight latches with TRI-STATE outputs for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

Features

- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})
- Guaranteed 4000V minimum ESD protection
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed latchup protection
- Low I_{CCZ} through BiCMOS techniques

Ordering Code: See Section 11

Logic Symbols



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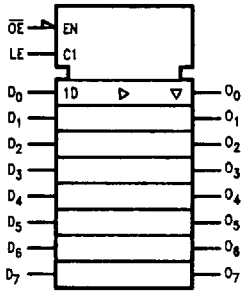
IEEE/IEC



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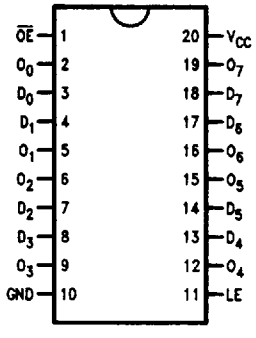
Connection Diagram

Pin Assignment for DIP and SOIC



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Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Latch Outputs

Functional Description

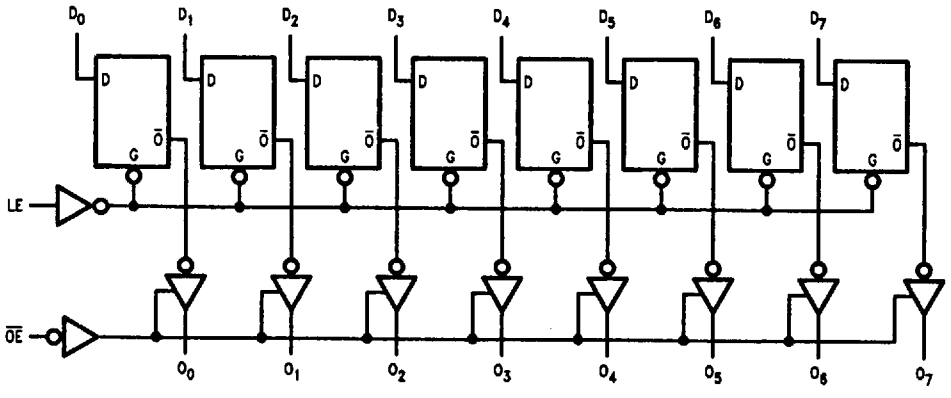
The 'BCT373 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Output
LE	$\overline{OE}$	D_n	O_n
H	L	H	H
H	L	L	L
L	L	X	O_n (no change)
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance State

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} + 4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current			8	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			30	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			10	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.0 2.0		9.3 11.6	2.0 1.5	9.3 11.6	ns	8-3
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	2.0 2.0		10.3 9.3	2.0 2.0	10.3 9.3	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0		11.8 11.8	2.0 2.0	11.8 11.8	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0		6.9 6.1	2.0 2.0	6.9 6.1	ns	8-5

AC Electrical Characteristics: See Section 8 for Waveforms

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$		74BCT $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to LE	5.9 5.9		5.9 5.9		ns	8-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to LE	1.5 1.5		1.5 1.5			
$t_w(H)$	LE Pulse Width, HIGH	3.0		3.0		ns	8-4

Extended AC Electrical Characteristics: See Section 8

Symbol	Parameter	74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 50$ pF 8 Outputs Switching (Note 3)		74BCT $T_A = Com$ $V_{CC} = Com$ $C_L = 250$ pF (Note 4)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.0 2.0	10.5 13.0	2.0 2.0	11.8 14.0	ns	8-3

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	5	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	8	pF	$V_{CC} = 5.0V$