# Samurai

6 Port 10/100 Mbit/s Single Chip Ethernet Switch Controller (ADM6996LCX - Green Package Version; ADM6996LHX - Heat Sink and Green Package)
Version AC

Communications

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**Samurai 6 Port 10/100 Mbit/s Single Chip Ethernet Switch Controller (ADM6996LCX - Green Package Version)**

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| Page19 | Modify LNKFP5 pin description |
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# 1 Product Overview

## 1.1 Overview

The Samurai (ADM6996LC/LCX/LHX) is a high performance, low cost, highly integrated (Controller, PHY and Memory) five-port 10/100 Mbit/s TX/FX plus one 10/100 MAC port Ethernet switch controller with all ports supporting 10/100 Mb/s Full/Half duplex. The ADM6996LC/LCX/LHX is intended for applications for stand alone bridges for low cost SOHO markets such as Wire/ADSL/Wireless Router, IP Set Top Box, VDSL2, Gateway and HomePNA/HomePlug applications. The ADM6996LCX is the environmentally friendly "green" package version. The LH solution contains a heat sink which can be used in special circumstances but is not recommended for all projects.

ADM6996LC/LCX/LHX provides advanced functions such as:**802.1p(Q.O.S.), Port-based/Tag-based VLAN, Port MAC address Locking, Management, Port Status, MAC Address Access and Bandwidth Control**.

The ADM6996LC/LCX/LHX also supports Back Pressure in Half-Duplex mode and 802.3x Flow Control Pause packet in Full-Duplex mode to prevent packet loss when buffer is full. When Back Pressure is enabled, and there is no receive buffer available for the incoming packet, the ADM6996LC/LCX/LHX will issue a JAM pattern on the receiving port in Half Duplex mode and transmit the 802.3x Pause packet back to receiving end in Full Duplex mode.

The built-in SRAM used for packet buffering is divided into 256 bytes/block to achieve the optimized memory utilization through complicated link lists on packets with various lengths.

ADM6996LC/LCX/LHX also supports priority features by Port-Base, VLAN, IP TOS, TCP/UDP Layer4 destination port number, MAC destination address field checking. Users can be easily set different priority modes in individual ports, through a small low-cost micro controller to initialize or on-the-fly to configure. Each output port supports four queues in the way of fixed N:1 or programmable fairness queuing to fit the bandwidth demand on various types of packets such as Voice, Video and Data. Tag/Untag, and up to 16 groups of VLAN also is supported.

An intelligent address recognition algorithm makes ADM6996LC/LCX/LHX to recognize up to 2K different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by ADM6996LC/LCX/LHX to use on Building Internet access to prevent multiple users sharing one port traffic.

## 1.2 Features

- Supports five 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces and one MII/GPSI port.
- Supports 2K MAC addresses table with 4-ways associative hash algorithm.
- Supports four queue for QoS
- Supports priority features by Port-Based, 802.1p, IP TOS of packets, Layer4 TCP/UDP destination port number and MAC address DA.
- Supports MAC dress accessible such as Search, Add and Delete.
- Supports Engress/Ingress 64K Scalable Bandwidth control.
- Supports Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed.
- Supports buffer allocation with 256 bytes per block
- Supports Aging function Enable/Disable.
- Supports per port Single/Dual color mode with Power On auto diagnostic.
- Supports 802.3x Flow Control pause packet for Full Duplex in case buffer is full.
- Supports Back Pressure function for Half Duplex operation in case buffer is full.
- Supports packet length up to 1518/1522 (Default)/1536/1784 bytes in maximum.
- Broadcast/Multicast Storm Suppression.

- Supports Tag-based VLAN. Up to 16 VLAN groups is implemented by the last four bits of VLAN ID.
- 2bit MAC clone to support multiple WAN application
- Supports TP interface Auto MDIX function for auto TX/RX swap by strapping-pin.
- Easy Management 32bits smart counter for per port RX/TX byte/packet count, 16-bit smart counter for per port ERROR count and Collision count through serial 32/16 bits mode access. 16 bits mode is MDC/MDIO timing compatible.
- Supports PHY status output for management system.
- 25M Crystal only for the whole system.
- 128 QFP package with 0.18um technology. 1.8 V/3.3 V power supply.
- 1.0 W low power consumption.

## 1.3 Applications

ADM6996LC/LCX/LHX in 128-pin PQFP:

- Wire/ADSL/Wireless/VDSL2 Router
- IP Setop Box, HomePNA, HomePlug application.

## 1.4 Block Diagram

Figure 1 below shows a simple block diagram of the ADM6996LC/LCX/LHX internal blocks.
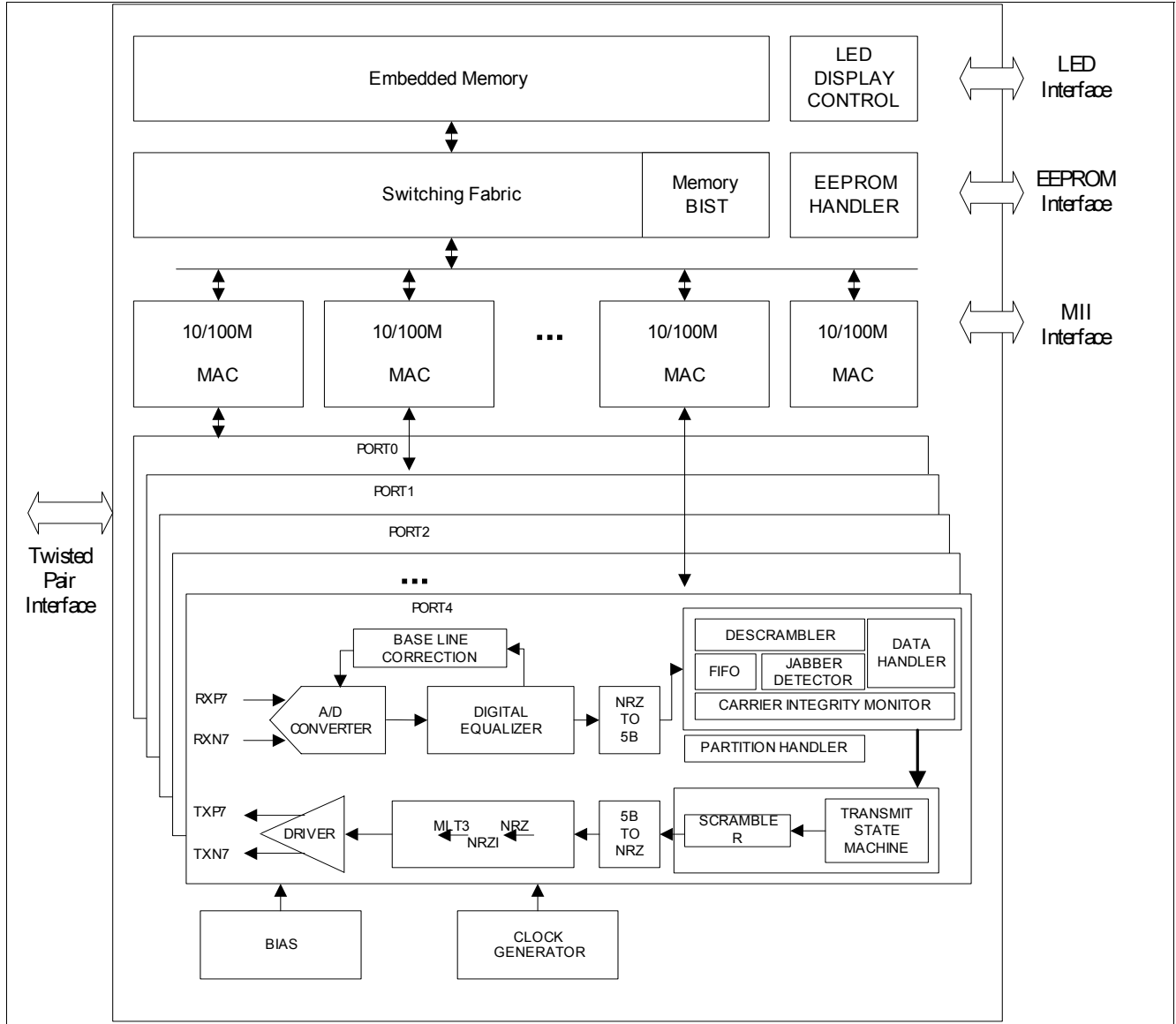


**Figure 1    ADM6996LC/LCX/LHX Block Diagram**

# 2 Interface Description

This chapter describes the interface descriptions for the ADM6996LC/LCX/LHX

- Pin Diagram
- Abbreviations
- Pin Description by Function

## 2.1 Pin Diagram

**Figure 2** shows the pin diagram for the ADM6996LC/LCX/LHX.
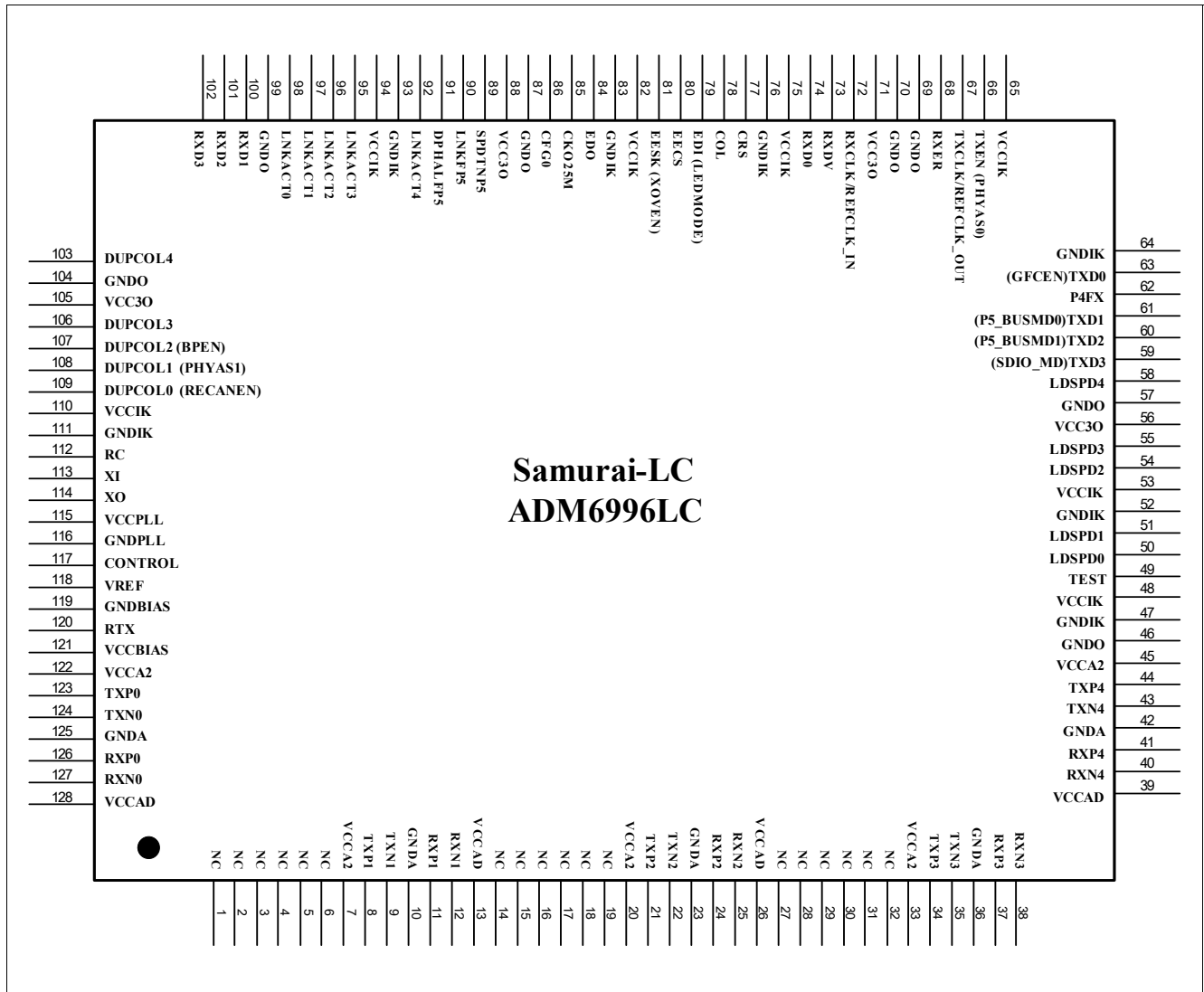


**Figure 2    5 TP/FX PORT + 1 MII PORT 128 Pin Diagram**

## 2.2 Abbreviations

Standard abbreviations for I/O tables:

**Table 1    Abbreviations for Pin Type**

| Abbreviations | Description |
|---|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| AO | Output. Analog levels. |
| AI/O | Input or Output. Analog levels. |
| PWR | Power |
| GND | Ground |
| MCL | Must be connected to Low (JEDEC Standard) |
| MCH | Must be connected to High (JEDEC Standard) |
| NU | Not Usable (JEDEC Standard) |
| NC | Not Connected (JEDEC Standard) |

**Table 2    Abbreviations for Buffer Type**

| Abbreviations | Description |
|---|---|
| Z | High impedance |
| PU | Pull up, 10 k$\Omega$ |
| PD | Pull down, 10 k$\Omega$ |
| TS | Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance. |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource. |
| OC | Open Collector |
| PP | Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute). |
| OD/PP | Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute. |
| ST | Schmitt-Trigger characteristics |
| TTL | TTL characteristics |

## 2.3 Pin Description by Function

ADM6996LC/LCX/LHX pins are categorized into one of the following groups:

- Network Media Connection
- Port 5 MII Interface
- LED Interface
- EEPROM Interface
- Power/Ground, 48 pins
- Miscellaneous

*Note: Table 1 can be used for reference.*

**Table 3    IO Signals**

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| **Network Media Connection** | | | | |
| 41 | RXP_4 | AI/O | ANA | **Receive Pair** Differential data is received on this pin. |
| 37 | RXP_3 | | | |
| 24 | RXP_2 | | | |
| 11 | RXP_1 | | | |
| 126 | RXP_0 | | | |
| 40 | RXN_4 | AI/O | ANA | |
| 38 | RXN_3 | | | |
| 25 | RXN_2 | | | |
| 12 | RXN_1 | | | |
| 127 | RXN_0 | | | |
| 44 | TXP_4 | AI/O | ANA | **Transmit Pair** Differential data is transmitted on this pin. |
| 34 | TXP_3 | | | |
| 21 | TXP_2 | | | |
| 8 | TXP_1 | | | |
| 123 | TXP_0 | | | |
| 43 | TXN_4 | AI/O | ANA | |
| 35 | TXN_3 | | | |
| 22 | TXN_2 | | | |
| 9 | TXN_1 | | | |
| 124 | TXN_0 | | | |
| **Port 5 MII Interface** | | | | |
| 63 | GFCEN | I | PU, LVTTL | **Global Flow Control Enable** Value on this pin will be latched by ADM6996LC/LCX/LHX at the rising edge of RESETL(**RC**) as Flow control enable. *Note: Power On Setting* $0_B$     Flow Control Capability is depended upon the register setting in corresponding EEPROM register $1_B$     All ports flow control capability is enabled |
| | MII_TXD0 | O | 4 mA, PU, LVTTL | **Port 5 Transmit Data Bit 0 in MII Mode** The bit[0] of MII Transmit data of port 5. Synchronous to the rising edge of MII_TXCLK. |
| | GPSI_TXD | O | 4 mA, PU, LVTTL | **Port 5 Transmit Data in GPSI Mode** When port 5 is operating in GPSI mode, this pin acts as GPSI Transmit Data. Synchronous to the rising edge of GPSI_TXCLK. |
| | RMII_TXD0 | O | 4 mA, PU, LVTTL | **Port 5 Transmit Data Bit 0 in RMII Mode** When port 5 is operating in RMII mode, this pin acts as RMII Transmit Data Bit [0]. Synchronous to the rising edge of REFCLK_IN. |

**Table 3    IO Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 61 | P5_BUSMD0 | I | PD, LVTTL | **Port 5 Bus Mode Selection Bit 0**<br>Value on this pin will be latched by ADM6996LC/LCX/LHX at the rising edge of RESETL as port 5 bus mode selection bit 0. Combined with **P5_BUSMD1**, ADM6996LC/LCX/LHX provides 3 bus type for port 5.<br>P5_BUSMD[1:0], Interface<br>*Note: Power On Setting*<br><br>$00_B$    MII<br>$01_B$    GPSI<br>$10_B$    RMII<br>$11_B$    Reserved and not allowed |
| | MII_TXD1 | O | 4 mA, PD, LVTTL | **Port 5 Transmit Data Bit 1 in MII Mode**<br>The bit[1] of MII Transmit data of port 5. Synchronous to the rising edge of MII_TXCLK. |
| | RMII_TXD1 | O | 4 mA, PD, LVTTL | **Port 5 Transmit Data Bit 1 in RMII Mode**<br>The bit[1] of RMII Transmit data of port 5. Synchronous to the rising edge of REFCLK_IN. |
| 60 | P5_BUSMD1 | I | PD, LVTTL | **Port 5 Bus Mode Selection Bit 1**<br>Value on this pin will be latched by ADM6996LC/LCX/LHX at the rising edge of RESETL as port 5 bus mode selection bit 1. Combined with **P5_BUSMD0**, ADM6996LC/LCX/LHX provides 3 bus type for port 5.<br>*Note: Power On Setting* |
| | MII_TXD2 | O | 4 mA, PD, LVTTL | **Port 5 Transmit Data Bit 2 in MII Mode**<br>The bit[2] of MII Transmit data of port 5. Synchronous to the rising edge of MII_TXCLK. |
| 59 | SDIO_MD | I | PD, LVTTL | **SDC/SDIO Mode Selection**<br>Value on this pin will be latched by ADM6996LC/LCX/LHX at the rising edge of RESETL for SDIO 32/16 bits selection.<br>$0_B$     32 Bits Mode<br>$1_B$     16 Bits Mode. Same timing as MDC/MDIO. |
| | MII_TXD3 | O | 4 mA, PD, LVTTL | **Port 5 Transmit Data Bit 3 in MII Mode**<br>The bit[3] of MII Transmit data of port 5. Synchronous to the rising edge of MII_TXCLK. |

**Table 3** **IO Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 66 | PHYAS0 | I | PD, LVTTL | **PHY Address MSB Bit 0**<br>During power on reset, value will be latched by ADM6996LC/LCX/LHX at the rising edge of RESETL as PHY start address select.<br>PHYAS[1:0] = $00_B$ and PHY address starts from $01000_B$.<br>*Note: Power On Setting* |
| | MII_TXEN | O | 8 mA, PD, LVTTL | **Port 5 Transmit Enable TXEN in MII Mode**<br>Active high to indicate that the data on MII_TXD[3:0] is valid. Synchronous to the rising edge of MII_TXCLK. |
| | GPSI_TXEN | O | 8 mA, PD, LVTTL | **Port 5 Transmit Enable TXEN in GPSI Mode**<br>Active high to indicate that the data on GPSI_TXD is valid. Synchronous to the rising edge of GPSI_TXCLK. |
| | RMII_TXEN | O | 8 mA, PD, LVTTL | **Port 5 R Transmit Enable TXEN in RMII Mode**<br>Active high to indicate that the data on RMII_TXD[1:0] is valid. Synchronous to the rising edge of REFCLK_IN. |
| 74 | MII_RXD0 | I | PD, LVTTL | **Port 5 Receive Data Bit 0 in MII Mode**<br>The bit[0] of MII receive data, synchronous to the rising edge of MII_RXCLK. |
| | GPSI_RXD | I | PD, LVTTL | **Port 5 Receive Data in GPSI Mode**<br>In GPSI Mode, this acts as Receive Data Input, synchronous to the rising edge of GPSI_RXCLK. |
| | RMII_RXD0 | I | PD, LVTTL | **Port 5 Receive Data Bit 0 in RMII Mode**<br>The bit[0] of RMII receive data, synchronous to the rising edge of REFCLK_IN. |
| 100 | MII_RXD1 | I | PD, LVTTL | **Port 5 Receive Data Bit 1in MII Mode**<br>The bit[1] of MII receive data, synchronous to the rising edge of MII_RXCLK. |
| | RMII_RXD1 | I | PD, LVTTL | **Port 5 Receive Data Bit 1in RMII Mode**<br>Bit[1] of RMII receive data, synchronous to the rising edge of REFCLK_IN. |
| 101 | MII_RXD2 | I | PD, LVTTL | **Port 5 Receive Data Bit 2 in MII Mode**<br>The bit[2] of MII receive data. Synchronous to the rising edge of MII_RXCLK. |
| 102 | MII_RXD3 | I | PD, LVTTL | **Port 5 Receive Data Bit 3 in MII Mode**<br>The bit[3] of MII receive data. Synchronous to the rising edge of MII_RXCLK. |
| 73 | MII_RXDV | I | PD, LVTTL | **Port 5 Receive Data Valid in MII Mode**<br>Active high to indicate that the data on MII_RXD[3:0] is valid. Synchronous to the rising edge of MII_RXCLK. |
| | RMII_CRSDV | I | PD, LVTTL | **Port 5 Carrier Sense and Receive Data Valid in RMII Mode**<br>Active high to indicate that the data on RMII_RXD[1:0] is valid. Synchronous to the rising edge of REFCLK _IN. |

**Table 3    IO Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 68 | MII_RXER | I | PD, LVTTL | **Port 5 Receive Error in MII Mode**<br>Active high to indicate that there is error on the MII_RXD [3:0]. Upon receiving this signal, ADM6996LC/LCX/LHX will send Error Symbol onto the medium. Only valid in 100M operation. |
|  | RMII_RXER | I | PD, LVTTL | **Port 5 Receive Error in RMII Mode**<br>Active high to indicate that there is error on the RMII_ RXD[1:0]. Upon receiving this signal, ADM6996LC/LCX/LHX will send Error Symbol onto the medium. Only valid in 100M operation. |
| 77 | MII_CRS | I | PD, LVTTL | **Port 5 Carrier Sense in MII Mode**<br>In full duplex mode, MII_P5CRS reflects the receive carrier sense situation on medium only; In Half Duplex, MII_CRS will be high both in receive and transmit condition. |
|  | GPSI_CRS | I | PD, LVTTL | **Port 5 Carrier Sense in GPSI Mode**<br>In full duplex mode, GPSI_CRS reflects the receive carrier sense situation on medium only; In Half Duplex, GPSI_CRS will be high both in receive and transmit condition. |
| 78 | MII_COL | I | PD, LVTTL | **Port 5 Collision Input in MII Mode**<br>Active high to indicate that there is collision on the medium. Stay low in full duplex operation. |
|  | GPSI_COL | I | PD, LVTTL | **Port 5 Collision Input in GPSI Mode**<br>Active high to indicate that there is collision on the medium. Stay low in full duplex operation. |
| 72 | MII_RXCLK | I | PD, LVTTL | **Port 5 Receive Clock Inputin MII Mode**<br>MII_RXDV and MII_RXD[3:0] are synchronous to the rising edge of this clock. It is free running 25 MHz clock in 100M mode and 2.5 MHz clock in 10M mode. |
|  | GPSI_ RXCLK | I | PD, LVTTL | **Port 5 Receive Clock Input in GPSI Mode**<br>GPSI_RXD are synchronous to the rising edge of this clock. It is non-continuous 10 MHz Clock input. |
|  | REFCLK_IN | I | PD, LVTTL | **50MHz Reference Clock Input in RMII mode**<br>RMII_RXD[1:0], RMII_TXD[1:0], RMII_TXEN and RMII_CRSDV are synchronous to the rising edge of this clock. |
| 67 | MII_TXCLK | I | PD, LVTTL | **Port 5 Transmit Clock Input in MII Mode**<br>MII_TXEN and MII_TXD[3:0] are output at the rising edge of this clock. It is free running 25 MHz clock in 100M mode and 2.5 MHz clock in 10M mode. |
|  | GPSI_TXCLK | I | PD, LVTTL | **Port 5 Transmit Clock Input in GPSI Mode**<br>GPSI_TXEN and GPSI_TXD are synchronous to the rising edge of this clock. It is continuous 10 MHz Clock input. |
|  | REFCLK _ OUT | O | 8 mA, PD, LVTTL | **50MHz Reference Clock Output in RMII mode**<br>This pin is used as 50 MHz reference clock signal output pin when port 5 operates in RMII mode. |

**Table 3     IO Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 89 | SPDTNP5 | I | PD, LVTTL | **Port 5 Speed Input**<br>$0_B$     100M<br>$1_B$     10M |
| 90 | LNKFP5 | I | PD, LVTTL | **Port 5 Link Fail Status Input**<br>$0_B$     Link Up<br>$1_B$     Link Failed |
| 91 | DPHALFP5 | I | PD, LVTTL | **Port 5 Duplex Status Input**<br>$0_B$     Full Duplex<br>$1_B$     Half Duplex |
| **LED Interface** | | | | |
| 103 | DUPCOL4 | O | 8 mA, PD, LVTTL | **Port 4 Duplex /Collision LED**<br>In Full duplex mode, this pin acts as DUPLEX LED for port 4, respectively; in half duplex mode, it is collision LED for each port. See **Chapter 3.23 LED Display** for more detail. |
| 106 | DUPCOL3 | O | 8 mA, PD, LVTTL | **Port 3 Duplex /Collision LED**<br>In Full duplex mode, this pin acts as DUPLEX LED for port 3, respectively; in half duplex mode, it is collision LED for each port. See **Chapter 3.23 LED Display** for more detail. |
| 107 | BPEN | I | PU, LVTTL | **Recommend Back-Pressure in Half-Duplex**<br>The value on this pin will be latched by ADM6996LC/LCX/LHX during power on reset as the beck-pressure enable in half-duplex mode.<br>*Note: Power On Setting*<br>$0_B$     Disable Back-Pressure<br>$1_B$     Enable Back-Pressure |
|  | DUPCOL2 | O | 8 mA, PU, LVTTL | **Port 2 Duplex-collision LED**<br>In Full duplex mode, this pin acts as port 2 DUPLEX LED; in half duplex mode, it is collision LED for port 2. See **Chapter 3.23 LED Display** for more detail. |
| 108 | PHYAS1 | I | PD, LVTTL | **Recommend PHY Address Bit 1**<br>Value on this pin will be latched by ADM6996LC/LCX/LHX during power on reset as the PHY address recommend value bit 1. See **PHYAS0** description for more detail.<br>*Note: Power On Setting* |
|  | DUPCOL1 | O | 8 mA, PD, LVTTL | **Port 1 Duplex-collision LED**<br>In Full duplex mode, this pin acts as port 1 DUPLEX LED; in half duplex mode, it is collision LED for port 1. See **Chapter 3.23 LED Display** for more detail. |

**Table 3    IO Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 109 | RECANEN | I | PU, LVTTL | **Recommend Auto Negotiation Enable**<br>Only valid for Twisted pair interface. Programming this bit to 1 has no effect on the Fiber port.<br>*Note: Power On Setting.*<br><br>$0_B$    Disable all TP port auto negotiation capability<br>$1_B$    Enable all TP port auto negotiation capability |
|  | DUPCOL0 | O | 8 mA, PU, LVTTL | **Port 0 Duplex-collision LED**<br>In Full duplex mode, this pin acts as port 0 DUPLEX LED; in half duplex mode, it is the collision LED for port 0. See **Chapter 3.23 LED Display** for more detail. |
| 92<br>95<br>96<br>97<br>98 | LNKACT_4<br>LNKACT_3<br>LNKACT_2<br>LNKACT_1<br>LNKACT_0 | O | 8 mA, PD, LVTTL | **LINK/Activity LED of Port 4 to 0**<br>Used to indicate corresponding port' s link/activity status, see **Chapter 3.23 LED Display** for more detail. |
| 58<br>55<br>54<br>51<br>50 | LDSPD_4<br>LDSPD_3<br>LDSPD_2<br>LDSPD_1<br>LDSPD_0 | O | 8 mA, PD, LVTTL | **Port 4 to Port 0 Speed LED**<br>Used to indicate corresponding port' s speed status, see **Chapter 3.23 LED Display** for more detail. |
| **EEPROM Interface** | | | | |
| 84 | EDO | I | PU, LVTTL | **EEPROM Data Output**<br>This pin is used to input EEPROM data when reading EEPROM. During ADM6996LC/LCX/LHX initialization, ADM6996LC/LCX/LHX will drive EEPROM interface signal to read settings from EEPROM. Any other devices attach to EEPROM interface SHOULD drive Hi-Z or keep tristate during this period. See **Chapter 4.6 EEPROM Access** for more detail. |
| 80 | IFSEL | I | PD, LVTTL | **Interface Selection**<br>After ADM6996LC/LCX/LHX initialization, this pin is used to select using EEPROM interface or SDC/SDIO interface. EECS/IFSEL interface<br>$0_B$    SDC/SDIO interface<br>$1_B$    EEPROM interface |
|  | EECS | O | 4 mA, PD, LVTTL | **EEPROM Chip Select**<br>During ADM6996LC/LCX/LHX initialization, this pin is used as the EEPROM chip select signal.<br>During ADM6996LC/LCX/LHX initialization, ADM6996LC/LCX/LHX will drive EEPROM interface signal to read settings from the EEPROM. Any other devices attached to the EEPROM interface SHOULD drive Hi-Z or keep tristate during this period. See **Chapter 4.6 EEPROM Access** for more detail. |

**Table 3    IO Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 81 | XOVEN | I | PD, LVTTL | **Cross Over Enable**<br>Value on this pin (active low) will be latched by ADM6996LC/LCX/LHX at the rising edge of RESETL for port 4~0 crossover auto detect (Only available in TP interface).<br>*Note: Power On Setting.*<br>$0_B$     Disable<br>$1_B$     Enable |
|  | EESK | I/O | 4 mA, PD, LVTTL | **EEPROM Serial Clock**<br>During ADM6996LC/LCX/LHX initialization, this pin is used to output clock to EEPROM. After ADM6996LC/LCX/LHX initialization process is done, this pin is used as EEPROM interface clock input if **IFSEL** = 1. |
|  | SDC | I | PD, LVTTL | **Serial Management interface Clock input**<br>If **IFSEL** = 0, this pin is used as a serial management interface clock input. |
| 79 | LED_MODE | I | PD, LVTTL | **Enable Mac to Choose LED Display Mode**<br>Value on this pin will be latched by ADM6996LC/LCX/LHX at the rising edge of RESETL as Dsingle/dual color LED mode control signal. See **Chapter 3.23 LED Display** for more detail.<br>*Note: Power On Setting.* |
|  | EDI | I/O | 8 mA, PD, LVTTL | **EEPROM Serial Data Input**<br>During ADM6996LC/LCX/LHX initialization, this pin is used to output address and command to access EEPROM. After the initialization process is done, this pin becomes an input pin to monitor EEPROM data if **IFSEL** = 1. |
|  | SDIO | I/O | 8 mA, PD, LVTTL | **Serial Management interface Data input/Output**<br>If **IFSEL** = 0, this pin is used as data input/output pin of serial management interface. |
| **Power/Ground, 48 Pins** | | | | |
| 10, 23, 36, 42, 125 | GNDA | GND | – | **Ground**<br>Used by AD Block |
| 7, 20, 33, 45, 122 | VCCA2 | PWR | – | **1.8 V, Power**<br>Used by TX Line Driver |
| 13, 26, 39, 128 | VCCAD | PWR | – | **3.3 V, Power**<br>Used by AD Block |
| 119 | GNDBIAS | GND | – | **Ground**<br>Used by Bias Block |
| 121 | VCCBIAS | PWR | – | **3.3 V, Power**<br>Used by Bias Block. |
| 116 | GNDPLL | GND | – | **Ground**<br>Used by PLL |

**Table 3    IO Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 115 | VCCPLL | PWR | – | **1.8 V, Power**<br>Used by PLL |
| 47, 52, 64, 76, 83, 93 | GNDIK | GND | – | **Ground**<br>Used by Digital Core |
| 48, 53, 75, 82, 94, 110 | VCCIK | PWR | – | **1.8 V, Power**<br>Used by Digital Core |
| 46, 57, 70, 87, 99, 104 | GNDO | GND | – | **Ground**<br>Used by Digital Pad |
| 56, 71, 88, 105 | VCC3O | PWR | – | **3.3 V, Power**<br>Used by Digital Pad |
| **Miscellaneous** | | | | |
| 62 | P4FX | I | PD, LVTTL | **Port 4 Fiber Selection**<br>During power on reset, value will be latched by ADM6996LC/LCX/LHX at the rising edge of RESETL as Port 4 Fiber select.<br>$0_B$    Twisted Pair Mode<br>$1_B$    Fiber Mode |
| 65 | INT_N | O | OD,8 mA | **Interrupt**<br>Active low interrupt signal to indicate the status change in the interrupt status register. Interrupt signal will keep active low until host read the status of ISR register.<br>$0_B$    Interrupt<br>$1_B$    Not interrupt |
| 69 | WAIT_INIT | I | PD, LVTTL | **Wait Initialization**<br>This pin will be used to pause all activities after power up until EEPROM is loaded successfully or CPU initialization is done.<br>$0_B$    pause until loading EEPROM is done.<br>$1_B$    pause until EEPROM successfully loaded or CPU initialization is done. |
| 1, 2, 3, 4, 5, 6, 14, 15, 16, 17, 18, 19, 27, 28, 29, 30, 31, 32 | NC | - | - | **Not Connected** |
| 49 | TEST | I | PD, LVTTL | **Test Mode**<br>Reserved and should be kept 0 when under normal operation. |
| 86 | CFG0 | I | PU, LVTTL | **Configuration 0**<br>Reserved and should be kept 0 when under normal operation. |
| 85 | CKO25M | O | 8 mA, PD, LVTTL | **25MHz Clock Output**<br>Free Running 25 MHz Clock output (Even during power on reset) |

**Table 3    IO Signals** (cont'd)

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|---|---|---|---|
| 112 | RC | I | ST | **RC Input For Power On Reset**<br>This pin is sampled by using the 25 MHz free running clock signal which inputs from **XI** to generate the low-active reset signal, RESETL. See **Chapter 7.3.2 Power On Reset** for the timing requirement. |
| 113 | XI | AI | ANA | **25MHz Crystal /Oscillator Input**<br>25MHz Crystal or Oscillator Input. Variation is limited to +/- 50ppm. |
| 114 | XO | AO | ANA | **25M Crystal Output**<br>When connected to oscillator, this pin should be left unconnected. |
| 120 | RTX | AI | ANA | **Constant Voltage Reference**<br>External 1.0 kΩ 1% resistor connection to ground. |
| 118 | VREF | AI | ANA | **Analog Reference Voltage**<br>Used by Internal Bias Circuit for voltage reference.<br>External 0.1uF capacitor connection to ground for noise filter. |
| 117 | CONTROL | AI/O | ANA | **FET Control Signal**<br>The pin is used to control FET for 3.3 V to 1.8 V regulator. External 0.1uF capacitor connection to ground for noise filter, even the pin is un-connected. |

# 3 Function Description

## 3.1 Functional Descriptions

The ADM6996LC/LCX/LHX integrates five 100Base-X physical sub-layer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, five complete 10Base-T modules, a 6 port 10/100 switch controller and one 10/100 MII/GPSI MAC and memory into a single chip for both 10Mbit/s, 100Mbit/s Ethernet switch operation. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either Full Duplex mode or Half-Duplex mode in 10Mbit/s and 100Mbit/s. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The ADM6996LC/LCX/LHX consists of three major blocks:

- 10/100M PHY Block
- Switch Controller Block
- Built-in SSRAM

The interfaces used for communication between the PHY block and switch core is an MII interface.

An auto MDIX function is supported in this block. This function can be Enabled and Disabled by the hardware pin.

## 3.2 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair transceiver (PMD)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

## 3.3 100Base-X Module

The ADM6996LC/LCX/LHX implements a 100Base-X compliant PCS and PMA and 100Base-TX compliant TP-PMD as illustrated in Figure 2. Bypass options for each of the major functional blocks within the 100Base-X PCS provides flexibility for various applications. 100Mbit/s PHY loop back is included for diagnostic purpose.

## 3.4 100Base-X Receiver

The 100Base-X receiver consists of functional blocks required to recover and condition the 125Mbit/s receive data stream. The ADM6996LC/LCX/LHX implements the 100Base-X receiving state machine diagram as given in the ANSI/IEEE Standard 802.3u, Clause 24. The 125Mbit/s receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional sub-blocks:

- A/D Converter
- Adaptive Equalizer and timing recovery module
- NRZI/NRZ and serial/parallel decoder
- De-scrambler
- Symbol alignment block
- Symbol Decoder

- Collision Detect Block
- Carrier sense Block
- Stream decoder block

### 3.4.1 A/D Converter

A high performance A/D converter with a 125 MHz sampling rate converts signals received on the RXP/RXN pins to 6 bits data streams. It possess an auto-gain-control capability that will further improve receive performance especially under long cabling or harsh detrimental signal integrity. Due to high pass characteristic on a transformer, a built in base-line-wander correcting circuit will be cancelled out and its DC level restored.

### 3.4.2 Adaptive Equalizer and timing Recovery Module

All digital design is especially immune to noise environments and achieves better correlation between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates for line loss induced from twisted pairs and tracks a far end clock at 125M samples per second. Adaptive Equalizer's implemented with Feed forward and Decision Feedback techniques meet the requirement of BER with less than 10-12 for transmission on a CAT5 twisted pair cable ranging from 0 to 120 meters.

### 3.4.3 NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to the 4B/5B code group's boundary.

### 3.4.4 Data De-scrambling

The de-scrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and de-scrambled.

In order to maintain synchronization, the de-scrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the de-scrambler the hold timer starts a 722 micro second countdown. Upon detection of sufficient idle symbols within the 722 micro sec. period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given an operating network connection operating with good signal integrity. If the link state monitor does not recognize sufficient unscrambled idle symbols within the 722 micro second period, the de-scrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

### 3.4.5 Symbol Alignment

The symbol alignment circuit in the ADM6996LC/LCX/LHX determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the de-scrambler. Once the /J/K symbol pair (11000 10001$_B$) is detected, subsequent data is aligned on a fixed boundary.

### 3.4.6 Symbol Decoding

The symbol decoder functions is a look-up table that translates incoming 5B symbols into 4B nibbles as shown in Table 1. The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with a MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the internal RXD[3:0] signal lines where RXD[0] represents the least significant bit of the translated nibble.

### 3.4.7 Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are being presented on the internal RXD[3:0] synchronous receive clock, RXCLK. RXDV is asserted when the first nibble of a translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is de-asserted.

### 3.4.8 Receive Errors

The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

### 3.4.9 100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmit and receive operations until such time that a valid link is detected.

The ADM6996LC/LCX/LHX performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10Mbit/s link status to form the reportable link status bit in the serial management register 1h, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 micro secs, and waits for an enable from the auto negotiation module. When received, the link-up state is entered, and the transmission and reception logic blocks become active. Should auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

### 3.4.10 Carrier Sense

Carrier sense (CRS) for 100Mbit/s operation is asserted upon the detection of two non contiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle symbol pair is detected in the received data stream, CRS is de-asserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

### 3.4.11 Bad SSD Detection

A Bad Start of Stream Delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if a carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, then the ADM6996LC/LCX/LHX will assert RXER and present RXD[3:0] = $1110_B$ to the internal MII for the cycles that correspond to received 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become de-asserted.

### 3.4.12 Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will be receiving valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all $1_B$'s to a group of 84 $1_B$'s followed by a single $0_B$. This is referred to as the FEFI idle pattern.

## 3.5 100Base-TX Transceiver

The ADM6996LC/LCX/LHX implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmit driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetic for both the 10Base-T and the 100Base-TX transmissions with a simple RC component connection. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmission output driver selection.

### 3.5.1 Transmit Drivers

The ADM6996LC/LCX/LHX 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range as specified in the ANSI TP-PMD standard.

### 3.5.2 Twisted-Pair Receiver

For 100Base-TX operation, the incoming signal is detected by the on-chip twisted-pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuits.

The ADM6996LC/LCX/LHX uses an adaptive equalizer that changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

## 3.6 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loop back, jabber, wave shaper, and link integrity functions, as defined in the standard. Figure 3 provides an overview for the 10Base-T module.

The ADM6996LC/LCX/LHX 10Base-T module is comprised of the following functional blocks:

- Manchester encoder and decoder
- Collision detector
- Link test function
- Transmit driver and receiver
- Serial and parallel interface
- Jabber and SQE test functions
- Polarity detection and correction

### 3.6.1 Operation Modes

The ADM6996LC/LCX/LHX 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the ADM6996LC/LCX/LHX functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmit and receive. In full duplex mode the ADM6996LC/LCX/LHX can simultaneously transmit and receive data.

### 3.6.2 Manchester Encoder/Decoder

Data encoding and transmission begins when the transmission enable input (TXEN) goes high and continues as long as the transceiver is in a good link state. Transmission ends when the transmission enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a $1_B$, or at the boundary of the bit cell if the last bit is $0_B$.

Decoding is accomplished using a differential input receiver circuit and a phase-locked loop that separate the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when

no more mid bit transitions are detected. Within one and a half bit times after the last bit, carrier sense is de-asserted.

### 3.6.3 Transmit Driver and Receiver

The ADM6996LC/LCX/LHX integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmission signal are attenuated properly.

### 3.6.4 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential receive. The ADM6996LC/LCX/LHX implements an intelligent receive squelch on the RXP/RXN differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of the packet is checked by the analog squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating the end of a packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise, causing premature end-of-packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 10 of register address $11_H$.

### 3.7 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbit/s half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbit/s full duplex and repeater mode operations, the CRS is asserted only due to receive activity.

### 3.8 Jabber Function

The jabber function monitors the ADM6996LC/LCX/LHX output and disables the transmitter if it attempts to transmit a longer than legal sized packet. If TXEN is high for greater than 24ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be de-asserted for approximately 256 ms (the un-jab time) before the jabber function re-enables the transmit outputs. The jabber function can be disabled by programming bit 4 of register address $10_H$ to high.

### 3.9 Link Test Function

A link pulse is used to check he integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.

The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100ns in duration and is transmitted every 16 ms, in the absence of transmit data.

## 3.10 Automatic Link Polarity Detection

The ADM6996LC/LCX/LHX's 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 5 of register $10_H$.

## 3.11 Clock Synthesizer

The ADM6996LC/LCX/LHX implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz +/- 50ppm

## 3.12 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The ADM6996LC/LCX/LHX supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

Highest priority is relative to the following list:

• 100Base-TX full duplex (highest priority)
• 100Base-TX half duplex
• 10Base-T full duplex
• 10Base-T half duplex (lowest priority)

## 3.13 Memory Block

The ADM6996LC/LCX/LHX's built in memory is divided into two blocks. One is a MAC addressing table and the other one is a data buffer.

The MAC address Learning Table size is 2K entries with each entry occupying eight bytes length. These eight bytes of data include a 6 byte source address, VLAN information, Port information and an aging counter.

A data buffer is divided into 256 bytes/block. The ADM6996LC/LCX/LHX buffer management is per port fixed block number and all ports share one global buffer. This architecture can get better memory utilization and network balance at different speeds and duplex test conditions.

Received packets will separate into several 256 bytes/block and chain together. If a packet size is more than 256 bytes then the ADM6996LC/LCX/LHX will chain two or more blocks to store receiving packets.

## 3.14 Switch Functional Description

The ADM6996LC/LCX/LHX uses a "store & forward" switching approach for the following reason:

• Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require large elastic buffers especially when bridging between a server on a 100 Mbit/s network and clients on a 10 Mbit/s segment.
• Store & forward switches improve overall network performance by acting as a "network cache"
• Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

## 3.15 Basic Operation

The ADM6996LC/LCX/LHX receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port within the same VLAN group, where

appropriate. If the destination address is not found in the address table, the ADM6996LC/LCX/LHX treats the packet as a broadcast packet and forwards the packet to the other ports within the same VLAN group.

The ADM6996LC/LCX/LHX automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed. If the Source Address is not found in the Address Table, the device adds it to the table.

## 3.15.1    Address Learning

A four-way hash algorithm is implemented to allow the maximum of 4 different addresses with the same hash key to be stored at the same time. Up to 2K entries can be created and all entries are stored in the internal SSRAM. An address is stored in the Address Table. The ADM6996LC/LCX/LHX searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

1. If the SA was not found in the Address Table (a new address), the ADM6996LC/LCX/LHX waits until the end of the packet (non-error packet) and updates the Address Table. If the SA was found in the Address Table, then the aging value of each corresponding entry will be reset to $0_B$.
2. When the DA is PAUSE command, then the learning process will be disabled automatically by ADM6996LC/LCX/LHX.

## 3.15.2    Address Recognition and Packet Forwarding

The ADM6996LC/LCX/LHX forwards the incoming packets between bridged ports according to the Destination Address (DA) as below. All the packet forwarded will check the VLAN first. A forwarding port must be the within the same VLAN as the source port.

If the DA is a UNICAST address and the address was found in the Address Table, the ADM6996LC/LCX/LHX will check the port number and act as follows:

- If the port number is equal to the port on which the packet was received, the packet is discarded.
- If the port number is different, the packet is forwarded across the bridge.
- If the DA is a UNICAST address and the address was not found, the ADM6996LC/LCX/LHX treats it as a multicast packet and forwards it across the bridge.
- If the DA is a Multicast address, the packet is forwarded across the bridge.
- If the DA is a PAUSE Command (01 80 C2 00 00 $01_H$), then this packet will be dropped by the ADM6996LC/LCX/LHX. The ADM6996LC/LCX/LHX can issue and learn PAUSE commands.
- The ADM6996LC/LCX/LHX will forward the packet with a DA of (01 80 C2 00 00 $00_H$), filter out the packet with a DA of (01 80 C2 00 00 01 $_H$), and forward a packet with a DA of (01-80-C2-00-00-$02_H$ to 01 80 C2 00 00 $0F_H$)

## 3.15.3    Address Aging

Address aging is supported for topology changes such as an address moving from one port to another. When this happens, the ADM6996LC/LCX/LHX internally has a 300 second timer which will "age-out" (remove) the address from the address table. The aging function can be enabled/disabled by the user. Normally, disabling an aging function is for security purposes.

## 3.15.4    Back off Algorithm

The ADM6996LC/LCX/LHX implements the truncated exponential back off algorithm compliant to the 802.3 CSMA-CD standard. The ADM6996LC/LCX/LHX will restart the back off algorithm by choosing 0-9 collision counts. The ADM6996LC/LCX/LHX resets the collision counter after 16 consecutive retransmit trials.

## 3.15.5    Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The typical number is 96 bits at a time. The value is 9.6 micro secs for 10 Mbit/s Ethernet, 960ns for 100 Mbit/s fast Ethernet and 96ns for 1000M.

The ADM6996LC/LCX/LHX provides an option of 92 bit gap in an EEPROM to prevent packet loss when Flow Control is turned off and clock P.P.M. values differ.

### 3.15.6 Illegal Frames

The ADM6996LC/LCX/LHX will discard all illegal frames such as runt packets (less than 64 bytes), oversized packets (greater than 1518 or 1522 bytes) and bad CRC. Dribbling packing with good CRC value will be accepted by the ADM6996LC/LCX/LHX. In case of bypass mode enable, the ADM6996LC/LCX/LHX will support tag and untagged packets with sizes up to 1522 bytes. In case of non-bypass mode, the ADM6996LC/LCX/LHX will support tag packets up to 1526bytes and untagged packets up to 1522bytes.

### 3.15.7 Half Duplex Flow Control

A back pressure function is supported for half-duplex operations. When the ADM6996LC/LCX/LHX cannot allocate a receive buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision. Back Pressure is enabled by the BPEN set during RESET assertion. An Infineon proprietary algorithm is implemented inside the ADM6996LC/LCX/LHX to prevent the back pressure function causing HUB partitioned under heavy traffic environment and reducing the packet loss rate to increase the whole system performance.

### 3.15.8 Full Duplex Flow Control

When full duplex port run out of its receive buffer, a PAUSE packet command will be issued by ADM6996LC/LCX/LHX to notice the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. ADM6996LC/LCX/LHX can issue or receive pause packet.

### 3.15.9 Old Broadcast Storm filter (0x0b[0]=0 and 0x11[6]=0)

If the Broadcast Storm filter is enabled, the broadcast packets over 50 ms of the threshold will be discarded by the threshold setting. See EEPROM Reg.$10_H$.

Broadcast storm mode:

Time interval: 50ms

Max. packet number = 7490 in 100Base, 749 in 10Base

**Table 4     The max. packet number = 7490 in 100Base, 749 in 10Base**

**Per Port Falling Threshold**

|  | $00_B$ | $01_B$ | $10_B$ | $11_B$ |
|---|---|---|---|---|
| All 100TX | Disable | 7440fps | 14880fps | 29760fps |
| Not All 100TX | Disable | 744fps | 1488fps | 2976fps |

**Table 5     The max. packet number = 7490 in 100Base, 749 in 10Base**

**Per Port Rising Threshold**

|  | $00_B$ | $01_B$ | $10_B$ | $11_B$ |
|---|---|---|---|---|
| All 100TX | Disable | 14880fps | 29760fps | 59520fps |
| Not All 100TX | Disable | 1488fps | 2976fps | 5952fps |

### 3.15.10 New Broadcast/Multicast Storm (0x0b[0]=1 and 0x11[6]=1)

ADM6996LC/LCX allows users to limit the traffic of the broadcast address (DA = $FFFFFFFFFFFF_H$) to prevent them from blocking the switch bandwidth. If users also want to limit the multicast packets(DA[40] = $1_B$), they can

set the Multicast Packet Counted into Storming Counter (see $0010_H[5]$) function. Two thresholds and storm enable bits (see $003B_H$ and $003C_H$) are used to control the broadcast storm.

1. Time Scale. ADM6996LC/LCX uses 50ms as a scale to meter the storm packets.

| Parameter | Rising Threshold | Falling Threshold |
|---|---|---|
| All link ports are 100M | 100M Threshold (See $003B_H[12:0]$) | 1/2 100M Threshold |
| All link ports are not all 100M | 10M Threshold (See $003C_H[12:0]$) | 1/2 10M Threshold |

2. Storm keeps on at least 1.6 seconds if any of the ports meets the rising threshold in the 4 consecutive 50 ms intervals. In these 1.6 seconds, the ports meeting the rising threshold will start to discard the broadcast or multicast packets until the 50 ms interval expires. Users could also disable Input Filter (see $000B_H[14]$) function to forward above packets to the un-congested port instead of discarding directly.

3. Storm finishes. After the 1.6-second storm period, ADM6996LC/LCX will check the port that makes the storm on. If all of these ports meet the falling threshold in the 2 consecutive 50 ms intervals and no other ports satisfy the rising threshold at the same time, the storm will finish.

## 3.16 Auto TP MDIX function

At normal application which Switch connect to NIC card is by one by one TP cable. If Switch connect other device such as another Switch must by two way. First one is Cross Over TP cable. Second way is use extra RJ45 which crossover internal TX+- and RX+- signal. By second way customer can use one by one cable to connect two Switch devices. All these effort need extra cost and not good solution. ADM6996LC/LCX/LHX provide Auto MDIX function which can adjust TX+- and RX+- at correct pin. User can use one by one cable between ADM6996LC/LCX/LHX and other device. This function can be Enable/Disable by hardware pin and EEPROM configuration register $01_H \sim 09_H$ bit 15. If hardware pin set all port at Auto MDIX mode then EEPROM setting is useless. If hardware pin set all port at non Auto MDIX mode then EEPROM can set each port this function enable or disable.

## 3.17 Port Locking

Port locking function will provide customer simple way to limit per port user number to one. If this function is turn on then ADM6996LC/LCX/LHX will lock first MAC address in learning table. After this MAC address locking will never age out except Reset signal. Another MAC address which not same as locking one will be dropped. ADM6996LC/LCX/LHX provide one MAC address per port. This function is per port setting. When turn on Port Locking function, recommend customer turn off aging function. See EEPROM register $12_H$ bit 0~8.

## 3.18 VLAN setting & Tag/Untag & port-base VLAN

ADM6996LC/LCX/LHX supports bypass mode and untagged port as default setting while the chip is power-on. Thus, every packet with or without tag will be forwarded to the destination port without any modification by ADM6996LC/LCX/LHX. Meanwhile port-base VLAN could be enabled according to the PVID value (user define 4bits to map 16 groups written at register $13_H$ to register $22_H$) of the configuration content of each port.

ADM6996LC/LCX/LHX also supports 16 802.1Q VLAN groups. In VLAN four bytes tag include twelve VLAN ID. ADM6996LC/LCX/LHX learn user define four bits of VID. If user need to use this function, two EEPROM registers are needed to be programmed first:

* Port VID number at EEPROM register $01_H \sim 09_H$ bit 13~10, register $28_H \sim 2B_H$ and register $2C_H$ bit 7~0: ADM6996LC/LCX/LHX will check coming packet. If coming packet is non VLAN packet then ADM6996LC/LCX/LHX will use PVID as VLAN group reference. ADM6996LC/LCX/LHX will use packet's VLAN value when receive tagged packet.

* VLAN Group Mapping Register. EEPROM register $13_H \sim 22_H$ define VLAN grouping value. User use these register to define VLAN group.

User can define each port as Tag port or Untag port by Configuration register Bit 4. The operation of packet between Tag port and Untag port can explain by follow example:

**Example1: Port receives Untag packet and send to Untag port.**

ADM6996LC/LCX/LHX will check the port user define four bits of VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port then this packet will forward to destination port without any change. If destination port not same VLAN as receiving port then this packet will be dropped.

**Example2: Port receives Untag packet and send to Tag port.**

ADM6996LC/LCX/LHX will check the port user define fours bits of VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port with four byte VLAN Tag and new CRC. If destination port not same VLAN as receiving port then this packet will be dropped.

**Example3: Port receives Tag packet and send to Untag port.**

ADM6996LC/LCX/LHX will check the packet VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port after remove four bytes with new CRC error. If destination port not same VLAN as receiving port then this packet will be dropped.

**Example4: Port receives Tag packet and send to Tag port.**

ADM6996LC/LCX/LHX will check the user define packet VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port without any change. If destination port not same VLAN as receiving port then this packet will be dropped.

## 3.19 Old Fixed Ingress Bandwidth Control (0x0b[0]=0)

ADM6996LC/LCX/LHX also supports ADM6996L compatible Bandwidth Control with fixed rate.

**Table 6 Fixed Ingress Bandwidth Control**

| 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
|------|------|-----|-----|-----|-----|-----|-----|
| 256K | 512k | 1M  | 2M  | 5M  | 10M | 20M | 50M |

## 3.20 New Scalable Egress/Ingress Bandwidth Control (0x0b[0]=1 and 0x33[12]=1)

Bandwidth control function is useful on community networks for different levels of service. ADM6996LC/LCX/LHX provides Scalable Egress/Ingress Bandwidth Control. Users can set any value that is based on a 64K unit.

## 3.21 MAC Table Accessible

CPU accesses Switch internal MAC table is provided by ADM6996LC/LCX/LHX. CPU can Search, Add, Delete and Set ADM6996LC/LCX/LHX internal MAC table through a serial interface.

Search: CPU can search target MAC address Switch port number.

Add: CPU can add MAC address to learning table.

Delete: CPU can delete MAC address from learning table.

Set MAC Address: CPU can set MAC address as Static or no Static address. Static means not aging out.

## 3.22 Priority Setting

It is a trend that data, voice and video will be put on networking, Switch not only deal data packet but also provide service of multimedia data. ADM6996LC/LCX/LHX provides two priority queues on each port with N:1 rate. See EEPROM Reg.10$_H$.

This priority function can set three ways as below:

* By Port Base: Set specific port at specific queue. ADM6996LC/LCX/LHX only check the port priority and not check packet's content VLAN and TOS.

\* By VLAN first: ADM6996LC/LCX/LHX check VLAN three priority bit first then IP TOS priority bits.

\* By IP TOS first: ADM6996LC/LCX/LHX check IP TOS three priority bit first then VLAN three priority bits.

If port set at VLAN/TOS priority but receiving packet without VLAN or TOS information then port base priority will be used.

\* By TCP/UDP Destination Port Number: ADM6996LC/LCX/LHX check Layer4 TCP/UDP Destination Port number to map the priority queue.

\* By MAC Destination Address: User can set MAC address to map priority queue.

## 3.23 LED Display

Three LEDs per port are provided by ADM6996LC/LCX/LHX. Link/Act, Duplex/Col. & Speed are three LED display of ADM6996LC/LCX/LHX. Dual color LED mode also supported by ADM6996LC/LCX/LHX. For easy production purpose ADM6996LC/LCX/LHX will send test signal to each LED at power on reset stage. EEPROM register $12_H$ define LED configuration table.

1. **LED_MODE**: It is the value latched on the EDI pin during the power on reset. It's also used to control the dual or single color mode and is useless when the value wait_init is high.
2. **DCS** (see $0012_H$): Dupcol LEDs indicate the duplex status only.
3. **DHCOL** (See $0030_H$): When enabled, pin DUPCOL0 shows col_10m status and pin DUPCOL1 shows col_100m status. These two LEDs are necessary in the dual-speed hub.

ADM6996LC/LCX/LHX LED is active Low signal. Dupcol0 & Dupcol1 will check external signal at Reset time. If external signal add pull high then LED will active Low. If external signal add pull down resister then LED will drive high.

### 3.23.1 Single Color LED Display

**Table 7    Single Color LED Display**

| Pin Name | Status |
|---|---|
| LNKACT4/LNKACT3/ LNKACT2/LNKACT1/ LNKACT0 | These pins have no power on reset values on them, and ADM6996LC/LCX/LHX uses active low value to drive the led. So the output values of these pins after the power on reset are shown as follows: <br> 1. First period: This period lasts 1.28 s for LED on test. ADM6996LC/LCX/LHX drives value 0 to open the LED. <br> 2. Second period: This period lasts 0.48 s for LED off test. ADM6996LC/LCX/LHX drives value 1 to close the LED. <br> 3. Normal Period: Tis period indicates the link status. <br> $0_B$    Port links up and LED is ON. <br> $1_B$    Port links down and LED is OFF. <br> $0/1_B$    Port links up and is transmitting or receiving. The LED flashes at 10 Hz. |
| LDSPD4/LDSPD3/ LDSPD2/LDSPD1/ LDSPD0 | The behavior of these pins is the same as the LNKACT, except the normal period. <br> Normal period: This period indicates the speed status. <br> $0_B$    Port links up and its speed is 100M. LED is ON. <br> $1_B$    Port links down or its speed is 10M. LED is OFF. |

**Table 7    Single Color LED Display** (cont'd)

| Pin Name | Status |
|---|---|
| DUPCOL2/ DUPCOL1/ DUPCOL0 | These 3 pins have power on reset values on them. ADM6996LC/LCX/LHX needs to consider these values to drive the correct value. If the power on reset value is value_power_on, then the display is as follows:<br>1. First period: This period lasts 1.28 s for LED on test. ADM6996LC/LCX/LHX drives ~value_power_on to open the LED.<br>2. Second period: This period lasts 0.48 s for LED off test. ADM6996LC/LCX/LHX drives value_power_on to close the LED.<br>3. Normal Period: Tis period indicates the duplex/collision status.<br>~value_power_on = Port links up in the full-duplex mode. LED is ON.<br>value_power_on = Port links down. LED flashes at 10 Hz.<br>$0/1_B$   Port links up and collision is detected. The LED flashes at 10 Hz.<br>If **DCS** is enabled, the normal period changes its way to display.<br>~value_power_on = Port links up in the duplex mode. LED is ON.<br>value_power_on = Port links down or links up in the half-duplex mode. LED is OFF.<br>$0/1_B$   This value is cancelled. LED doesn't blink.<br>If **DHCOL** is enabled, the display in the normal period is as follows:<br>DUPCOL0: 10m collision indicator.<br>$0/1_B$   One of the ports links up in 10M half-duplex mode and detects a collision event. The LED flashes at 20 Hz.<br>value_power_on = When the above event is not satisfied, the LED is OFF.<br>DUPCOL1: 100 m collision indicator.<br>$0/1_B$   One of the ports links up in 100M half-duplex mode and detects a collision event. The LED flashes at 20 Hz.<br>value_power_on = The above event is not satisfied. LED is OFF. |
| DUPCOL4/ DUPCOL3 | The behavior of these pins is the same as the LNKACT, except for the normal period.<br>Normal period: This period indicates the duplex/collision status.<br>~value_power_on = Port links up in the full-duplex mode. LED is ON.<br>value_power_on = Port links down. LED is OFF.<br>$0/1_B$   Port links up and collision is detected. The LED flashes at 10 Hz.<br>If **DCS** is enabled, the normal period changes its way to display.<br>~value_power_on = Port links up in the duplex mode. LED is ON.<br>value_power_on = Port links down or links up in the half-duplex mode. LED is OFF.<br>$0/1_B$   This value is cancelled. LED doesn't blink. |

### 3.23.2    Dual Color LED Display

Users should be careful that DUPCOL LED only supports the single color mode. The only difference between single and dual color for DUPCOL LED is the self-test time.

**Table 8    Dual Color LED Display**

| Pin Name | Status |
|---|---|
| (LNKACT4, LDSPD4)/ (LNKACT3, LDSPD3) (LNKACT2, LDSPD2) (LNKACT1, LDSPD1) (LNKACT0, LDSPD0) | First Period: Test LED on with green color. It lasts 1.28 s. $01_B$    LED is on with green color. Second Period: Test LED on with yellow color. It lasts 1.28 s. $10_B$    LED is on with yellow color. Third period: Test LED off. $00_B$    LED is off. Normal Period: This period shows the status of the link and speed at the same time. $00_B$          Port links down.LED is off. $11_B$          Port links down. LED is off. $01_B$          Port links up in 100M. LED glows green. $10_B$          Port links up in 10M. LED glows yellow. $0/1,1_B$        Port links up in 100M and is receiving or transmitting. LED blinks with green color at 10 Hz. $0/1,0_B$        Port links up in 10M and is receiving or transmitting. LED blinks with yellow color at 10 Hz. |
| DUPCOL4/DUPCOL3/ DUPCOL2/DUPCOL1/ DUPCOL0 | The behavior of these pins is the same as the single mode, except the self-test period. The LED on test period is 2.56 s instead of 1.28 s. |

### 3.23.3    Circuit for Single LED Mode
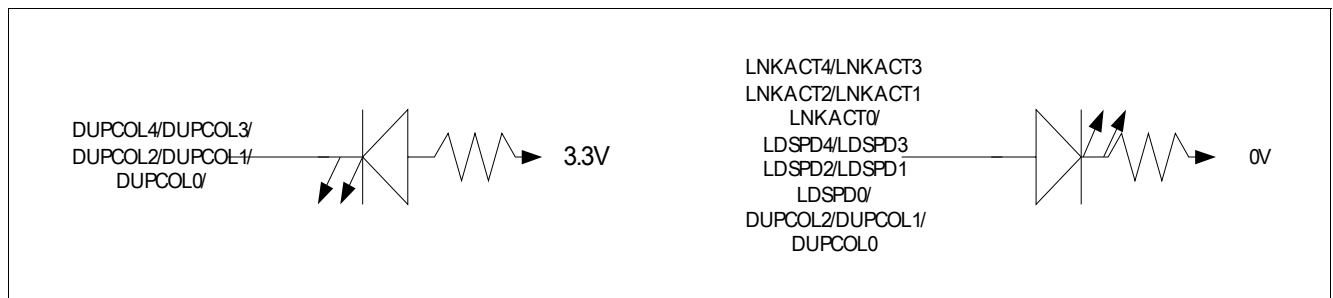


**Figure 3    Circuit for Single Color LED Mode**

### 3.23.4    Circuit for Dual Led Mode
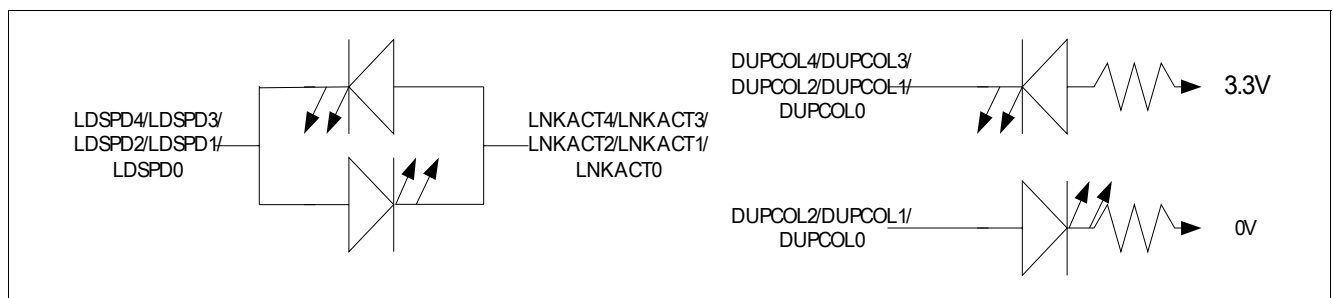


**Figure 4    Circuit for Dual Color LED Mode**

## 3.24    MAC Clone and Port5 MII connection

In ADM6996LC/LCX, there are three different configurations (MAC type MII mode, GPSI mode and RMII, **P5_BUSMD0**) for Port5 to connect the CPU's MII/GPSI or RMII interface.

Here we dipicted a general router applications of ADM6996LC/LCX, connected to CPU with single MII. In **Figure 5**, we can see either LAN to WAN or WAN to LAN, the packets will go through the same MII port. Because the CPU need to send out the packets with the registered MAC ID to the WAN port, and this MAC ID may also come in from the LAN ports. We know the switch learning scheme can't permit the packets with same MAC ID input from different port. In the ADM6996LC/LCX design, we use the MAC clone and VLAN group to solve this problem. From **Figure 6**, users can have more details for this implementation.
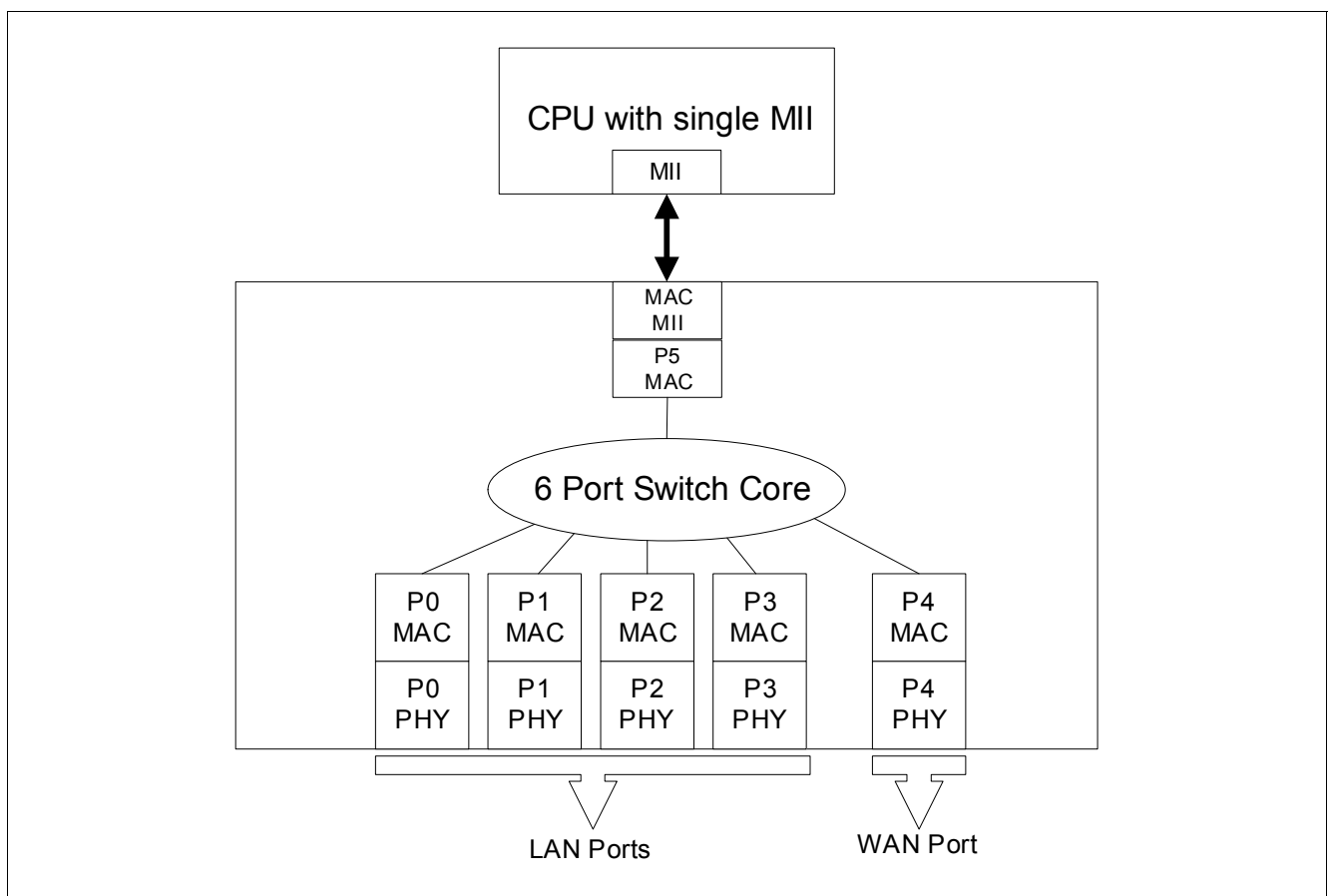


**Figure 5     ADM6996LC/LCX to CPU with single MII Connection**

Here we use an example to describe how to enable the MAC clone and set the VLAN group to reach this LAN/WAN routing activity.

CPU

3) CPU changes VID=1 to 2

2) Tag packet with VID=1          MII          4) Tag packet with VID=2

Port 5 MII, Tag, PVID=2

| Port 0 UnTag PVID=1 | Port 1 UnTag PVID=1 | Port 2 UnTag PVID=1 | Port 3 UnTag PVID=1 | Port 4 UnTag PVID=2 |

LAN Port          WAN Port

1) UnTag packet          5) UnTag packet
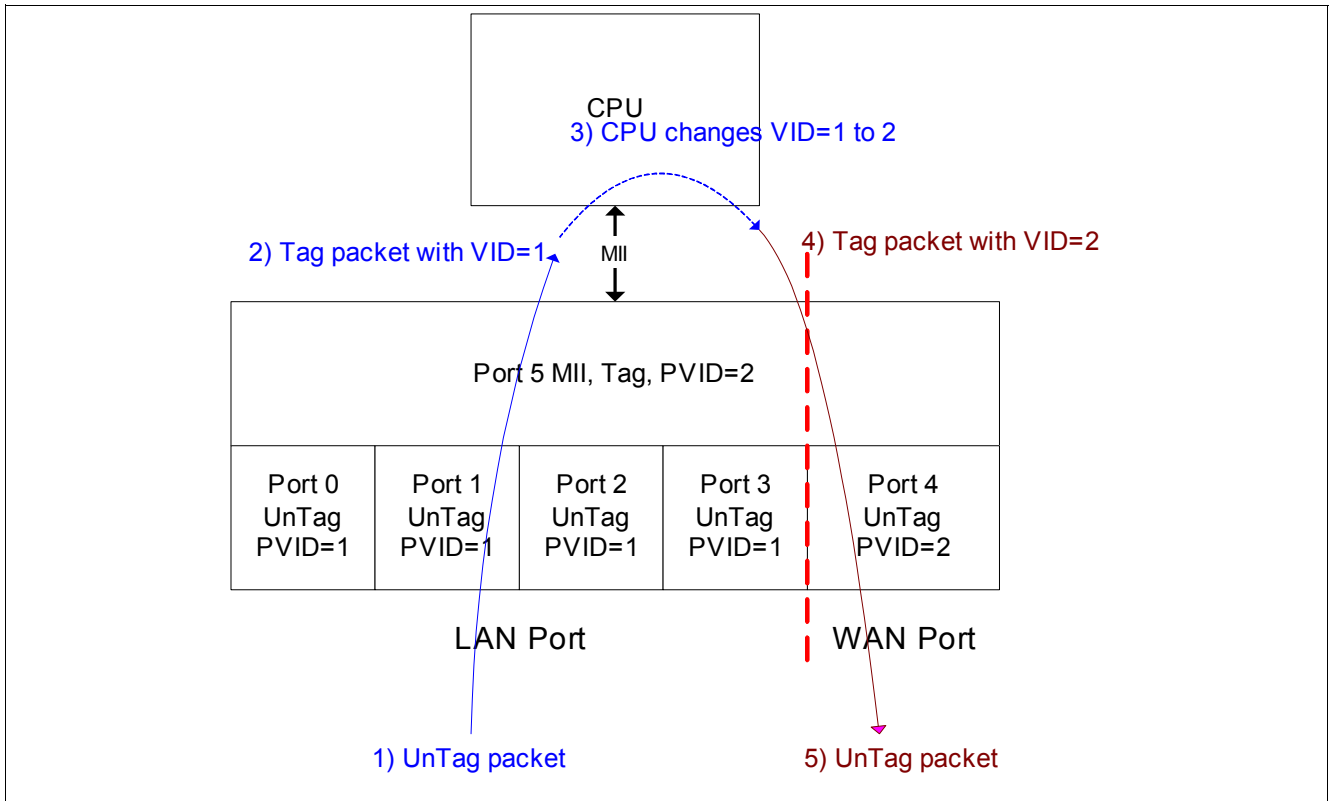
**Figure 6     MAC Clone Enable and VLAN Setting**

Step1: Set ADM6996LC/LCX to tag-based VLAN mode -- set EEPROM $0x11_H$ to $0xff20_H$

Step2: Set per port PVID and Tag/UnTag output port --

Port0, UnTag, PVID=1, set EEPROM $0x01_H$ to $0x840f_H$

Port1, UnTag, PVID=1, set EEPROM $0x03_H$ to $0x840f_H$

Port2, UnTag, PVID=1, set EEPROM $0x05_H$ to $0x840f_H$

Port3, UnTag, PVID=1, set EEPROM $0x07_H$ to $0x840f_H$

Port4, UnTag, PVID=2, set EEPROM $0x08_H$ to $0x880f_H$

Port5, Tag, PVID=2, set EEPROM $0x09_H$ to $0x881f_H$

Step3: Set WAN/LAN group

Group1: Port 0/1/2/3/5, set EEPROM $0x14_H$ to $0x0155_H$

Group2: Port 4/5, set EEPROM $0x15_H$ to $0x0180_H$

If Untag packet received from LAN port and forwards to CPU port, ADM6996LC/LCX will use ingress port PVID as the egress tag VID. CPU can recognize the source group of the packet by VID. If VID=1, it means the packet is received from the LAN port. Otherwise, if VID=2, it means the packet is received from the WAN port.

CPU has to change the tag VID to determine the destination group. The tag packet received from CPU port will follow tag-based VLAN to determine the broadcast domain. If the tag packet with VID=1 will follow VLAN group 1 (LAN group) and the tag packet with VID=2 will follow the VLAN group 2 (WAN group).

Normally, the MAC mode MII should be connected to the PCS mode MII. But in some applications, we need to connect both MAC mode MII to each other as shown in above figures. In **Figure 7**, due to most CPU's MII being MAC mode, so Port5 is MAC to MAC connected.

Through the hardware setting, it is easy to set ADM6996LC/LCX Port5 MII to operate in 100M Full Duplex mode. This mode (100M Full) is normally the operation mode to be with CPU, the interface connection is described in the following diagram.

(1) CKO25M is the 25M clock driven out by ADM6996LC/LCX to fit 100M MII operation. This clock output provides 8mA driving capability and it can directly connected to TXCLK/RXCLK.

(2) Due to it is operated in Full duplex mode, so COL is tied to GND.
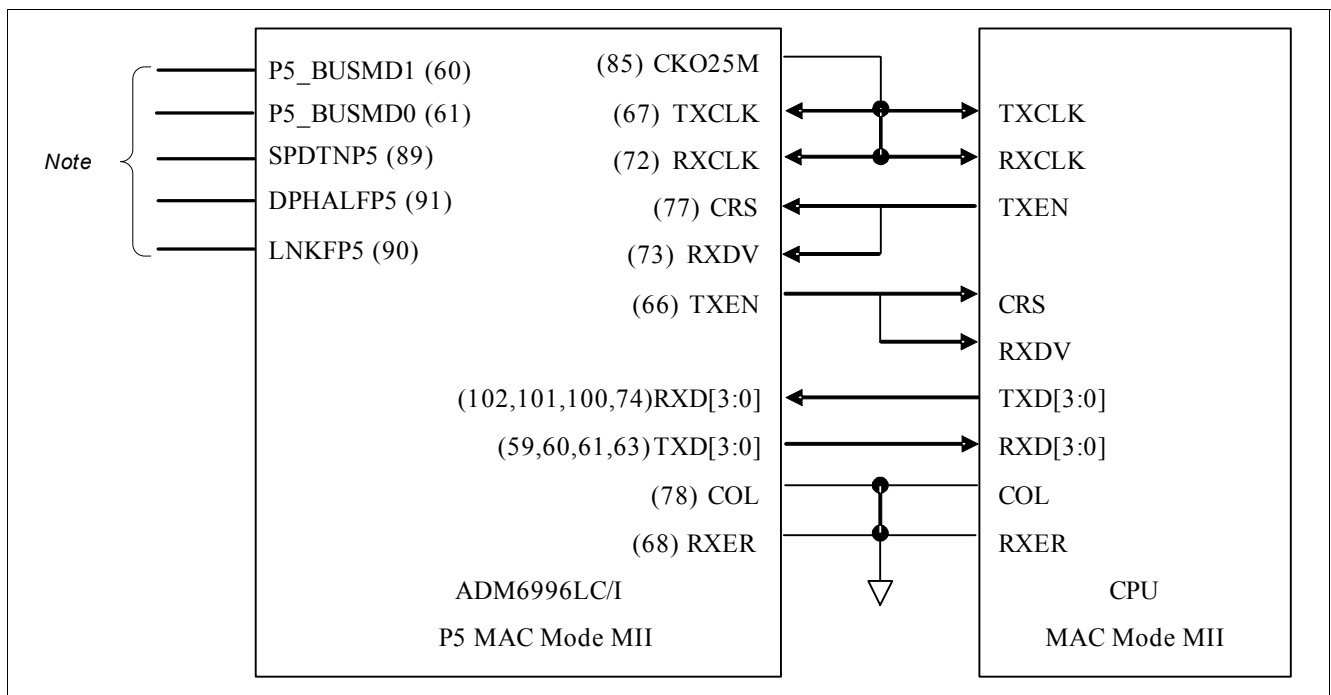


**Figure 7      100M Full duplex MAC to MAC MII Connection**

*Note:*

1. *Pin 60 and pin 61 should be pull low to let P5_BUSMD be latched as "00" and make Port5 be operating in MII mode (**P5_BUSMD0**).*
2. *Pin 89 (SPDTNP5) should be pull low or floating to set Port5 be operating in 100Mbit/s.*
3. *Pin 91 (DPHALFP5) should be pull low or floating to set Port5 be operating in full duplex mode.*
4. *Pin 90 (LNKFP5) should be pull low or floating to set Port5 Link up.*

## 3.25 The Hardware Difference between ADM6996LC/LCX/I and ADM6996L

ADM6996LC/LCX is power-down version to replace ADM6996L and ADM6996I is advanced function version to new application.

**Pin Description(QFP128)**

**Table 9    Pin Description(QFP128)**

| Pin No. | ADM6996LC/LCX | ADM6996L | Notes |
|---|---|---|---|
| 47 | GNDIK(GND Digital) | NC | GNDIK in ADM6996L datasheetAsk the customer to double-check |
| 48 | VCCIK(1.8V Digital) | NC | VCCIK in ADM6996L datasheetAsk the customer to double-check |
| 59 | P5TXD3(SDIO_MD) | P5TXD3(VOL23) | For ADM6996LC/LCX, SDIO_MD=0 default 32bit modeFor ADM6996I, SDIO_MD=0 default 16bit modeAdd pull-up/down resistor for ADM6996L/LC/I compatible design to avoid wrong power-on-latch. |
| 60 | P5TXD2(RMIISEL) | P5TXD2(ROMCODE25) | Add pull down resistor for ADM6996L/LC/I P5 MII mode to avoid wrong power-on-latch. |
| 61 | P5TXD1(7WIRE) | P5TXD1(P5GPSI) | Add pull down resistor for ADM6996L/LC/I P5 MII mode to avoid wrong power-on-latch. |
| 65 | INT_N | VCCIK(1.8V Digital) | Interrupt for Learning Table Access/Port Security/Counter Overflow/Port StatusAdd a option design to CPU INT_N pin |

# 4 32 Bits Mode Registers Description

## 4.1 EEPROM Registers (0x0b[0]=0)

**Table 10    Registers Address Space**

| Module | Base Address | End Address | Note |
|---|---|---|---|
| EEPROM | $00_H$ | $33_H$ | Independent Address Space |

**Table 11    Registers Overview**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| **SigReg** | Signature Register | $00_H$ | **43** |
| **CtrlReg_0** | Basic Control Register 0 | $01_H$ | **44** |
| **ResReg_0** | Reserved Register 0 | $02_H$ | **45** |
| CtrlReg_P1 | Basic Control Register 1 | $03_H$ | **45** |
| ResReg_1 | Reserved Register 1 | $04_H$ | **45** |
| CtrlReg_P2 | Basic Control Register 2 | $05_H$ | **45** |
| ResReg_2 | Reserved Register 2 | $06_H$ | **45** |
| CtrlReg_P3 | Basic Control Register 3 | $07_H$ | **45** |
| CtrlReg_P4 | Basic Control Register 4 | $08_H$ | **45** |
| ResReg_3 | Reserved Register 3 | $09_H$ | **45** |
| **ResReg_4** | Reserved Register 4 | $0A_H$ | **46** |
| **ConfigReg_1** | Configuration Register 1 | $0B_H$ | **46** |
| **ResReg_5** | Reserved Register 5 | $0C_H$ | **46** |
| ResReg_6 | Reserved Register 6 | $0D_H$ | **47** |
| **VLAN_Map_P** | VLAN priority Map Register | $0E_H$ | **47** |
| **TOS_Priority** | TOS priority Map Register | $0F_H$ | **48** |
| **ConfigReg_2** | Configuration Register 2 | $10_H$ | **48** |
| **VLAN_Mode** | VLAN Mode Select Register | $11_H$ | **49** |
| **ConfigReg_3** | Miscellaneous Configuration Register 3 | $12_H$ | **52** |
| **VLAN_Map_0** | VLAN mapping table registers 0 | $13_H$ | **53** |
| VLAN_Map_1 | VLAN mapping table registers 1 | $14_H$ | **54** |
| VLAN_Map_2 | VLAN mapping table registers 2 | $15_H$ | **54** |
| VLAN_Map_3 | VLAN mapping table registers 3 | $16_H$ | **54** |
| VLAN_Map_4 | VLAN mapping table registers 4 | $17_H$ | **54** |
| VLAN_Map_5 | VLAN mapping table registers 5 | $18_H$ | **54** |
| VLAN_Map_6 | VLAN mapping table registers 6 | $19_H$ | **54** |
| VLAN_Map_7 | VLAN mapping table registers 7 | $1A_H$ | **54** |
| VLAN_Map_8 | VLAN mapping table registers 8 | $1B_H$ | **54** |
| VLAN_Map_9 | VLAN mapping table registers 9 | $1C_H$ | **54** |
| VLAN_Map_10 | VLAN mapping table registers 10 | $1D_H$ | **54** |

**Table 11    Registers Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| VLAN_Map_11 | VLAN mapping table registers 11 | $1E_H$ | **54** |
| VLAN_Map_12 | VLAN mapping table registers 12 | $1F_H$ | **54** |
| VLAN_Map_13 | VLAN mapping table registers 13 | $20_H$ | **54** |
| VLAN_Map_14 | VLAN mapping table registers 14 | $21_H$ | **54** |
| VLAN_Map_15 | VLAN mapping table registers 15 | $22_H$ | **54** |
| **ResReg_7** | Reserved Register 7 | $23_H$ | **54** |
| ResReg_8 | Reserved Register 8 | $24_H$ | **55** |
| ResReg_9 | Reserved Register 9 | $25_H$ | **55** |
| ResReg_10 | Reserved Register 10 | $26_H$ | **55** |
| ResReg_11 | Reserved Register 11 | $27_H$ | **55** |
| **ConfigReg_4** | Configuration Register 4 | $28_H$ | **55** |
| **ConfigReg_5** | Configuration Register 5 | $29_H$ | **55** |
| **ConfigReg_6** | Configuration Register 6 | $2A_H$ | **56** |
| **ConfigReg_7** | Configuration Register 7 | $2B_H$ | **56** |
| **ConfigReg_8** | Configuration Register | $2C_H$ | **56** |
| **ResReg_12** | Reserved Register 12 | $2D_H$ | **57** |
| **ResReg_13** | Reserved Register 13 | $2E_H$ | **58** |
| **PH_Restart** | PHY Restart | $2F_H$ | **58** |
| **ConfigReg_** | Miscellaneous Configuration Register 9 | $30_H$ | **59** |
| **BWCon_0** | Bandwidth Control Register 0 | $31_H$ | **59** |
| **BWCon_1** | Bandwidth Control Register 1 | $32_H$ | **60** |
| **BWConEn** | Bandwidth Control Enable Register | $33_H$ | **61** |

The register is addressed wordwise.

**Table 12    Register Access Types**

| Mode | Symbol | Description HW | Description SW |
|---|---|---|---|
| read/write | rw | Register is used as input for the HW | Register is read and writable by SW |
| read | r | Register is written by HW (register between input and output -> one cycle delay) | Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.) |
| Read only | ro | Register is set by HW (register between input and output -> one cycle delay) | SW can only read this register |
| Read virtual | rv | Physically, there is no new register, the input of the signal is connected directly to the address multiplexer. | SW can only read this register |
| Latch high, self clearing | lhsc | Latch high signal at high level, clear on read | SW can read the register |
| Latch low, self clearing | llsc | Latch high signal at low-level, clear on read | SW can read the register |
| Latch high, mask clearing | lhmk | Latch high signal at high level, register cleared with written mask | SW can read the register, with write mask the register can be cleared (1 clears) |

**Table 12    Register Access Types** (cont'd)

| Mode | Symbol | Description HW | Description SW |
|---|---|---|---|
| Latch low, mask clearing | llmk | Latch high signal at low-level, register cleared on read | SW can read the register, with write mask the register can be cleared (1 clears) |
| Interrupt high, self clearing | ihsc | Differentiate the input signal (low->high) register cleared on read | SW can read the register |
| Interrupt low, self clearing | ilsc | Differentiate the input signal (high->low) register cleared on read | SW can read the register |
| Interrupt high, mask clearing | ihmk | Differentiate the input signal (high->low) register cleared with written mask | SW can read the register, with write mask the register can be cleared |
| Interrupt low, mask clearing | ilmk | Differentiate the input signal (low->high) register cleared with written mask | SW can read the register, with write mask the register can be cleared |
| Interrupt enable register | ien | Enables the interrupt source for interrupt generation | SW can read and write this register |
| latch_on_reset | lor | rw register, value is latched after first clock cycle after reset | Register is read and writable by SW |
| Read/write self clearing | rwsc | Register is used as input for the hw, the register will be cleared due to a HW mechanism. | Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW. |

**Table 13    Registers Clock Domains**

| Clock Short Name | Description |
|---|---|
| – | – |

## 4.1.1    EEPROM Register Descriptions

**Signature Register**

Description

| **SigReg** | **Offset** | **Reset Value** |
|---|---|---|
| **Signature Register** | **00$_H$** | **4154$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Signature | | | | | | | | |

ro
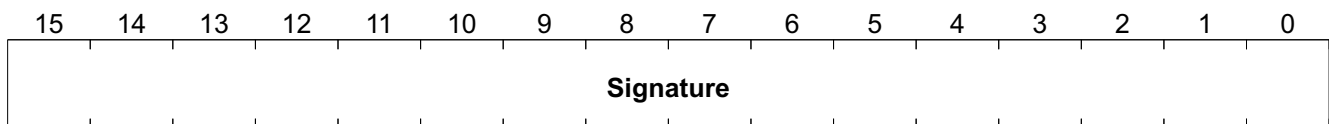
| Field | Bits | Type | Description |
|---|---|---|---|
| Signature | 15:0 | ro | **Signature** <br> 4154$_H$    **SigReg** Obligatory value (AT) |

*Note: ADM6996LC/LCX/LHX will check register 0 value before read all EEPROM content. If this value not match with 0x4154h then other values in EEPROM will be useless. ADM6996LC/LCX/LHX will use internal default value. User cannot write Signature register when programming ADM6996LC/LCX/LHX internal register.*

**Basic Control Register 0**

Used to configure chip settings

| CtrlReg_0 | Offset | Reset Value |
|---|---|---|
| Basic Control Register 0 | $01_H$ | $040F_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CAM | FSE | | PV | | | | PP | PPE | TV | PD | OT | DUP | OPS | AN | FC |
| rw | rw | | rw | | | | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| CAM | 15 | rw | **Crossover Auto MDIX**<br>$0_B$ **D** Disable<br>    *Note: Hardware Reset latch value EESK can be set globally using the Auto MDIX function.*<br>$1_B$ **E** Enable |
| FSE | 14 | rw | **Fx Select Enable**<br>$0_B$ **TP** Tp Mode<br>    *Note: If this bit has been set to Fx in hardware then the bit does not have the power to change from Fx to Tp*<br>$1_B$ **FX** Fx Mode |
| PV | 13 :10 | rw | **Port VLAN ID** |
| PP | 9:8 | rw | **Port Based Priority** |
| PPE | 7 | rw | **Port Based Priority Enable**<br>$0_B$ **VTE** VLAN or TOS Priority Enable<br>    *Note: This bit is default $0_B$ to enable VLAN or TOS priority check. If user would like to check the VLAN priority, Tag mode should be enabled.*<br>$1_B$ **PBE** Port Based Priority Enable<br>    *Note: If this bit is set to $1_B$, only port based priority will be checked.* |
| TV | 6 | rw | **TOS over VLAN priority**<br>$0_B$ **V** VLAN Enable<br>$1_B$ **T** TOS Enable |
| PD | 5 | rw | **Port Disable**<br>$0_B$ **E** Enable<br>$1_B$ **D** Disable |
| OT | 4 | rw | **Output Packet Tagging**<br>$0_B$ **U** Un-tag<br>$1_B$ **T** Tag |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| DUP | 3 | rw | **Duplex Enable**<br>$0_B$ **H** Half<br>$1_B$ **F** Full |
| OPS | 2 | rw | **Operating Speed**<br>$0_B$ **10** 10 Mbit/s<br>$1_B$ **100** 100 Mbit/s |
| AN | 1 | rw | **Auto-negotiation**<br>$0_B$ **D** Disable<br>$1_B$ **E** Enable |
| FC | 0 | rw | **802.x Flow Control Command**<br>$0_B$ **D** Disable<br>$1_B$ **E** Enable |

**Similar Registers**

**Table 14    Basic Control Registers 1 to 4**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|----------------|-------------|
| CtrlReg_P1 | Basic Control Register 1 | $03_H$ | |
| CtrlReg_P2 | Basic Control Register 2 | $05_H$ | |
| CtrlReg_P3 | Basic Control Register 3 | $07_H$ | |
| CtrlReg_P4 | Basic Control Register 4 | $08_H$ | |

**Reserved Register 0**

Register reserved for future use

| **ResReg_0** | **Offset** | **Reset Value** |
|---|---|---|
| **Reserved Register 0** | $02_H$ | $040F_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Res | | | | | | | | |

ro
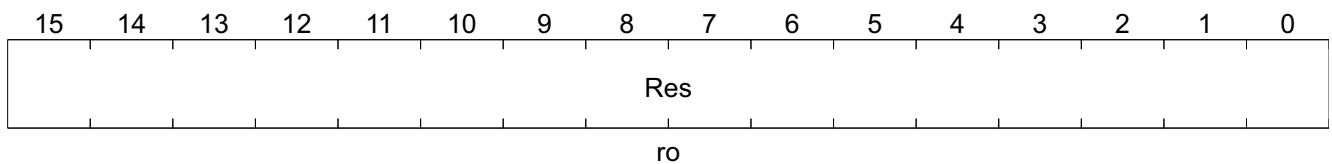
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:0 | ro | **Reserved** |

**Similar Registers**

**Table 15    Reserved Register 1 to 3**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|----------------|-------------|
| ResReg_1 | Reserved Register 1 | $04_H$ | |
| ResReg_2 | Reserved Register 2 | $06_H$ | |
| ResReg_3 | Reserved Register 3 | $09_H$ | |

## Reserved Register 4

Register reserved for future use

| **ResReg_4** | **Offset** | **Reset Value** |
|---|---|---|
| **Reserved Register 4** | **0A$_H$** | **5902$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | | Res | | | IDR | | | | | Res | | | | |
| | | | ro | | | rw | | | | | ro | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15:10 | ro | **Reserved** |
| IDR | 9 | rw | **Replace Packet ID** <br> 0$_B$ **N** Not replaced <br> 1$_B$ **Y** Replaced with 1 by PVID |
| Res | 8:0 | ro | **Reserved** |
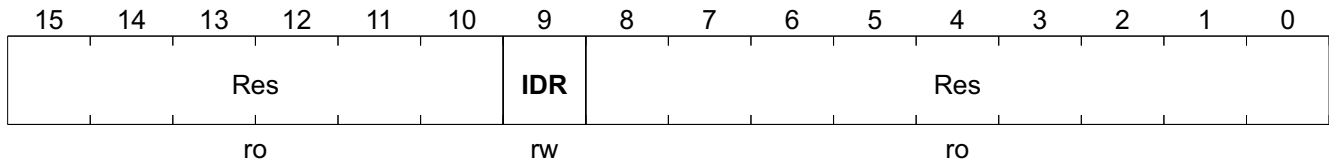
## Configuration Register 1

Used to configure the chip
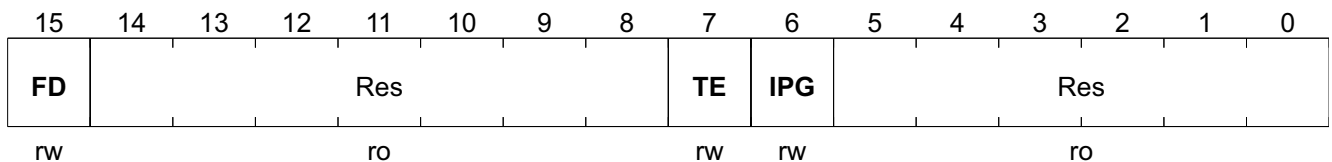
| **ConfigReg_1** | **Offset** | **Reset Value** |
|---|---|---|
| **Configuration Register 1** | **0B$_H$** | **8000$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| FD | | | | Res | | | | TE | IPG | | | Res | | | |
| rw | | | | ro | | | | rw | rw | | | ro | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| FD | 15 | rw | **Far End Fault Detection** <br> 0$_B$ **D** Disable <br> 1$_B$ **E** Enable |
| Res | 14:8 | ro | **Reserved** |
| TE | 7 | rw | **Trunk Enable** <br> 0$_B$ **D** Disable Port 3 and 4 <br> 1$_B$ **E** Enable Port 3 and 4 |
| IPG | 6 | rw | **Inter Packet Gap Setting** <br> 0$_B$ **96B** 96 bits <br> 1$_B$ **92B** 92 bits |
| Res | 5:0 | ro | **Reserved** |

## Reserved Register 5

Reserved for future use

| ResReg_5 | Offset | Reset Value |
|---|---|---|
| Reserved Register 5 | 0C$_H$ | FA50$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Res | | | | | | | | |
| | | | | | | | ro | | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15:0 | ro | **Reserved** |
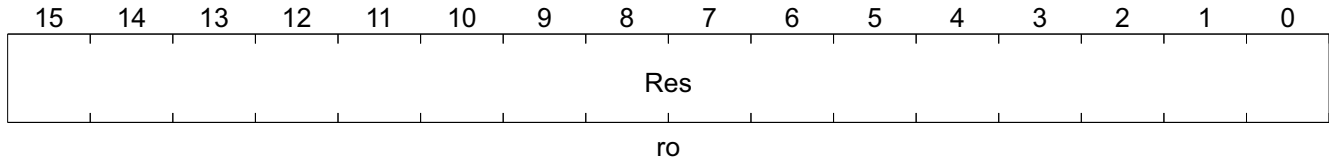
**Similar Registers**

**Table 16    Reserved Register 6**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| ResReg_6 | Reserved Register 6 | 0D$_H$ | |

**VLAN Priority Map Register**

Sets the VLAN priorities
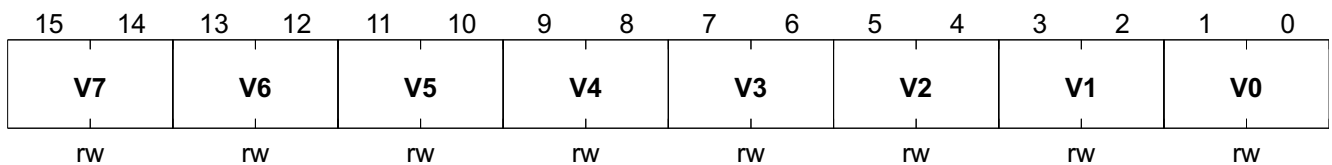
| VLAN_Map_P | Offset | Reset Value |
|---|---|---|
| VLAN priority Map Register | 0E$_H$ | 5500$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **V7** | | **V6** | | **V5** | | **V4** | | **V3** | | **V2** | | **V1** | | **V0** | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| V7 | 15:14 | rw | **Mapped priority of tag value (VLAN)** |
| V6 | 13:12 | rw | |
| V5 | 11:10 | rw | |
| V4 | 9:8 | rw | |
| V3 | 7:6 | rw | |
| V2 | 5:4 | rw | |
| V1 | 3:2 | rw | |
| V0 | 1:0 | rw | |

*Note: Value 3 ~ 0 are for priority queue Q3~Q0 respectively.The Weight ratio is Q3: Q2: Q1: Q0 = 8: 4: 2: 1. The default is port-base priority for un-tagged packets and non_IP frame.*

## Type of Service (TOS) Priority Map Register

Sets TOS priority

| **TOS_Priority** | **Offset** | **Reset Value** |
|---|---|---|
| **TOS priority Map Register** | **0F$_H$** | **5500$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **T7** | | **T6** | | **T5** | | **T4** | | **T3** | | **T2** | | **T1** | | **T0** | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| T7 | 15:14 | rw | **Mapped priority of tag value (TOS)** |
| T6 | 13:12 | rw | |
| T5 | 11:10 | rw | |
| T4 | 9:8 | rw | |
| T3 | 7:6 | rw | |
| T2 | 5:4 | rw | |
| T1 | 3:2 | rw | |
| T0 | 1:0 | rw | |

*Note: Value 3 ~ 0 are for priority queues Q3~Q0 respectively. The Weight ratio is Q3: Q2: Q1: Q0 = 8: 4: 2: 1. The default is port-based priority for un-tagged packets and non_IP frames.*

## Configuration Register 2

Used to configure the chip

| **ConfigReg_2** | **Offset** | **Reset Value** |
|---|---|---|
| **Configuration Register 2** | **10$_H$** | **0040$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Q3** | | **Q2** | | **Q1** | | **Q0** | | **AGE** | **Res** | | **XC** | **Res** | **SF** | **ST** | |
| rw | | rw | | rw | | rw | | rw | ro | | rw | rw | rw | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| Q3 | 15:14 | rw | **Discard mode** |
| Q2 | 13:12 | rw | Drop scheme for Queue n. See **Table 19** for details on the drop scheme of each queue |
| Q1 | 11:10 | rw | |
| Q0 | 9:8 | rw | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| AGE | 7 | rw | **Aging Status**<br>$0_B$   **E** Enable<br>$1_B$   **D** Disable |
| Res | 6:5 | ro | **Reserved** |
| XC | 4 | rw | **CRC Check**<br>$0_B$   **E** Enable CRC check<br>$1_B$   **D** Disable CRC check |
| Res | 3 | rw | **Reserved** |
| SF | 2 | rw | **Broadcast Storm Filter**<br>$0_B$   **D** Disable<br>$1_B$   **E** Enable |
| ST | 1:0 | rw | **Broadcast Storm Threshold**<br>See below **Table 17** and **Table 18** for details on the Broadcast Storm Threshold |

*Note: Broadcast storm initial time interval = 50ms. The max. packet number = 7490 in 100Base, 749 in 10Base*

**Table 17**     **The max. packet number = 7490 in 100Base, 749 in 10Base**

**Per Port Rising Threshold**

| | $00_B$ | $01_B$ | $10_B$ | $11_B$ |
|---|--------|--------|--------|--------|
| All 100TX | Disable | 14880fps | 29760fps | 59520fps |
| Not All 100TX | Disable | 1488fps | 2976fps | 5952fps |

**Table 18**     **The max. packet number = 7490 in 100Base, 749 in 10Base**

**Per Port Falling Threshold**

| | $00_B$ | $01_B$ | $10_B$ | $11_B$ |
|---|--------|--------|--------|--------|
| All 100TX | Disable | 7440fps | 14880fps | 29760fps |
| Not All 100TX | Disable | 744fps | 1488fps | 2976fps |

**Table 19**     **Drop Scheme for Each Queue**

| Discard Mode Utilization | 00 | 01 | 10 | 11 |
|---|----|----|----|----|
| TBD | 0% | 0% | 25% | 50% |

**VLAN mode select Register**

Selects VLAN Mode

| VLAN_Mode | Offset | Reset Value |
|-----------|--------|-------------|
| VLAN Mode Select Register | $11_H$ | $FF00_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | Res | | | | | VM | MAC | | | Res | |
| | | | | | ro | | | | | rw | rw | | | ro | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:6 | ro | **Reserved** |
| VM | 5 | rw | **VLAN Mode Select**<br>$0_B$ **P** Port based by-pass mode<br>$1_B$ **Q** 802.1Q based |
| MAC | 4 | rw | **MAC Clone Enable**<br>$0_B$ **N** Normal Mode.Learning with SA only. The MAC table will be searched or filled using only SA or DA.<br>$1_B$ **M** Mac Mode. Learned using SA VID0. MAC table will be searched or filled using VID0 SA or DA. This bit allows two identical addresses with different VID0 to be learned. |
| Res | 3:0 | ro | **Reserved** |

*Note:*

**Below is an example of a VLAN Tag and a MAC application for Bit4 and Bit5.**

Below is an old router architecture example. The disadvantages of this are:

1. WAN port only supports 10M Half-Duplex and non-MDIX functions
2. Needs extra 10M NIC cost.
3. ISA bus will become a bottleneck for the whole system
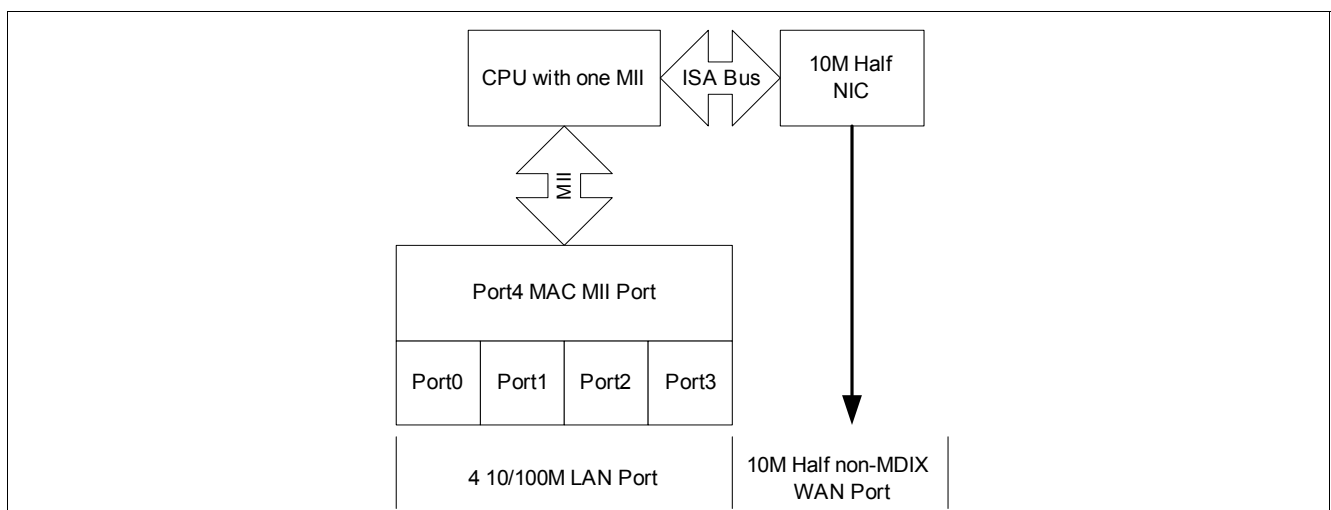


**Figure 8    Old Router Architecture Example**

Below is new architecture by using ADM6996LC/LCX/LHX serial chip VLAN function. The advantages of below are:

1. WAN Port can upgrade to 100/10 Full/Half, Auto MDIX.
2. WAN/LAN Port is programmable and put on same Switch.

3. No need extra NIC and save lot of cost.
4. High bandwidth of MII port up to 200M speed.
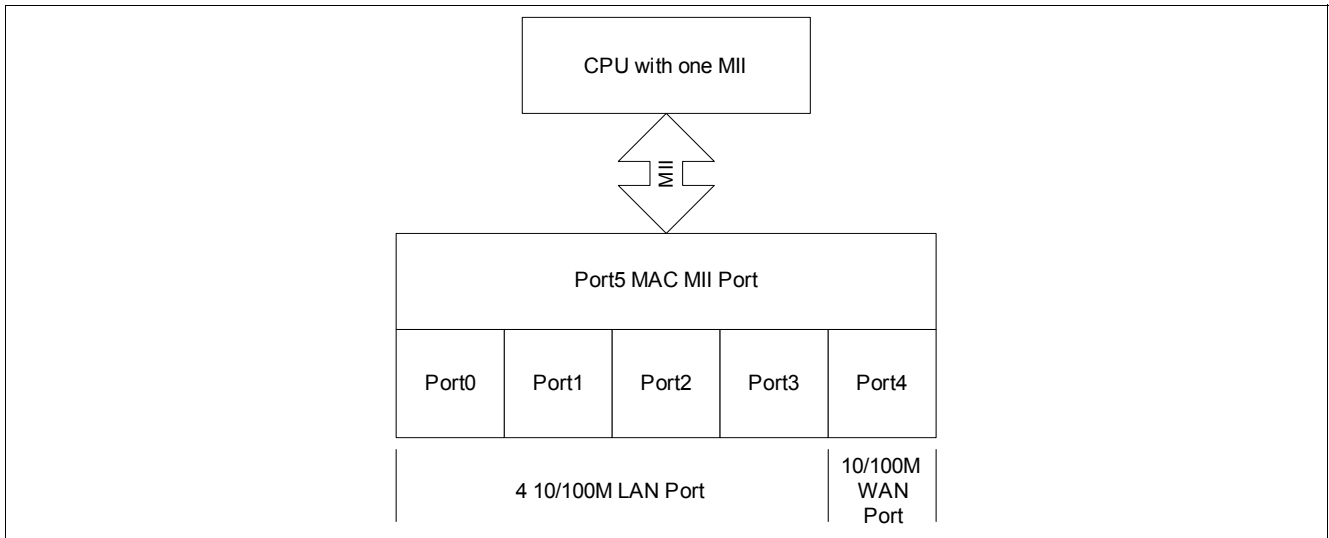


**Figure 9    New Router Architecture using ADM6996LC/LCX/LHX**

New Router application works well on normal application. If user's ISP vendor(cable modem) lock Registration Card's ID then Router CPU must send this Lock Registration Card's ID to WAN Port. One condition happen is there exist two same MAC ID on this Switch. One is original Card and another one is CPU. This will make Switch learning table trouble.

ADM6996LC/LCX/LHX provide MAC Clone function that allow two same MAC address with different VLAN ID0 on learning table. This will solve Lock registration Card's ID issue. ADM6996 series chip will put these two same MAC addresses with different VLAN ID0 at different learning table entry.

**How to Set ADM6996LC/LCX/LHX on Router**

Port0~3: LAN Port.

Port4: WAN Port.

Port5: MII Port as CPU Port.

Step1: Set Register 0x11h bit4 and bit5 to 1.

{Coding: Write Register 0x11h as 0xff30h}

Step2: Set Port0~3 as Untag Port and set PVID=1.

{Coding: Write Register 0x01h, 0x03h, 0x05h, 0x07h as 0x840f. Port0~3 as Untag, PVID=1, Enable MDIX}

Step3: Set Port4 as Untag Port and set PVID=2.

{Coding:Write Register 0x08h as 0x880fh. Port4 as Untag, PVID=2, Enable MDIX.}

Step4: Set Port5 MII Port as Tag Port and set PVID=2.

{Coding:Write Register 0x09h as 0x881fh. Port5 MII port as Tag, PVID=2.}

Step5: Group Port0, 1, 2, 3, 5 as VLAN 1.

{Coding: Write Register 0x14h as 0x0155h. VLAN1 cover Port0, 1, 2, 3, 5.}

Step6: Group Port4, 5 as VLAN 2.

{Coding: Write Register 0x15h as 0x0180h. VLAN2 cover Port4, 5.}

**How MAC Clone Operation**

• LAN to LAN/CPU Traffic.

ADM6996LC/LCX/LHX LAN traffic to LAN/CPU only. Traffic to another LAN port will be

untag packet. Traffic to CPU is Tag packet with VID=1. CPU can check VID to
distinguish LAN traffic or WAN traffic.

• WAN to CPU Traffic.

ADM6996LC/LCX/LHX WAN traffic to CPU only. Traffic to CPU is Tag packet with VID=2.
CPU can check VID to distinguish LAN traffic or WAN traffic.

• CPU to LAN Packet.

ADM6996LC/LCX/LHX CPU Packet to LAN port must add VID=1 in VLAN field.

ADM6996LC/LCX/LHX check VID to distinguish LAN traffic or WAN traffic. LAN output
packet is Untag.

• CPU to WAN Packet.

ADM6996LC/LCX/LHX CPU Packet to WAN port must add VID=2 in VLAN filed.

ADM6996LC/LCX/LHX check VID to distinguish LAN traffic or WAN traffic. WAN output
packet is Untag.

• ADM6996LC/LCX/LHX learning sequence

ADM6996LC/LCX/LHX will check VLAN mapping setting first then check learning table.

User does not worry LAN/WAN traffic mix up.

Bit 10: Half Duplex Back Pressure enable. 1/enable, 0/disable.

**Configuration Register 3**

**ConfigReg_3**          **Offset**          **Reset Value**
**Miscellaneous Configuration Register 3**       $12_H$          $3600_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CD | DCS | | | Res | | | ML5 | ML4 | ML3 | Res | ML2 | Res | ML1 | Res | ML0 |
| rw | rw | | | rw | | | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| CD | 15 | rw | **Excessive Collision Drop** <br> $0_B$   **D** Disable <br> $1_B$   **E** Enable |
| DCS | 14 | rw | **Duplex and Col Separate** <br> $0_B$   **D** Indicate the duplex and collision status at the same time <br> $1_B$   **LM** Indicate the duplex status only |
| Res | 13:9 | rw | **Reserved** |
| ML5 | 8 | rw | **Port5 MAC Lock** <br> $0_B$   **D** Disable <br> $1_B$   **LM** Lock first MAC Source Address |
| ML4 | 7 | rw | **Port4 MAC Lock** <br> $0_B$   **D** Disable <br> $1_B$   **LM** Lock first MAC Source Address |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| ML3 | 6 | rw | **Port3 MAC Lock**<br>$0_B$ **D** Disable<br>$1_B$ **LM** Lock first MAC Source Address |
| Res | 5 | rw | **Reserved** |
| ML2 | 4 | rw | **Port 2 MAC Lock**<br>$0_B$ **D** Disable<br>$1_B$ **LM** Lock first MAC source address |
| Res | 3 | rw | **Reserved** |
| ML1 | 2 | rw | **Port1 MAC Lock**<br>$0_B$ **D** Disable<br>$1_B$ **LM** Lock first MAC source address |
| Res | 1 | rw | **Reserved** |
| ML0 | 0 | rw | **Port0 MAC Lock**<br>$0_B$ **D** Disable<br>$1_B$ **LM** Lock first MAC source address |

**VLAN Mapping Table Registers 0**

| VLAN_Map_0 | Offset | Reset Value |
|---|---|---|
| VLAN mapping table registers 0 | $13_H$ | $FFFF_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | Res | | | | VM5 | VM4 | VM3 | Res | VM2 | Res | VM1 | Res | VM0 |
| | | | ro | | | | rw | rw | rw | ro | rw | ro | rw | ro | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:9 | ro | **Reserved** |
| VM5 | 8 | rw | **Port 5 VLAN Mapping**<br>$0_B$ **NM** Port 5 is not the member of the VLAN.<br>$1_B$ **M** Port 5 is the member of the VLAN. |
| VM4 | 7 | rw | **Port 4 VLAN Mapping**<br>$0_B$ **NM** Port 4 is not the member of the VLAN.<br>$1_B$ **M** Port 4 is the member of the VLAN. |
| VM3 | 6 | rw | **Port 3 VLAN Mapping**<br>$0_B$ **NM** Port 3 is not the member of the VLAN.<br>$1_B$ **M** Port 3 is the member of the VLAN. |
| Res | 5 | ro | **Reserved** |
| VM2 | 4 | rw | **Port 2 VLAN Mapping**<br>$0_B$ **NM** Port 2 is not the member of the VLAN.<br>$1_B$ **M** Port 2 is the member of the VLAN. |
| Res | 3 | ro | **Reserved** |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| VM1 | 2 | rw | **Port 1 VLAN Mapping**<br>$0_B$ **NM** Port 1 is not the member of the VLAN.<br>$1_B$ **M** Port 1 is the member of the VLAN. |
| Res | 1 | ro | **Reserved** |
| VM0 | 0 | rw | **Port 0 VLAN Mapping**<br>$0_B$ **NM** Port 0 is not the member of the VLAN.<br>$1_B$ **M** Port 0 is the member of the VLAN. |
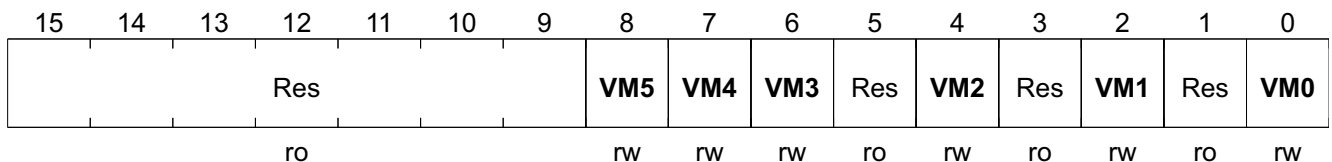
*Note: 16 VLAN Group: See Register 0x2ch bit 11. Select the VLAN group ports and set the corresponding bits to 1.*

**Similar Registers**

**Table 20    VLAN Mapping Table Registers 1 to 15**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|----------------|-------------|
| VLAN_Map_1 | VLAN mapping table registers 1 | $14_H$ | |
| VLAN_Map_2 | VLAN mapping table registers 2 | $15_H$ | |
| VLAN_Map_3 | VLAN mapping table registers 3 | $16_H$ | |
| VLAN_Map_4 | VLAN mapping table registers 4 | $17_H$ | |
| VLAN_Map_5 | VLAN mapping table registers 5 | $18_H$ | |
| VLAN_Map_6 | VLAN mapping table registers 6 | $19_H$ | |
| VLAN_Map_7 | VLAN mapping table registers 7 | $1A_H$ | |
| VLAN_Map_8 | VLAN mapping table registers 8 | $1B_H$ | |
| VLAN_Map_9 | VLAN mapping table registers 9 | $1C_H$ | |
| VLAN_Map_10 | VLAN mapping table registers 10 | $1D_H$ | |
| VLAN_Map_11 | VLAN mapping table registers 11 | $1E_H$ | |
| VLAN_Map_12 | VLAN mapping table registers 12 | $1F_H$ | |
| VLAN_Map_13 | VLAN mapping table registers 13 | $20_H$ | |
| VLAN_Map_14 | VLAN mapping table registers 14 | $21_H$ | |
| VLAN_Map_15 | VLAN mapping table registers 15 | $22_H$ | |

**Reserved Register 7**
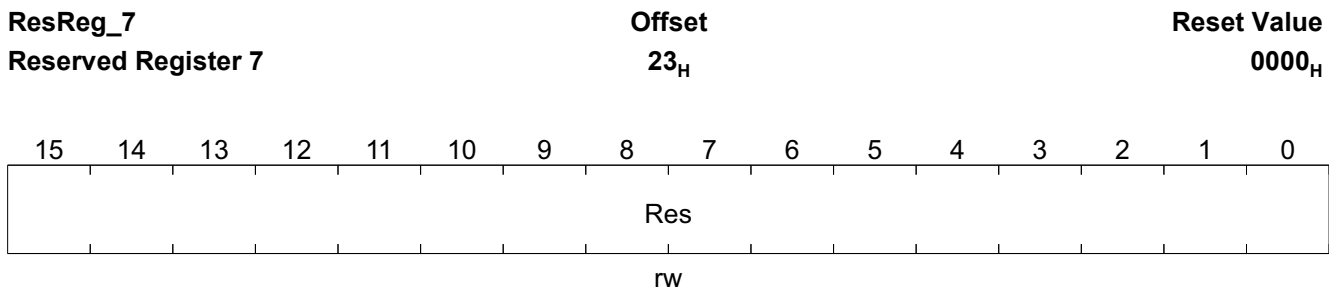
| ResReg_7 | Offset | Reset Value |
|----------|--------|-------------|
| Reserved Register 7 | $23_H$ | $0000_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Res | | | | | | | |
| | | | | | | | | rw | | | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:0 | rw | **Reserved** |

**Similar Registers**

**Table 21    Reserved Register 8 to 11**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|---------------------|----------------|-------------|
| ResReg_8 | Reserved Register 8 | 24$_H$ | |
| ResReg_9 | Reserved Register 9 | 25$_H$ | |
| ResReg_10 | Reserved Register 10 | 26$_H$ | |
| ResReg_11 | Reserved Register 11 | 27$_H$ | |

**Configuration Register 4**
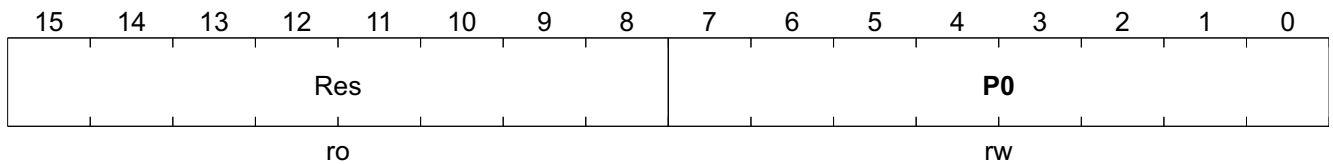
| ConfigReg_4 | Offset | Reset Value |
|---|---|---|
| **Configuration Register 4** | **28**$_H$ | **0000**$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | | | Res | | | | | | | | P0 | | | |
| | | | | ro | | | | | | | | rw | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:8 | ro | **Reserved** |
| P0 | 7:0 | rw | **Port 0 PVID** <br> 0001$_H$    **PVID** These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID. |

**Configuration Register 5**
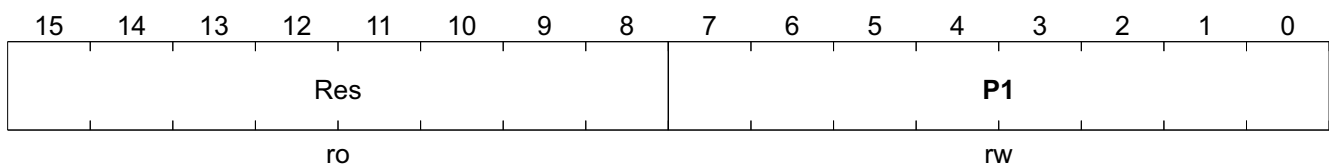
| ConfigReg_5 | Offset | Reset Value |
|---|---|---|
| **Configuration Register 5** | **29**$_H$ | **0000**$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | | | Res | | | | | | | | P1 | | | |
| | | | | ro | | | | | | | | rw | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:8 | ro | **Reserved** |

| Field | Bits | Type | Description |
|---|---|---|---|
| P1 | 7:0 | rw | **Port1 PVID bit 11~4.**<br>$0003_H$ **PVID 1** These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID. |

**Configuration Register 6**

**ConfigReg_6**        **Offset**        **Reset Value**
**Configuration Register 6**        $2A_H$        $0000_H$
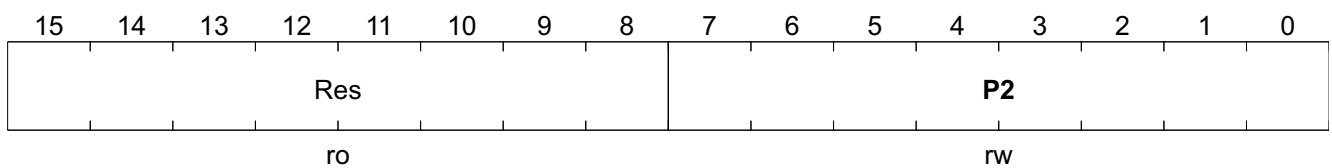
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Res | | | | | | | | P2 | | | | |
| | | | ro | | | | | | | | rw | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15:8 | ro | **Reserved** |
| P2 | 7:0 | rw | **Port2 PVID bit 11~4.**<br>$0005_H$ **PVID 2** These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID. |

**Configuration Register 7**

**ConfigReg_7**        **Offset**        **Reset Value**
**Configuration Register 7**        $2B_H$        $0000_H$
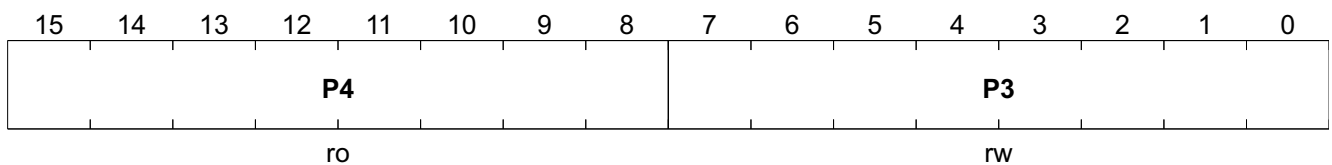
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | P4 | | | | | | | | P3 | | | | |
| | | | ro | | | | | | | | rw | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| P4 | 15:8 | ro | **Port4 PVID bit 11~4.**<br>$0008_H$ **PVID 1** These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID. |
| P3 | 7:0 | rw | **Port3 PVID bit 11~4.**<br>$0007_H$ **PVID 1** These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID. |

**Configuration Register 8**

**ConfigReg_8**              **Offset**                    **Reset Value**
**Configuration Register**        **2C**$_H$                      **D000**$_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CR0 | CR1 | CR2 | CR3 | Res | | VS | | | | | P5 | | | | |
| rw | rw | rw | rw | rw | | rw | | | | | rw | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| CR0 | 15 | rw | **Control Reserved MAC** <br> Control reserved MAC (0180C2000000) <br> 0$_B$ **D** Discard <br> 1$_B$ **F** Forward |
| CR1 | 14 | rw | **Control Reserved MAC** <br> Control reserved MAC (0180C2000001) <br> 0$_B$ **D** Discard <br> 1$_B$ **F** Forward |
| CR2 | 13 | rw | **Control Reserved MAC** <br> Control reserved MAC (0180C2000002- 0180C200000F) <br> 0$_B$ **D** Discard <br> 1$_B$ **F** Forward |
| CR3 | 12 | rw | **Control Reserved MAC** <br> Control reserved MAC (0180C2000010-0180C20000FF) <br> 0$_B$ **D** Discard <br> 1$_B$ **F** Forward |
| Res | 11 | rw | **Reserved** |
| VS | 10:8 | rw | **VLAN Grouping Tag Shift** <br> 0$_D$ **VID0** VID [3:0] <br> 1$_D$ **VID1** VID [4:1] <br> 2$_D$ **VID2** VID [5:2] <br> 3$_D$ **VID3** VID [6:3] <br> 4$_D$ **VID4** VID [7:4] <br> 5$_D$ **VID5** VID [8:5] <br> 6$_D$ **VID6** VID [9:6] <br> 7$_D$ **VID7** VID [10:7] |
| P5 | 7:0 | rw | **Port5 PVID bit 11~4.** <br> 0009$_H$  **PVID 1** These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID. |

*Note: Bit[10:8]: VLAN Tag shift register. ADM6996LC/LCX/LHX will select 4 bit form total 12 bit VID as VLAN group reference. Bit[15:12]: IEEE 802.3 reserved DA forward or drop police.*

**Reserved Register 12**

**ResReg_12**        **Offset**        **Reset Value**
**Reserved Register 12**        **2D$_H$**        **4442$_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Res | | | | | | | | |

rw
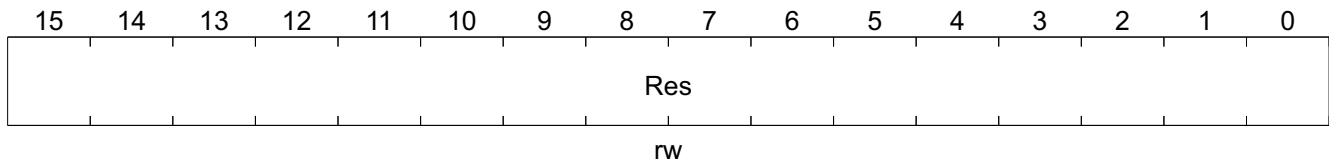
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:0 | rw | **Reserved** |

**Reserved Register 13**

**ResReg_13**        **Offset**        **Reset Value**
**Reserved Register 13**        **2E$_H$**        **0000$_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Res | | | | | | | | |

rw
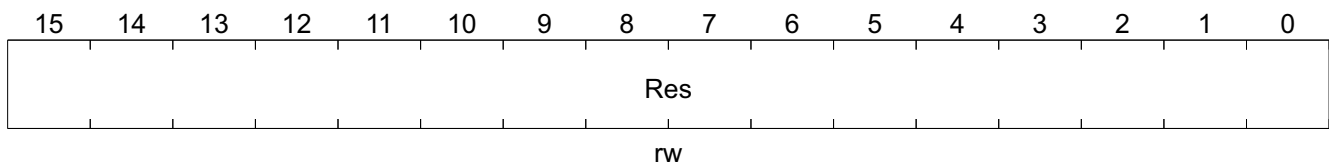
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:0 | rw | **Reserved** |

**PHY Restart**

**PH_Restart**        **Offset**        **Reset Value**
**PHY Restart**        **2F$_H$**        **0000$_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **PR** | | | | | | | | |

rw
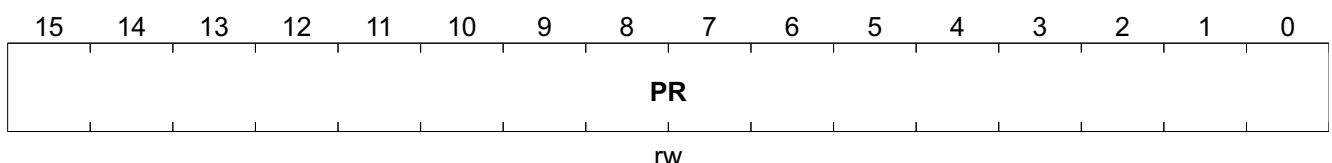
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| PR | 15:0 | rw | **PHY Restart** 0000$_H$ **PHY Restart** Writing this Hex value to this register restarts the internal PHYs. |

**Configuration Register 9**

| ConfigReg_ | Offset | Reset Value |
|---|---|---|
| **Miscellaneous Configuration Register 9** | **30**$_H$ | **0987**$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | Res | | **LM** | Res | Res | **DHCOL** | | Res | **RCL** | **MAC** | | | Res | | |
| | rw | | rw | rw | rw | rw | | rw | rw | rw | | | rw | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:13 | rw | **Reserved** |
| LM | 12 | rw | **Port 4 LED Mode**<br>0$_B$   **D** LinkAct/DupCol/Speed<br>1$_B$   **S** LinkAct/Speed |
| Res | 11 | rw | **Reserved** |
| Res | 10 | rw | **Reserved** |
| DHCOL | 9 | rw | **Dual Speed Hub COL_LED Enable**<br>0$_B$   **N** Normal LED display.<br>1$_B$   **D** Dual Speed Hub LED display. Port0 Col LED: 10M Col LED.<br>      Port1 Col LED: 100M Col LED. |
| Res | 8:7 | rw | **Reserved** |
| RCL | 6 | rw | **MII Speed Double**<br>0$_B$   **25** TxCLK max speed is 25 MHz<br>1$_B$   **50** TxCLK max speed is 50 MHz |
| MAC | 5 | rw | **Mac Clone Enable**<br>MAC Clone Enable Bit[1]. |
| Res | 4:0 | rw | **Reserved** |

**Bandwidth Control Register**

| BWCon_0 | Offset | Reset Value |
|---|---|---|
| **Bandwidth Control Register 0** | **31**$_H$ | **0000**$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| **RC3** | | **P3T** | | **RC2** | | **P2T** | | **RC1** | | **P1T** | | **RC0** | | **P0T** | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| RC3 | 15 | rw | **Receive Packet Length Count** <br> Counted on the Source Port 3. <br> $0_D$ **R3** The switch will add length to the P3 counter |
| P3T | 14:12 | rw | **Port 3 Threshold Control Meter** <br> Reference **Table 22** in note below. |
| RC2 | 11 | rw | **Receive Packet Length Count** <br> Counted on the Source Port 2. <br> $0_D$ **R2** The switch will add length to the P2 counter |
| P2T | 10:8 | rw | **Port 2 Threshold Control Meter** <br> Reference **Table 22** in note below. |
| RC1 | 7 | rw | **Receive Packet Length Count** <br> Counted on the Source Port 1. <br> $0_D$ **R1** The switch will add length to the P1 counter |
| P1T | 6:4 | rw | **Port 1 Threshold Control Meter** <br> Reference **Table 22** in note below. |
| RC0 | 3 | rw | **Receive Packet Length Count** <br> Counted on the Source Port 0. <br> $0_D$ **R0** The switch will add length to the P2 counter |
| P0T | 2:0 | rw | **Port 0 Threshold Control Meter** <br> Reference **Table 22** in note below. |

**Table 22    Note: Reference Table**

| 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| 256K | 512K | 1M | 2M | 5M | 10M | 20M | 50M |

**Bandwidth Control Register 1**
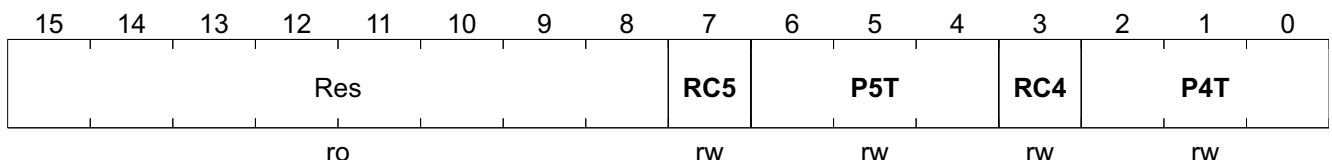
| **BWCon_1** | **Offset** | **Reset Value** |
|-------------|------------|-----------------|
| **Bandwidth Control Register 1** | **$32_H$** | **$0000_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | Res | | | | | RC5 | | P5T | | RC4 | | P4T | |
| | | | ro | | | | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:8 | ro | **Reserved** |
| RC5 | 7 | rw | **Receive Packet Length Count** <br> Counted on the Source Port 5. <br> $0_D$ **Count5** The switch will add length to the P5 counter |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| P5T | 6:4 | rw | **Port 5 Threshold Control Meter**<br>Reference **Table 22** in note below. |
| RC4 | 3 | rw | **Receive Packet Length Count**<br>Counted on the Source Port 4.<br>$0_D$ **Count4** The switch will add length to the P4 counter |
| P4T | 2:0 | rw | **Port 4 Threshold Control Meter**<br>Reference **Table 22** in note below. |

**Bandwidth Control Enable Register**

**BWConEn**  **Offset**  **Reset Value**
**Bandwidth Control Enable Register**  $33_H$  $0000_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | Res | | | | BW5 | BW4 | BW3 | Res | BW2 | Res | BW1 | Res | BW0 |
| | | | ro | | | | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:9 | ro | **Reserved** |
| BW5 | 8 | rw | **Port 5 Bandwidth Control Enable**<br>$0_B$ **D** Disable<br>$1_B$ **E** Enable |
| BW4 | 7 | rw | **Port 4 Bandwidth Control Enable**<br>$0_B$ **D** Disable<br>$1_B$ **E** Enable |
| BW3 | 6 | rw | **Port 3 Bandwidth Control Enable**<br>$0_B$ **D** Disable<br>$1_B$ **E** Enable |
| Res | 5 | rw | **Reserved** |
| BW2 | 4 | rw | **Port 2 Bandwidth Control Enable**<br>$0_B$ **D** Disable<br>$1_B$ **E** Enable |
| Res | 3 | rw | **Reserved** |
| BW1 | 2 | rw | **Port 1 Bandwidth Control Enable**<br>$0_B$ **D** Disable<br>$1_B$ **E** Enable |
| Res | 1 | rw | **Reserved** |
| BW0 | 0 | rw | **Port 0 Bandwidth Control Enable**<br>$0_B$ **D** Disable<br>$1_B$ **E** Enable |

## 4.2        Serial Registers

**Table 23     Registers Address Space**

| Module | Base Address | End Address | Note |
|---|---|---|---|
| Serial Registers | $00_H$ | $3C_H$ | Independent Address Space |

**Table 24     Registers Overview**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| **ChipID** | Chip Identifier Register | $00_H$ | **63** |
| **PortStat_0** | Port Status Register 0 | $01_H$ | **63** |
| **PortStat_1** | Port Status Register 1 | $02_H$ | **65** |
| **CabStat** | Cable Broken Status | $03_H$ | **66** |
| **P0_RP_CNT** | Port 0 Receive Packet Count | $04_H$ | **66** |
| P1_RP_CNT | Port 1 Receive Packet Count | $06_H$ | **67** |
| P2_RP_CNT | Port 2 Receive Packet Count | $08_H$ | **67** |
| P3_RP_CNT | Port 3 Receive Packet Count | $0A_H$ | **67** |
| P4_RP_CNT | Port 4 Receive Packet Count | $0B_H$ | **67** |
| P5_RP_CNT | Port 5 Receive Packet Count | $0C_H$ | **67** |
| P0_RB_CNT | Port 0 Receive Byte Count | $0D_H$ | **67** |
| P1_RB_CNT | Port 1 Receive Byte Count | $0F_H$ | **67** |
| P2_RB_CNT | Port 2 Receive Byte Count | $11_H$ | **67** |
| P3_RB_CNT | Port 3 Receive Byte Count | $13_H$ | **67** |
| P4_RB_CNT | Port 4 Receive Byte Count | $14_H$ | **67** |
| P5_RB_CNT | Port 5 Receive Byte Count | $15_H$ | **67** |
| P0_TP_CNT | Port 0 Transmit Packet Count | $16_H$ | **67** |
| P1_TP_CNT | Port 1 Transmit Packet Count | $18_H$ | **67** |
| P2_TP_CNT | Port 2 Transmit Packet Count | $1A_H$ | **67** |
| P3_TP_CNT | Port 3 Transmit Packet Count | $1C_H$ | **67** |
| P4_TP_CNT | Port 4 Transmit Packet Count | $1D_H$ | **67** |
| P5_TP_CNT | Port 5 Transmit Packet Count | $1E_H$ | **67** |
| P0_TB_CNT | Port 0 Transmit Byte Count | $1F_H$ | **67** |
| P1_TB_CNT | Port 1 Transmit Byte Count | $21_H$ | **67** |
| P2_TB_CNT | Port 2 Transmit Byte Count | $23_H$ | **67** |
| P3_TB_CNT | Port 3 Transmit Byte Count | $25_H$ | **67** |
| P4_TB_CNT | Port 4 Transmit Byte Count | $26_H$ | **67** |
| P5_TB_CNT | Port 5 Transmit Byte Count | $27_H$ | **67** |
| P0_COL_CNT | Port 0 Collision Count | $28_H$ | **67** |
| P1_COL_CNT | Port 1 Collision Count | $2A_H$ | **67** |
| P2_COL_CNT | Port 2 Collision Count | $2C_H$ | **67** |
| P3_COL_CNT | Port 3 Collision Count | $2E_H$ | **67** |
| P4_COL_CNT | Port 4 Collision Count | $2F_H$ | **67** |
| P5_COL_CNT | Port 5 Collision Count | $30_H$ | **67** |

**Table 24    Registers Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| P0_ERR_CNT | Port 0 Error Count | 31$_H$ | **67** |
| P1_ERR_CNT | Port 1 Error Count | 33$_H$ | **68** |
| P2_ERR_CNT | Port 2 Error Count | 35$_H$ | **68** |
| P3_ERR_CNT | Port 3 Error Count | 37$_H$ | **68** |
| P4_ERR_CNT | Port 4 Error Count | 38$_H$ | **68** |
| P5_ERR_CNT | Port 5 Error Count | 39$_H$ | **68** |
| **OverFlow_0** | Over Flow Flag Register 0 | 3A$_H$ | **68** |
| **OverFlow_1** | Over Flow Flag Register 1 | 3B$_H$ | **68** |
| **OverFlow_2** | Over Flow Flag Register 2 | 3C$_H$ | **69** |

The register is addressed wordwise.

For Register Access Types see **Table 12 "Register Access Types" on Page 42**.

**Table 25    Registers Clock Domains**

| Clock Short Name | Description |
|---|---|
| – | – |

## 4.2.1    Serial Register Map

**Chip Identifier Register**

| **ChipID** | **Offset** | **Reset Value** |
|---|---|---|
| **Chip Identifier Register** | **00$_H$** | **0007 1022$_H$** |



| Field | Bits | Type | Description |
|---|---|---|---|
| ID | 31:4 | ro | **Chip Identifier Register**<br>000 7102$_H$ **ID** Chip Identifier |
| Ver | 3:0 | ro | **Version No**<br>2$_H$  **Ver** Version No. |
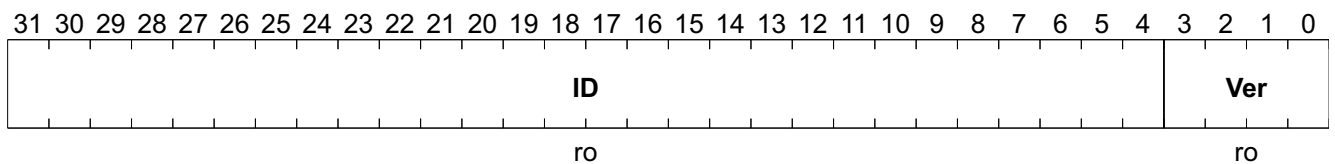
**Port Status Register 0**

| **PortStat_0** | **Offset** | **Reset Value** |
|---|---|---|
| **Port Status Register 0** | **01$_H$** | **0000 0000$_H$** |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 22 21 20 | 19 | 18 | 17 | 16 | 15 14 13 12 | 11 | 10 | 9 | 8 | 7 6 5 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FP 4 | DP 4 | SP 4 | LP 4 | FP 3 | DP 3 | SP 3 | LP 3 | Res | FP 2 | DP 2 | SP 2 | LP 2 | Res | FP 1 | DP 1 | SP 1 | LP 1 | Res | FP 0 | DP 0 | SP 0 | LP 0 |
| ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| FP4 | 31 | ro | **Port 4 Flow Control Enable**<br>$0_B$ **D** Flow Control Disable<br>$1_B$ **FC4** 802.3X on for full duplex or back pressure on for half duplex. |
| DP4 | 30 | ro | **Port 4 Duplex Status**<br>$0_B$ **H** Half Duplex<br>$1_B$ **F** Full Duplex |
| SP4 | 29 | ro | **Port 4 Speed Status**<br>$0_B$ **10** 10 Mbit/s<br>$1_B$ **100** 100 Mbit/s |
| LP4 | 28 | ro | **Port 4 Linkup Status**<br>$0_B$ **NE** Link is not established.<br>$1_B$ **E** Link is established. |
| FP3 | 27 | ro | **Port 3 Flow Control Enable**<br>$0_B$ **D** Flow Control Disable<br>$1_B$ **FC3** 802.3X on for full duplex or back pressure on for half duplex. |
| DP3 | 26 | ro | **Port 3 Duplex Status**<br>$0_B$ **H** Half Duplex<br>$1_B$ **F** Full Duplex |
| SP3 | 25 | ro | **Port 3 Speed Status**<br>$0_B$ **10** 10 Mbit/s<br>$1_B$ **100** 100 Mbit/s |
| LP3 | 24 | ro | **Port 3 Linkup Status**<br>Port 3 Linkup Status:<br>$0_B$ **N** Link is not established.<br>$1_B$ **E** Link is established. |
| Res | 23:20 | ro | **Reserved** |
| FP2 | 19 | ro | **Port 2 Flow Control Enable**<br>$0_B$ **D** Flow Control Disable<br>$1_B$ **FC2** 802.3X on for full duplex or back pressure on for half duplex. |
| DP2 | 18 | ro | **Port 2 Duplex Status**<br>$0_B$ **H** Half Duplex<br>$1_B$ **F** Full Duplex |
| SP2 | 17 | ro | **Port 2 Speed Status**<br>$0_B$ **10** 10 Mbit/s<br>$1_B$ **100** 100 Mbit/s |
| LP2 | 16 | ro | **Port 2 Linkup Status**<br>Port 2 Linkup Status:<br>$0_B$ **NE** Link is not established.<br>$1_B$ **E** Link is established. |
| Res | 15:12 | ro | **Reserved** |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| FP1 | 11 | ro | **Port 1 Flow Control Enable** <br> $0_B$   **D** Flow Control Disable <br> $1_B$   **FC1** 802.3X on for full duplex or back pressure on for half duplex. |
| DP1 | 10 | ro | **Port 1 Duplex Status** <br> $0_B$   **H** Half Duplex <br> $1_B$   **F** Full Duplex |
| SP1 | 9 | ro | **Port 1 Speed Status** <br> $0_B$   **10** 10 Mbit/s <br> $1_B$   **100** 100 Mbit/s |
| LP1 | 8 | ro | **Port 1 Linkup Status** <br> $0_B$   **NE** Not established. <br> $1_B$   **E** Established. |
| Res | 7:4 | ro | **Reserved** |
| FP0 | 3 | ro | **Port 0 Flow Control Enable** <br> $0_B$   **D** Flow Control Disable <br> $1_B$   **FC0** 802.3X on for full duplex or back pressure on for half duplex. |
| DP0 | 2 | ro | **Port 0 Duplex Status** <br> $0_B$   **H** Half Duplex <br> $1_B$   **F** Full Duplex |
| SP0 | 1 | ro | **Port 0 Speed Status** <br> $0_B$   **10** 10 Mbit/s <br> $1_B$   **100** 100 Mbit/s |
| LP0 | 0 | ro | **Port 0 Linkup Status** <br> $0_B$   **NE** Not established. <br> $1_B$   **E** Established. |

**Port Status Register 1**

| PortStat_1 | Offset | Reset Value |
|------------|--------|-------------|
| **Port Status Register 1** | $02_H$ | $0000\ 0000_H$ |

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
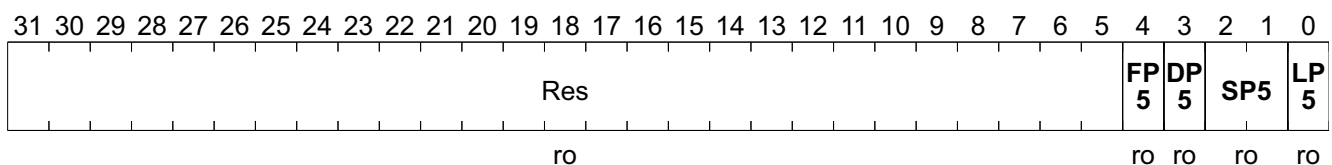
| Res | | | | | | | | | | | | | | | | | | | | | | | | | | | FP5 | DP5 | SP5 | | LP5 |

| ro | | | | | | | | | | | | | | | | | | | | | | | | | | | ro | ro | ro | | ro |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 31:5 | ro | **Reserved** |
| FP5 | 4 | ro | **Port 5 Flow Control Enable** <br> $0_B$   **D** Flow Control Disable <br> $1_B$   **FC5** 802.3X on for full duplex or back pressure on for half duplex. |
| DP5 | 3 | ro | **Port 5 Duplex Status** <br> $0_B$   **H** Half Duplex <br> $1_B$   **F** Full Duplex |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| SP5 | 2:1 | ro | **Port 5 Speed Status** <br> $0_B$    **10** 10 Mbit/s <br> $1_B$    **100** 100 Mbit/s |
| LP5 | 0 | ro | **Port 5 Linkup Status** <br> $0_B$    **NE** Not established. <br> $1_B$    **E** Established. |

**Cable Broken Status Register**
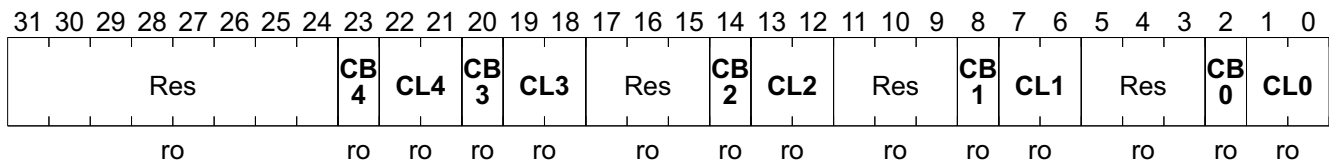
| CabStat | Offset | Reset Value |
|---------|--------|-------------|
| **Cable Broken Status** | $03_H$ | $0000\ 0000_H$ |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Res | | | | | CB4 | CL4 | | CB3 | CL3 | | Res | | | CB2 | CL2 | | Res | | | CB1 | CL1 | | Res | | | CB0 | CL0 | |
| | | | ro | | | | | ro | ro | | ro | ro | | ro | | | ro | ro | | ro | | | ro | ro | | ro | | | ro | ro | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 31:24 | ro | **Reserved** |
| CB4 | 23 | ro | **Port 4 Cable Broken** |
| CL4 | 22:21 | ro | **Port 4 Cable Broken Length** |
| CB3 | 20 | ro | **Port 3 Cable Broken** |
| CL3 | 19:18 | ro | **Port 3 Cable Broken Length** |
| Res | 17:15 | ro | **Reserved** |
| CB2 | 14 | ro | **Port 2 Cable Broken** |
| CL2 | 13:12 | ro | **Port 2 Cable Broken Length** |
| Res | 11:9 | ro | **Reserved** |
| CB1 | 8 | ro | **Port 1 Cable Broken** |
| CL1 | 7:6 | ro | **Port 1 Cable Broken Length** |
| Res | 5:3 | ro | **Reserved** |
| CB0 | 2 | ro | **Port 0 Cable Broken** |
| CL0 | 1:0 | ro | **Port 0 Cable Broken Length** |

**Port 0 Receive Packet Count**

| P0_RP_CNT | Offset | Reset Value |
|-----------|--------|-------------|
| **Port 0 Receive Packet Count** | $04_H$ | $0000\ 0000_H$ |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | **P0_RP_CNT** | | | | | | | | | | | | | | | | |

ro
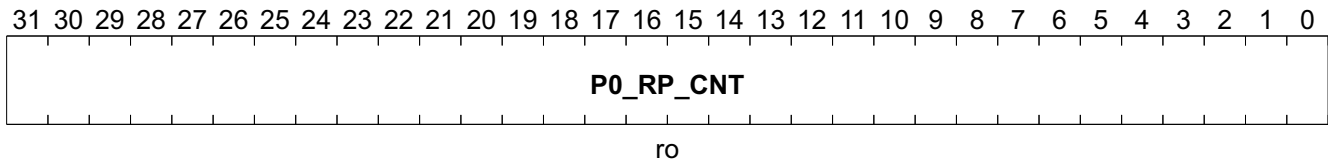
| Field | Bits | Type | Description |
|---|---|---|---|
| P0_RP_CNT | 31:0 | ro | **Counter** |

**Similar Registers**

**Table 26    Per Port Counters**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| P1_RP_CNT | Port 1 Receive Packet Count | 06$_H$ | |
| P2_RP_CNT | Port 2 Receive Packet Count | 08$_H$ | |
| P3_RP_CNT | Port 3 Receive Packet Count | 0A$_H$ | |
| P4_RP_CNT | Port 4 Receive Packet Count | 0B$_H$ | |
| P5_RP_CNT | Port 5 Receive Packet Count | 0C$_H$ | |
| P0_RB_CNT | Port 0 Receive Byte Count | 0D$_H$ | |
| P1_RB_CNT | Port 1 Receive Byte Count | 0F$_H$ | |
| P2_RB_CNT | Port 2 Receive Byte Count | 11$_H$ | |
| P3_RB_CNT | Port 3 Receive Byte Count | 13$_H$ | |
| P4_RB_CNT | Port 4 Receive Byte Count | 14$_H$ | |
| P5_RB_CNT | Port 5 Receive Byte Count | 15$_H$ | |
| P0_TP_CNT | Port 0 Transmit Packet Count | 16$_H$ | |
| P1_TP_CNT | Port 1 Transmit Packet Count | 18$_H$ | |
| P2_TP_CNT | Port 2 Transmit Packet Count | 1A$_H$ | |
| P3_TP_CNT | Port 3 Transmit Packet Count | 1C$_H$ | |
| P4_TP_CNT | Port 4 Transmit Packet Count | 1D$_H$ | |
| P5_TP_CNT | Port 5 Transmit Packet Count | 1E$_H$ | |
| P0_TB_CNT | Port 0 Transmit Byte Count | 1F$_H$ | |
| P1_TB_CNT | Port 1 Transmit Byte Count | 21$_H$ | |
| P2_TB_CNT | Port 2 Transmit Byte Count | 23$_H$ | |
| P3_TB_CNT | Port 3 Transmit Byte Count | 25$_H$ | |
| P4_TB_CNT | Port 4 Transmit Byte Count | 26$_H$ | |
| P5_TB_CNT | Port 5 Transmit Byte Count | 27$_H$ | |
| P0_COL_CNT | Port 0 Collision Count | 28$_H$ | |
| P1_COL_CNT | Port 1 Collision Count | 2A$_H$ | |
| P2_COL_CNT | Port 2 Collision Count | 2C$_H$ | |
| P3_COL_CNT | Port 3 Collision Count | 2E$_H$ | |
| P4_COL_CNT | Port 4 Collision Count | 2F$_H$ | |
| P5_COL_CNT | Port 5 Collision Count | 30$_H$ | |
| P0_ERR_CNT | Port 0 Error Count | 31$_H$ | |

**Table 26     Per Port Counters** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| P1_ERR_CNT | Port 1 Error Count | 33$_H$ | |
| P2_ERR_CNT | Port 2 Error Count | 35$_H$ | |
| P3_ERR_CNT | Port 3 Error Count | 37$_H$ | |
| P4_ERR_CNT | Port 4 Error Count | 38$_H$ | |
| P5_ERR_CNT | Port 5 Error Count | 39$_H$ | |

**Over Flow Flag Register 0**

| OverFlow_0 | Offset | Reset Value |
|---|---|---|
| Over Flow Flag Register 0 | 3A$_H$ | 0000 0000$_H$ |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Res | | | | | | | OR5 | OR4 | OR3 | Res | OR2 | Res | OR1 | Res | OR0 | OF5 | OF4 | OF3 | Res | OF2 | Res | OF1 | Res | OF0 |
| | | | | | | | ro | | | | | | | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 31:18 | ro | **Reserved** |
| OR5 | 17 | ro | **Overflow of Port 5 Receive Packet Byte Count** |
| OR4 | 16 | ro | **Overflow of Port 4 Receive Packet Byte Count** |
| OR3 | 15 | ro | **Overflow of Port 3 Receive Packet Byte Count** |
| Res | 14 | ro | **Reserved** |
| OR2 | 13 | ro | **Overflow of Port 2 Receive Packet Byte Count** |
| Res | 12 | ro | **Reserved** |
| OR1 | 11 | ro | **Overflow of Port 1 Receive Packet Byte Count** |
| Res | 10 | ro | **Reserved** |
| OR0 | 9 | ro | **Overflow of Port 0 Receive Packet Byte Count** |
| OF5 | 8 | ro | **Overflow of Port 5 Receive Packet Count** |
| OF4 | 7 | ro | **Overflow of Port 4 Receive Packet Count** |
| OF3 | 6 | ro | **Overflow of Port 3 Receive Packet Count** |
| Res | 5 | ro | **Reserved** |
| OF2 | 4 | ro | **Overflow of Port 2 Receive Packet Count** |
| Res | 3 | ro | **Reserved** |
| OF1 | 2 | ro | **Overflow of Port 1 Receive Packet Count** |
| Res | 1 | ro | **Reserved** |
| OF0 | 0 | ro | **Overflow of Port 0 Receive Packet Count** |
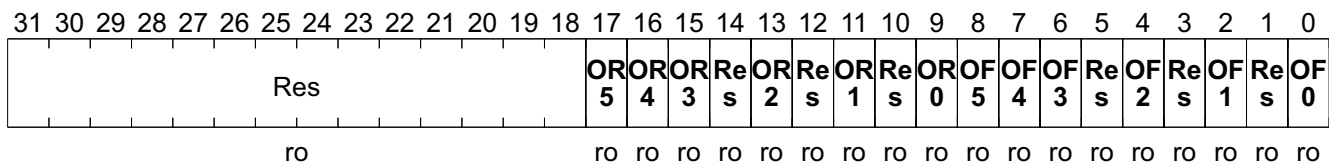
**Over Flow Flag Register 1**

**OverFlow_1**               **Offset**                    **Reset Value**
**Over Flow Flag Register 1**     3B$_H$                    0000 0000$_H$
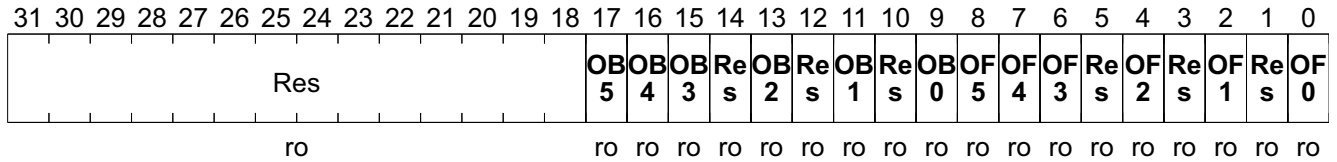
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Res | | | | | | | OB 5 | OB 4 | OB 3 | Re s | OB 2 | Re s | OB 1 | Re s | OB 0 | OF 5 | OF 4 | OF 3 | Re s | OF 2 | Re s | OF 1 | Re s | OF 0 |
| | | | | | | | ro | | | | | | | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 31:18 | ro | **Reserved** |
| OB5 | 17 | ro | **Overflow of Port 5 Transmit Packet Byte Count** |
| OB4 | 16 | ro | **Overflow of Port 4 Transmit Packet Byte Count** |
| OB3 | 15 | ro | **Overflow of Port 3 Transmit Packet Byte Count** |
| Res | 14 | ro | **Reserved** |
| OB2 | 13 | ro | **Overflow of Port 2 Transmit Packet Byte Count** |
| Res | 12 | ro | **Reserved** |
| OB1 | 11 | ro | **Overflow of Port 1 Transmit Packet Byte Count** |
| Res | 10 | ro | **Reserved** |
| OB0 | 9 | ro | **Overflow of Port 0 Transmit Packet Byte Count** |
| OF5 | 8 | ro | **Overflow of Port 5 Transmit Packet Count** |
| OF4 | 7 | ro | **Overflow of Port 4 Transmit Packet Count** |
| OF3 | 6 | ro | **Overflow of Port 3 Transmit Packet Count** |
| Res | 5 | ro | **Reserved** |
| OF2 | 4 | ro | **Overflow of Port 2 Transmit Packet Count** |
| Res | 3 | ro | **Reserved** |
| OF1 | 2 | ro | **Overflow of Port 1 Transmit Packet Count** |
| Res | 1 | ro | **Reserved** |
| OF0 | 0 | ro | **Overflow of Port 0 Transmit Packet Count** |

**Over Flow Flag Register 2**

**OverFlow_2**               **Offset**                    **Reset Value**
**Over Flow Flag Register 2**     3C$_H$                    0000 0000$_H$
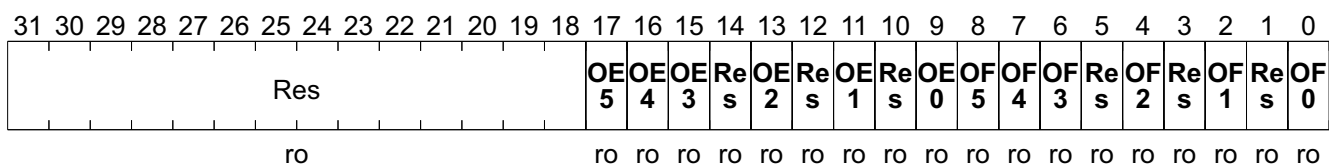
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Res | | | | | | | OE 5 | OE 4 | OE 3 | Re s | OE 2 | Re s | OE 1 | Re s | OE 0 | OF 5 | OF 4 | OF 3 | Re s | OF 2 | Re s | OF 1 | Re s | OF 0 |
| | | | | | | | ro | | | | | | | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 31:18 | ro | **Reserved** |
| OE5 | 17 | ro | **Overflow of Port 5 Error Count** |
| OE4 | 16 | ro | **Overflow of Port 4 Error Count** |
| OE3 | 15 | ro | **Overflow of Port 3 Error Count** |
| Res | 14 | ro | **Reserved** |
| OE2 | 13 | ro | **Overflow of Port 2 Error Count** |
| Res | 12 | ro | **Reserved** |
| OE1 | 11 | ro | **Overflow of Port 1 Error Count** |
| Res | 10 | ro | **Reserved** |
| OE0 | 9 | ro | **Overflow of Port 0 Error Count** |
| OF5 | 8 | ro | **Overflow of Port 5 Collision Count** |
| OF4 | 7 | ro | **Overflow of Port 4Collision Count** |
| OF3 | 6 | ro | **Overflow of Port 3Collision Count** |
| Res | 5 | ro | **Reserved** |
| OF2 | 4 | ro | **Overflow of Port 2 Collision Count** |
| Res | 3 | ro | **Reserved** |
| OF1 | 2 | ro | **Overflow of Port 1 Collision Count** |
| Res | 1 | ro | **Reserved** |
| OF0 | 0 | ro | **Overflow of Port 0 Collision Count** |

## 4.3 Packet with Priority: Normal packet content

**Table 27    Ethernet Packet from Layer 2**

| Preamble/SFD | Destination (6 bytes) | Source (6 bytes) | Packet length (2 bytes) | Data (46-1500 bytes) | CRC (4 bytes) |
|--------------|-----------------------|------------------|--------------------------|----------------------|---------------|
| | Byte 0~5 | Byte 6~11 | Byte 12~13 | Byte 14~ | |

## 4.4 VLAN Packet

**Table 28    VLAN Packet**

| Tag Protocol TD 8100 | Tag Control Information TCI | LEN Length | Routing Information |
|----------------------|----------------------------|------------|---------------------|
| Byte 12~13 | Byte14~15 | Byte 16~17 | Byte 18 |

*Note: ADM6996LC/LCX/LHX will check packet byte 12 &13. If byte[12:13]=8100h then this packet is a VLAN packet*

Byte 14~15: Tag Control Information TCI

Bit[15:13]: User Priority 7~0

Bit 12: Canonical Format Indicator (CFI)

Bit[11~0]: VLAN ID. The ADM6996LC/LCX/LHX will use bit[3:0] as VLAN group.

## 4.5 TOS IP Packet

**Table 29    IP Packet**

| Type 0800 | IP Header |
|---|---|
| Byte 12~13 | Byte 14~15 |

*Note: ADM6996LC/LCX/LHX checks bytes 12 &13. If this value is 0800h then the ADM6996LC/LCX/LHX knows this is a TOP priority packet.*

IP header define

Byte 14

Bit[7:0]: IP protocol version number & header length.

Byte 15: Service type

Bit[7~5]: IP Priority (Precedence) from 7~0

Bit 4: No Delay (D)

Bit 3: High Throughput

Bit 2: High Reliability (R)

Bit[1:0]: Reserved

## 4.6 EEPROM Access

Customer can select ADM6996LC/LCX/LHX read EEPROM contents as chip setting or not. ADM6996LC/LCX/LHX will check the signature of EEPROM to decide read content of EEPROM or not.

**Table 30    RESETL & EEPROM content relationship**

| RESETL | CS | SK | DI | DO |
|---|---|---|---|---|
| 0 | High Impedance | High Impedance | High Impedance | High Impedance |
| Rising edge 01 (30ms) | Output | Output | Output | Input |
| 1 (after 30ms) | Input | Input | Output | Input |

Keep at least 30ms after RESETL from 01. ADM6996LC/LCX/LHX will read data from EEPROM. After RESETL if CPU update EEPROM that ADM6996LC/LCX/LHX will update configuration registers too.

When CPU programming EEPROM & ADM6996LC/LCX/LHX, ADM6996LC/LCX/LHX recognizes the EEPROM WRITE instruction only. If there is any Protection instruction before or after the EEPROM WRITE instruction, CPU needs to generate separated CS signal cycle for each Protection & WRITE instruction.

CPU can directly program ADM6996LC/LCX/LHX after 30ms of Reset signal rising edge with or without EEPROM

ADM6996LC/LCX/LHX serial chips will latch hardware-reset value as recommend value. It includes EEPROM interface:

EECS: Internal Pull down 40K resister.

EESK: TP port Auto-MDIX select. Internal pull down 40K resister as non Auto-MDIX mode.

EDI: Dual Color Select. Internal pull down 40K resister as Single Color Mode.

EDO: EEPROM enable. Internal pull up 40K resister as EEPROM enable.

Below Figure is ADM6996LC/LCX/LHX serial chips EEPROM pins operation at different stage. Reset signal is control by CPU with at least 100ms low. Point1 is Reset rising edge. CPU must prepare proper value on EECS(0),

EESK, EDI, EDO(1) before this rising edge. ADM6996LC/LCX/LHX will read this value into chip at Point2. CPU must keep these values over point2. Point2 is 200ns after Reset rising edge.

ADM6996LC/LCX/LHX serial chips will read EEPROM content at Point4 which 800ns far away from the rising edge of Reset. CPU must turn EEPROM pins EECS, EESK, EDI and EDO to High-Z or pull high before Point4.

If user want change state to High-Z or pull high on EEPROM pins, the order is CS-> DI -> DO -> SK is better.
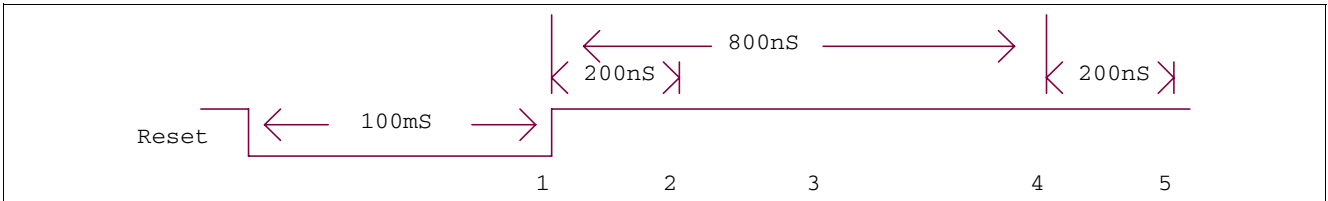


**Figure 10    CPU Generated Reset Signal Requirement**

A little bit different with the timing on writing EEPROM. See below graph. Must be careful when CS goes down after writing a command, SK must issue at least one clock. This is a difference between ADM6996LC/LCX/LHX with EEPROM write timing. If system without EEPROM then user must write ADM6996LC/LCX/LHX internal register by 93C66 timing. If user uses EEPROM then the writing timing is depend on EEPROM type.
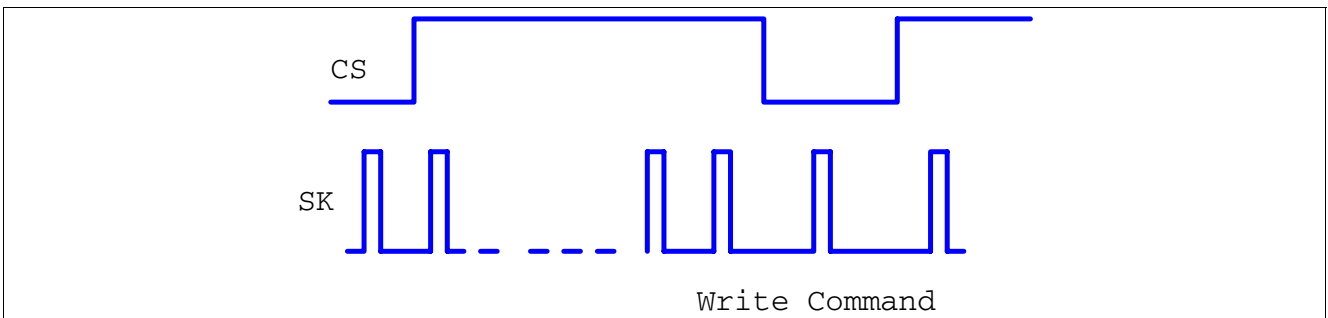


**Figure 11    CPU Write EEPROM Command Requirement**

## 4.7      Serial Interface Timing

**ADM6996LC/LCX/LHX serial chip's internal counter or EEPROM access timing**

EESK: Similar to the MDC signal.

EDI: Similar to the MDIO signal

ECS: Must keep be kept low.
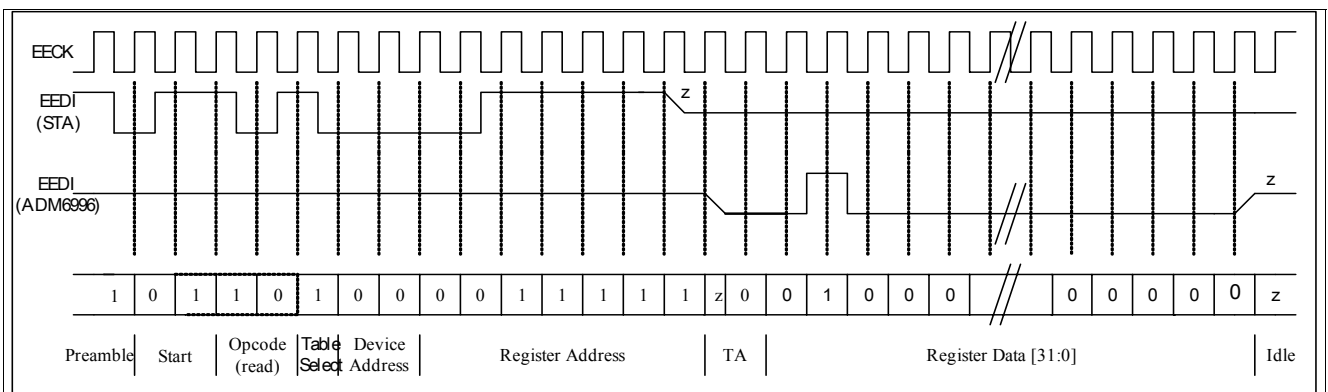


**Figure 12    Serial Interface Read Command Timing**

Preamble: At least 32 continuous $1_B$'s

Start: $01_B$(2 bits)

Opcode: $10_B$ (2 bits, Only supports a read command)

Table select: $1_B$ = Counter, $0_B$ = EEPROM (1 bit)

Register Address: Read Target register address. (7 bits)

TA: Turn Around.

Register Data: 32 bit data.

Counter output bit sequence is bit 31 to bit 0.

If a user reads the EEPROM then 32 bits of data will separate as two EEPROM registers. The sequence is:

1.  Register +1, Register (Register is even number)
2.  Register, Register-1(Register is Odd number)

**Example:**

Read Register $00_H$ then the ADM6996LC/LCX/LHX will drive $01_H$ & $00_H$

Read Register $03_H$ then ADM6996LC/LCX/LHX will drive $03_H$ & $02_H$

Idle: EESK must send at least one clock pulse at idle time

**ADM6996LC/LCX/LHX issue Reset internal counter command**

EESK: Similar to the MDC signal

EDI: Similar to the MDIO signal

ECS: Must keep low.
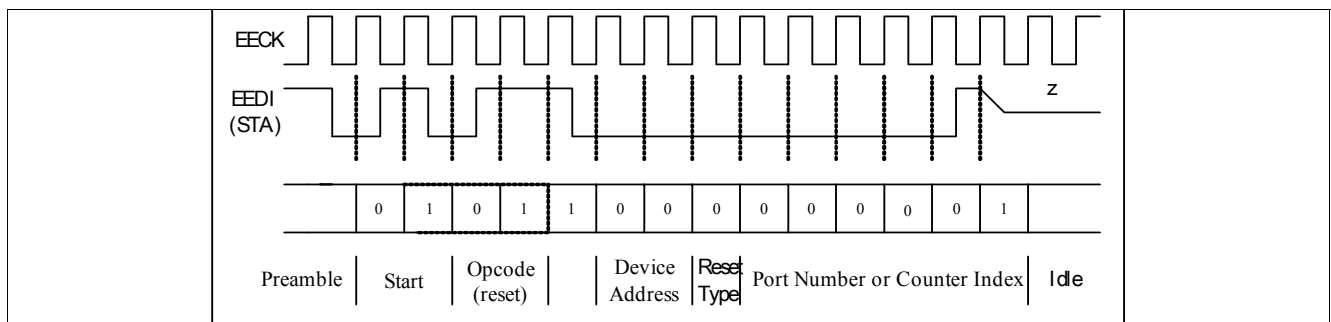


**Figure 13    Serial Interface Reset Command Timing**

Preamble: At least 32 continuous $1_B$'s

Start: $01_B$(2 bits)

Opcode: $01_B$ (2 bits, Reset command)

Device Address: Chip physical address as PHYAS[1:0].

Reset_type: Reset the counter by port number or by counter index

$1_B$ = Clear dedicate port's all counters

$0_B$ = Clear dedicate counter

Port_number or counter index: User defines clear port or counter

Idle: EESK must send at least one clock pulse at idle time

# 5    16 Bits Mode Registers Description

**Broadcast Storm**

ADM6996LC/LCX/LHX allows users to limit the traffic of the broadcast address (DA = $FFFFFFFFFFFF_H$) to prevent them from blocking the switch bandwidth. If users also want to limit the multicast packets(DA[40] = $1_B$), they can set the Multicast Packet Counted into Storming Counter (see $0010_H$, **MP**) function. Two threshold and storm enable bits (see $003B_H$ and $003C_H$, **STORM_EN**, **STORM_100_TH**, **STORM_10_TH**) are used to control the broadcast storm. The threshold is described in **Table 31 Broadcast Storming Threshold**.

1. Time Scale. ADM6996LC/LCX/LHX uses 50ms as the scale to meter the storm packets.

2. Storm keeps on at least 1.6 seconds if any of the ports meet the rising threshold in the 4 consecutive 50 ms intervals. In these 1.6 seconds, the ports meet the rising threshold and will start to discard the broadcast or multicast packets until the 50 ms interval expires. Users could also disable Input Filter (see $000B_H$, **IF**) function to forward above packets to the un-congested port instead of discarding directly.

3. Storm finishes. After the 1.6-second storm period, ADM6996LC/LCX/LHX will check the port that makes the storm on. If all of these ports meet the falling threshold in the 2 consecutive 50 ms intervals and no other ports meet the rising threshold at the same time, ADM6996LC/LCX/LHX will treat it the storm has finished.

Priority Queue

ADM6996LC/LCX/LHX supports 4 priority queues and each is assigned a weight. User can see **Priority Queue Weight Ratio** for more detail.

The EEPROM provides ADM6996LC/LCX/LHX with many option settings

**Main Settings**

- Port Configuration: Speed, Duplex, Flow Control Capability and Tag/ Untag.
- VLAN & TOS Priority Mapping
- Broadcast Storming rate and Trunk.
- Fiber Select, Auto MDIX select
- VLAN Mapping
- Per Port Buffer number
- Priority queue and smart discard ratio

**Table 31    Broadcast Storming Threshold**

| Parameter | Rising Threshold | Falling Threshold |
|---|---|---|
| All link ports are 100M | 100M Threshold (See $003B_H$) | 1/2 100M Threshold |
| Not All link ports are 100M | 10M Threshold (See $003C_H$) | 1/2 10M Threshold |

**Table 32    Priority Queue Weight Ratio**

| Queue | Weight |
|---|---|
| Queue 0 | Weight = 1 |
| Queue 1 | Weight = "Queue 1 Weight" bits in $0025_H$ |
| Queue 2 | Weight = "Queue 2 Weight" bits in $0026_H$ |
| Queue 3 | Weight = "Queue 3 Weight" bits in $0027_H$ |

**Table 33    Registers Address Space**

| Module | Base Address | End Address | Note |
|---|---|---|---|
| EEPROM Basic Register Map | $0000_H$ | $003F_H$ | |
| EEPROM Extended Register Map | $0040_H$ | $009C_H$ | |
| Counter and Switch Status Map | $00A0_H$ | $0143_H$ | |
| PHY Register Map | $0200_H$ | $02FF_H$ | |

**Table 34    Registers Overview**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| **SIG** | Signature Register | $00_H$ | **85** |
| **P0BC** | P0 Basic Control Register | $01_H$ | **85** |
| **Res0** | Reserved Register 0 | $02_H$ | **87** |
| P1 | Basic Control Register 1 | $03_H$ | **86** |
| Res1 | Reserved Register 1 | $04_H$ | **87** |
| P2 | Basic Control Register 2 | $05_H$ | **86** |
| Res2 | Reserved Register 2 | $06_H$ | **87** |
| P3 | Basic Control Register 3 | $07_H$ | **86** |
| P4 | Basic Control Register 4 | $08_H$ | **87** |
| P5 | Basic Control Register 5 | $09_H$ | **87** |
| **SC0** | System Control Register 0 | $0A_H$ | **88** |
| **SC1** | System Control Register 1 | $0B_H$ | **89** |
| Res3 | Reserved Register 3 | $0C_H$ | **87** |
| Res4 | Reserved Register 4 | $0D_H$ | **87** |
| **VPM** | VLAN Priority Map Register | $0E_H$ | **90** |
| **TPM** | TOS Priority Map Register | $0F_H$ | **91** |
| **SC2** | System Control Register 2 | $10_H$ | **92** |
| **SC3** | System Control Register 3 | $11_H$ | **92** |
| **SC4** | System Control Register 4 | $12_H$ | **94** |
| **P0SO** | Port 0 Security Option | $13_H$ | **95** |
| P1SO | Port 1 Security Option | $14_H$ | **96** |
| P2SO | Port 2 Security Option | $15_H$ | **96** |
| P3SO | Port 3 Security Option | $16_H$ | **96** |
| P4SO | Port 4 Security Option | $17_H$ | **96** |
| P5SO | Port 5 Security Option | $18_H$ | **96** |
| **UFGPM** | Unicast Port Map and Forward Group Port Map | $19_H$ | **96** |
| **BFGPM** | Broadcast Port Map andForward Group Port Map | $1A_H$ | **97** |
| **MFGPM** | Multicast Port Map and Forward Group Port Map | $1B_H$ | **98** |
| **RFGPM** | Reserve Port Map and Forward Group Port Map | $1C_H$ | **98** |
| **PIOFGPM** | Packet Identification Option, Forward Group Port Map | $1D_H$ | **99** |

**Table 34    Registers Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| **VPEFGPM** | VLAN Priority Enable and Forward Group Port Map | $1E_H$ | **100** |
| **SPEFGPM** | Service Priority Enable and Forward Group Port Map | $1F_H$ | **101** |
| **IFNTFGPM** | Input Force No Tag and Forward Group Port Map | $20_H$ | **102** |
| **IFFGPM** | Ingress Filter andForward Group Port Map | $21_H$ | **103** |
| **VSDFGPM** | VLAN Security Disable and Forward Group Port Map | $22_H$ | **104** |
| Res5 | Reserved Register 5 | $23_H$ | **87** |
| Res6 | Reserved Register 6 | $24_H$ | **87** |
| **IMEIJT** | IGMP/MLDTRAP Enable and Input Jam Threshold Register | $25_H$ | **105** |
| **Q2WVECPO** | Queue 2 Weight, VID Exist Check, and PPPOE Port Only | $26_H$ | **105** |
| **Q3WBPVAO** | Queue 3 Weight, Back to Port VLAN, and Admit Only VLAN-Tagged | $27_H$ | **106** |
| **IDTEP** | Input Double Tag Enable, and P0VID[11:4] | $28_H$ | **106** |
| **ODTEP** | Output Double Tag Enable, and P1VID[11:4] | $29_H$ | **107** |
| **OTBP** | Output Tag Bypass, and P2VID[11:4] | $2A_H$ | **107** |
| **P11_4** | P3VID[11:4], and P4VID[11:4] | $2B_H$ | **108** |
| **RACP** | Reserved Address Control, and P5VID[11:4] | $2C_H$ | **108** |
| **PHYC** | PHY Control Register | $2D_H$ | **108** |
| **ATET** | ADM TAG Ether Type | $2E_H$ | **109** |
| **PR** | PHY Restart Register | $2F_H$ | **109** |
| **MISC** | Miscellaneous Register | $30_H$ | **110** |
| **BBC0** | Basic Bandwidth Control Register 0 | $31_H$ | **111** |
| **BBC1** | Basic Bandwidth Control Register 1 | $32_H$ | **111** |
| **BCE** | Bandwidth Control Enable Register | $33_H$ | **112** |
| **EBC0** | Extended Bandwidth Control Register 0 | $34_H$ | **114** |
| **EBC1** | Extended Bandwidth Control Register 1 | $35_H$ | **114** |
| **EBC2** | Extended Bandwidth Control Register 2 | $36_H$ | **115** |
| **EBC3** | Extended Bandwidth Control Register 3 | $37_H$ | **115** |
| **EBC4** | Extended Bandwidth Control Register 4 | $38_H$ | **116** |
| **EBC5** | Extended Bandwidth Control Register 5 | $39_H$ | **117** |
| **DVMEBC6** | Default VLAN Member and Extended Bandwidth Control Register 6 | $3A_H$ | **117** |
| **NS0** | New Storm Register 0 | $3B_H$ | **118** |
| **NS1** | New Storm Register 1 | $3C_H$ | **118** |
| **NRAC0** | New Reserve Address Control Register 0 | $3D_H$ | **119** |
| **NRAC1** | New Reserve Address Control Register 1 | $3E_H$ | **120** |
| Res7 | Reserved Register 7 | $3F_H$ | **87** |
| **VF0L** | VLAN Filter 0 Low | $40_H$ | **122** |

**Table 34    Registers Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| **VF0H** | VLAN Filter 0 High | $41_H$ | **123** |
| VF1L | VLAN Filter 1 Low | $42_H$ | **122** |
| VF1H | VLAN Filter 1 High | $43_H$ | **123** |
| VF2L | VLAN Filter 2 Low | $44_H$ | **122** |
| VF2H | VLAN Filter 2 High | $45_H$ | **123** |
| VF3L | VLAN Filter 3Low | $46_H$ | **122** |
| VF3H | VLAN Filter 3 High | $47_H$ | **123** |
| VF4L | VLAN Filter 4 Low | $48_H$ | **122** |
| VF4H | VLAN Filter 4 High | $49_H$ | **123** |
| VF5L | VLAN Filter 5 Low | $4A_H$ | **122** |
| VF5H | VLAN Filter 5 High | $4B_H$ | **123** |
| VF6L | VLAN Filter 6 Low | $4C_H$ | **122** |
| VF6H | VLAN Filter 6 High | $4D_H$ | **123** |
| VF7L | VLAN Filter 7 Low | $4E_H$ | **122** |
| VF7H | VLAN Filter 7 High | $4F_H$ | **123** |
| VF8L | VLAN Filter 8 Low | $50_H$ | **122** |
| VF8H | VLAN Filter 8 High | $51_H$ | **123** |
| VF9L | VLAN Filter 9 Low | $52_H$ | **122** |
| VF9H | VLAN Filter 9 High | $53_H$ | **123** |
| VF10L | VLAN Filter 10 Low | $54_H$ | **122** |
| VF10H | VLAN Filter 10 High | $55_H$ | **123** |
| VF11L | VLAN Filter 11 Low | $56_H$ | **122** |
| VF11H | VLAN Filter 11 High | $57_H$ | **123** |
| VF12L | VLAN Filter 12 Low | $58_H$ | **122** |
| VF12H | VLAN Filter 12 High | $59_H$ | **123** |
| VF13L | VLAN Filter 13 Low | $5A_H$ | **122** |
| VF13H | VLAN Filter 13 High | $5B_H$ | **123** |
| VF14L | VLAN Filter 14 Low | $5C_H$ | **122** |
| VF14H | VLAN Filter 14 High | $5D_H$ | **123** |
| VF15L | VLAN Filter 15 Low | $5E_H$ | **122** |
| VF15H | VLAN Filter 15 High | $5F_H$ | **123** |
| **TF0** | Type Filter 0 | $60_H$ | **124** |
| TF1 | Type Filter 1 | $61_H$ | **124** |
| TF2 | Type Filter 2 | $62_H$ | **124** |
| TF3 | Type Filter 3 | $63_H$ | **124** |
| TF4 | Type Filter 4 | $64_H$ | **124** |
| TF5 | Type Filter 5 | $65_H$ | **124** |
| TF6 | Type Filter 6 | $66_H$ | **124** |
| TF7 | Type Filter 7 | $67_H$ | **124** |
| **PF_1_0** | Protocol Filter 1 and 0 | $68_H$ | **124** |
| PF_3_2 | Protocol Filter 3 and 2 | $68_H$ | **125** |

**Table 34    Registers Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| PF_5_4 | Protocol Filter 5 and 4 | $69_H$ | **125** |
| PF_7_6 | Protocol Filter 7 and 6 | $6A_H$ | **125** |
| Res8 | Reserved Register 8 | $6C_H$ | **87** |
| Res9 | Reserved Register 9 | $6D_H$ | **87** |
| Res10 | Reserved Register 10 | $6E_H$ | **87** |
| Res11 | Reserved Register 11 | $6F_H$ | **87** |
| Res12 | Reserved Register 12 | $70_H$ | **87** |
| Res13 | Reserved Register 13 | $71_H$ | **87** |
| Res14 | Reserved Register 14 | $72_H$ | **87** |
| Res15 | Reserved Register 15 | $73_H$ | **87** |
| Res16 | Reserved Register 16 | $74_H$ | **87** |
| Res17 | Reserved Register 17 | $75_H$ | **87** |
| Res18 | Reserved Register 18 | $76_H$ | **87** |
| Res19 | Reserved Register 19 | $77_H$ | **87** |
| Res20 | Reserved Register 20 | $78_H$ | **87** |
| Res21 | Reserved Register 21 | $79_H$ | **88** |
| Res22 | Reserved Register 22 | $7A_H$ | **88** |
| Res23 | Reserved Register 23 | $7B_H$ | **88** |
| Res24 | Reserved Register 24 | $7C_H$ | **88** |
| Res25 | Reserved Register 25 | $7D_H$ | **88** |
| Res26 | Reserved Register 26 | $7E_H$ | **88** |
| Res27 | Reserved Register 27 | $7F_H$ | **88** |
| Res28 | Reserved Register 28 | $80_H$ | **88** |
| Res29 | Reserved Register 29 | $81_H$ | **88** |
| Res30 | Reserved Register 30 | $82_H$ | **88** |
| Res31 | Reserved Register 31 | $83_H$ | **88** |
| Res32 | Reserved Register 32 | $84_H$ | **88** |
| Res33 | Reserved Register 33 | $85_H$ | **88** |
| Res34 | Reserved Register 34 | $86_H$ | **88** |
| Res35 | Reserved Register 35 | $87_H$ | **88** |
| Res36 | Reserved Register 36 | $88_H$ | **88** |
| Res37 | Reserved Register 37 | $89_H$ | **88** |
| Res38 | Reserved Register 38 | $8A_H$ | **88** |
| Res39 | Reserved Register 39 | $8B_H$ | **88** |
| **TUF0** | TCP/UDP Filter 0 | $8C_H$ | **125** |
| TUF1 | TCP/UDP Filter 1 | $8D_H$ | **125** |
| TUF2 | TCP/UDP Filter 2 | $8E_H$ | **125** |
| TUF3 | TCP/UDP Filter 3 | $8F_H$ | **125** |
| TUF4 | TCP/UDP Filter 4 | $90_H$ | **125** |
| TUF5 | TCP/UDP Filter 5 | $91_H$ | **125** |
| TUF6 | TCP/UDP Filter 6 | $92_H$ | **125** |

**Table 34    Registers Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| TUF7 | TCP/UDP Filter 7 | $93_H$ | **125** |
| **TFA** | Type Filter Action | $94_H$ | **126** |
| **PFA** | Protocol Filter Action | $95_H$ | **126** |
| **TUA0** | TCP/UDP Action 0 | $96_H$ | **127** |
| **TUA1** | TCP/UDP Action 1 | $97_H$ | **128** |
| **TUA2** | TCP/UDP Action 2 | $98_H$ | **129** |
| Res40 | Reserved Register 40 | $99_H$ | **88** |
| **IE** | Interrupt Enable Register | $9A_H$ | **130** |
| **IS** | Interrupt Status Register | $9B_H$ | **130** |
| Res41 | Reserved Register 41 | $9C_H$ | **88** |
| **CI0** | Chip Identifier 0 | $A0_H$ | **131** |
| **CI1** | Chip Identifier 1 | $A1_H$ | **131** |
| **PS0** | Port Status 0 | $A2_H$ | **132** |
| **PS1** | Port Status 1 | $A3_H$ | **133** |
| **PS2** | Port Status 2 | $A4_H$ | **134** |
| Res42 | Reserved Register 42 | $A5_H$ | **88** |
| Res43 | Reserved Register 43 | $A6_H$ | **88** |
| Res44 | Reserved Register 44 | $A7_H$ | **88** |
| **CL0** | Port 0 Receive Packet Counter Low | $A8_H$ | **134** |
| **CH0** | Port 0 Receive Packet Counter High | $A9_H$ | **136** |
| CL1 | Port 1 Receive Packet Counter Low | $AC_H$ | **135** |
| CH1 | Port 1 Receive Packet Counter High | $AD_H$ | **136** |
| CL2 | Port 2 Receive Packet Counter Low | $B0_H$ | **135** |
| CH2 | Port 2 Receive Packet Counter High | $B1_H$ | **136** |
| CL3 | Port 3 Receive Packet Counter Low | $B4_H$ | **135** |
| CH3 | Port 3 Receive Packet Counter High | $B5_H$ | **136** |
| CL4 | Port 4 Receive Packet Counter Low | $B6_H$ | **135** |
| CH4 | Port 4 Receive Packet Counter High | $B7_H$ | **136** |
| CL5 | Port 5 Receive Packet Counter Low | $B8_H$ | **135** |
| CH5 | Port 5 Receive Packet Counter High | $B9_H$ | **136** |
| CL6 | Port 0 Receive Packet Byte Count Low | $BA_H$ | **135** |
| CH6 | Port 0 Receive Packet Byte Count High | $BB_H$ | **136** |
| CL7 | Port 1 Receive Packet Byte Count Low | $BE_H$ | **135** |
| CH7 | Port 1 Receive Packet Byte Count High | $BF_H$ | **136** |
| CL8 | Port 2 Receive Packet Byte Count Low | $C2_H$ | **135** |
| CH8 | Port 2 Receive Packet Byte Count High | $C3_H$ | **136** |
| CL9 | Port 3 Receive Packet Byte Count Low | $C6_H$ | **135** |
| CH9 | Port 3 Receive Packet Byte Count High | $C7_H$ | **136** |
| CL10 | Port 4 Receive Packet Byte Count Low | $C8_H$ | **135** |
| CH10 | Port 4 Receive Packet Byte Count High | $C9_H$ | **136** |
| CL11 | Port 5 Receive Packet Byte Count Low | $CA_H$ | **135** |

**Table 34    Registers Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| CH11 | Port 5 Receive Packet Byte Count High | $CB_H$ | **136** |
| CL12 | Port 0 Transmit Packet Count Low | $CC_H$ | **135** |
| CH12 | Port 0 Transmit Packet Count High | $CD_H$ | **136** |
| CL13 | Port 1 Transmit Packet Count Low | $D0_H$ | **135** |
| CH13 | Port 1 Transmit Packet Count High | $D1_H$ | **136** |
| CL14 | Port 2 Transmit Packet Count Low | $D4_H$ | **135** |
| CH14 | Port 2 Transmit Packet Count High | $D5_H$ | **136** |
| CL15 | Port 3 Transmit Packet Count Low | $D8_H$ | **135** |
| CH15 | Port 3 Transmit Packet Count High | $D9_H$ | **137** |
| CL16 | Port 4 Transmit Packet Count Low | $DA_H$ | **135** |
| CH16 | Port 4 Transmit Packet Count High | $DB_H$ | **137** |
| CL17 | Port 5 Transmit Packet Count Low | $DC_H$ | **135** |
| CH17 | Port 5 Transmit Packet Count High | $DD_H$ | **137** |
| CL18 | Port 0 Transmit Packet Byte Count Low | $DE_H$ | **135** |
| CH18 | Port 0 Transmit Packet Byte Count High | $DF_H$ | **137** |
| CL19 | Port 1 Transmit Packet Byte Count Low | $E2_H$ | **135** |
| CH19 | Port 1 Transmit Packet Byte Count High | $E3_H$ | **137** |
| CL20 | Port 2 Transmit Packet Byte Count Low | $E6_H$ | **135** |
| CH20 | Port 2 Transmit Packet Byte Count High | $E7_H$ | **137** |
| CL21 | Port 3 Transmit Packet Byte Count Low | $EA_H$ | **135** |
| CH21 | Port 3 Transmit Packet Byte Count High | $EB_H$ | **137** |
| CL22 | Port 4 Transmit Packet Byte Count Low | $EC_H$ | **135** |
| CH22 | Port 4 Transmit Packet Byte Count High | $ED_H$ | **137** |
| CL23 | Port 5 Transmit Packet Byte Count Low | $EE_H$ | **135** |
| CH23 | Port 5 Transmit Packet Byte Count High | $EF_H$ | **137** |
| CL24 | Port 0 Collision Count Low | $F0_H$ | **135** |
| CH24 | Port 0 Collision Count High | $F1_H$ | **137** |
| CL25 | Port 1 Collision Count Low | $F4_H$ | **135** |
| CH25 | Port 1 Collision Count High | $F5_H$ | **137** |
| CL26 | Port 2 Collision Count Low | $F8_H$ | **135** |
| CH26 | Port 2 Collision Count High | $F9_H$ | **137** |
| CL27 | Port 3 Collision Count Low | $FC_H$ | **135** |
| CH27 | Port 3 Collision Count High | $FD_H$ | **137** |
| CL28 | Port 4 Collision Count Low | $FE_H$ | **135** |
| CH28 | Port 4 Collision Count High | $FF_H$ | **137** |
| CL29 | Port 5 Collision Count Low | $100_H$ | **135** |
| CH29 | Port 5 Collision Count High | $101_H$ | **137** |
| CL30 | Port 0 Error Count Low | $102_H$ | **136** |
| CH30 | Port 0 Error Count High | $103_H$ | **137** |
| CL31 | Port 1 Error Count Low | $106_H$ | **136** |
| CH31 | Port 1 Error Count High | $107_H$ | **137** |

**Table 34 Registers Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| CL32 | Port 2 Error Count Low | 10A$_H$ | **136** |
| CH32 | Port 2 Error Count High | 10B$_H$ | **137** |
| CL33 | Port 3 Error Count Low | 10E$_H$ | **136** |
| CH33 | Port 3 Error Count High | 10F$_H$ | **137** |
| CL34 | Port 4 Error Count Low | 110$_H$ | **136** |
| CH34 | Port 4 Error Count High | 111$_H$ | **137** |
| CL35 | Port 5 Error Count Low | 112$_H$ | **136** |
| CH35 | Port 5 Error Count High | 113$_H$ | **137** |
| **OFF0** | Over-Flow Flag 0 | 114$_H$ | **137** |
| **OFF1** | Over-Flow Flag 1 | 115$_H$ | **138** |
| **OFF2** | Over-Flow Flag 2 | 116$_H$ | **139** |
| **OFF3** | Over-Flow Flag 3 | 117$_H$ | **140** |
| **OFF4** | Over-Flow Flag 4 | 118$_H$ | **140** |
| **OFF5** | Over-Flow Flag 5 | 119$_H$ | **141** |
| **HSL** | Hardware Setting Low Register | 130$_H$ | **142** |
| **HSH** | Hardware Setting High Register | 131$_H$ | **142** |
| Res45 | Reserved Register 45 | 132$_H$ | **88** |
| Res46 | Reserved Register 46 | 133$_H$ | **88** |
| Res47 | Reserved Register 47 | 134$_H$ | **88** |
| **AO** | Assign Option Register | 135$_H$ | **143** |
| Res48 | Reserved Register 48 | 136$_H$ | **88** |
| Res49 | Reserved Register 49 | 137$_H$ | **88** |
| **SVP** | Security Violation Port | 138$_H$ | **144** |
| **SS0** | Security Status 0 | 139$_H$ | **144** |
| **SS1** | Security Status 1 | 13A$_H$ | **145** |
| **FLAS** | First Lock Address Search | 13B$_H$ | **145** |
| **FLA1** | First Lock Address [15:0] | 13C$_H$ | **146** |
| **FLA2** | First Lock Address [31:16] | 13D$_H$ | **146** |
| **FLA3** | First Lock Address [47:32] | 13E$_H$ | **146** |
| **FLF** | First Lock FID | 13F$_H$ | **147** |
| **CCL** | Counter Control Low Register | 140$_H$ | **147** |
| Res50 | Reserved Register 50 | 141$_H$ | **88** |
| **CSL** | Counter Status Low Register | 142$_H$ | **148** |
| **CSH** | Counter Status High Register | 143$_H$ | **148** |
| **PHY_C0** | PHY Control Register of Port 0 | 200$_H$ | **148** |
| **PHY_S0** | PHY Status Register of Port 0 | 201$_H$ | **151** |
| **PHY_I0_A** | PHY Identifier Register of Port 0 (A) | 202$_H$ | **152** |
| **PHY_I0_B** | PHY Identifier Register of Port 0 (B) | 203$_H$ | **153** |
| **ANAP0** | Auto Negotiation Advertisement Register of Port 0 | 204$_H$ | **154** |
| **ANLPA0** | Auto Negotiation Link Partner Ability Register of Port 0 | 205$_H$ | **155** |

**Table 34    Registers Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| **ANE0** | Auto Negotiation Expansion Register of Port 0 | 206$_H$ | **156** |
| **NPT0** | Next Page Transmit Register of Port 0 | 207$_H$ | **157** |
| **LPNP0** | Link Partner Next Page Register of Port 0 | 208$_H$ | **158** |
| PHY_C1 | PHY Control Register of Port 1 | 220$_H$ | **150** |
| PHY_S1 | PHY Status Register of Port 1 | 221$_H$ | **152** |
| PHY_I1_A | PHY Identifier Register of Port 1 (A) | 222$_H$ | **153** |
| PHY_I1_B | PHY Identifier Register of Port 1 (B) | 223$_H$ | **153** |
| ANAP1 | Auto Negotiation Advertisement Register of Port 1 | 224$_H$ | **155** |
| ANLPA1 | Auto Negotiation Link Partner Ability Register of Port 1 | 225$_H$ | **156** |
| ANE1 | Auto Negotiation Expansion Register of Port 1 | 226$_H$ | **157** |
| NPT1 | Next Page Transmit Register of Port 1 | 227$_H$ | **158** |
| LPNP1 | Link Partner Next Page Register of Port 1 | 228$_H$ | **159** |
| PHY_C2 | PHY Control Register of Port 2 | 240$_H$ | **150** |
| PHY_S2 | PHY Status Register of Port 2 | 241$_H$ | **152** |
| PHY_I2_A | PHY Identifier Register of Port 2 (A) | 242$_H$ | **153** |
| PHY_I2_B | PHY Identifier Register of Port 2 (B) | 243$_H$ | **153** |
| ANAP2 | Auto Negotiation Advertisement Register of Port 2 | 244$_H$ | **155** |
| ANLPA2 | Auto Negotiation Link Partner Ability Register of Port 2 | 245$_H$ | **156** |
| ANE2 | Auto Negotiation Expansion Register of Port 2 | 246$_H$ | **157** |
| NPT2 | Next Page Transmit Register of Port 2 | 247$_H$ | **158** |
| LPNP2 | Link Partner Next Page Register of Port 2 | 248$_H$ | **159** |
| PHY_C3 | PHY Control Register of Port 3 | 260$_H$ | **150** |
| PHY_S3 | PHY Status Register of Port 3 | 261$_H$ | **152** |
| PHY_I3_A | PHY Identifier Register of Port 3 (A) | 262$_H$ | **153** |
| PHY_I3_B | PHY Identifier Register of Port 3 (B) | 263$_H$ | **154** |
| ANAP3 | Auto Negotiation Advertisement Register of Port 3 | 264$_H$ | **155** |
| ANLPA3 | Auto Negotiation Link Partner Ability Register of Port 3 | 265$_H$ | **156** |
| ANE3 | Auto Negotiation Expansion Register of Port 3 | 266$_H$ | **157** |
| NPT3 | Next Page Transmit Register of Port 3 | 267$_H$ | **158** |
| LPNP3 | Link Partner Next Page Register of Port 3 | 268$_H$ | **159** |
| PHY_C4 | PHY Control Register of Port 4 | 280$_H$ | **150** |
| PHY_S4 | PHY Status Register of Port 4 | 281$_H$ | **152** |
| PHY_I4_A | PHY Identifier Register of Port 4 (A) | 282$_H$ | **153** |
| PHY_I4_B | PHY Identifier Register of Port 4 (B) | 283$_H$ | **154** |
| ANAP4 | Auto Negotiation Advertisement Register of Port 4 | 284$_H$ | **155** |
| ANLPA4 | Auto Negotiation Link Partner Ability Register of Port 4 | 285$_H$ | **156** |
| ANE4 | Auto Negotiation Expansion Register of Port 4 | 286$_H$ | **157** |

**Table 34    Registers Overview** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| NPT4 | Next Page Transmit Register of Port 4 | 287$_H$ | **158** |
| LPNP4 | Link Partner Next Page Register of Port 4 | 288$_H$ | **159** |

The register is addressed wordwise.

**Table 35    Register Access Types**

| Mode | Symbol | Description HW | Description SW |
|---|---|---|---|
| read/write | rw | Register is used as input for the HW | Register is read and writable by SW |
| read | r | Register is written by HW (register between input and output -> one cycle delay) | Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.) |
| Read only | ro | Register is set by HW (register between input and output -> one cycle delay) | SW can only read this register |
| Read virtual | rv | Physically, there is no new register, the input of the signal is connected directly to the address multiplexer. | SW can only read this register |
| Latch high, self clearing | lhsc | Latch high signal at high level, clear on read | SW can read the register |
| Latch low, self clearing | llsc | Latch high signal at low-level, clear on read | SW can read the register |
| Latch high, mask clearing | lhmk | Latch high signal at high level, register cleared with written mask | SW can read the register, with write mask the register can be cleared (1 clears) |
| Latch low, mask clearing | llmk | Latch high signal at low-level, register cleared on read | SW can read the register, with write mask the register can be cleared (1 clears) |
| Interrupt high, self clearing | ihsc | Differentiate the input signal (low->high) register cleared on read | SW can read the register |
| Interrupt low, self clearing | ilsc | Differentiate the input signal (high->low) register cleared on read | SW can read the register |
| Interrupt high, mask clearing | ihmk | Differentiate the input signal (high->low) register cleared with written mask | SW can read the register, with write mask the register can be cleared |
| Interrupt low, mask clearing | ilmk | Differentiate the input signal (low->high) register cleared with written mask | SW can read the register, with write mask the register can be cleared |
| Interrupt enable register | ien | Enables the interrupt source for interrupt generation | SW can read and write this register |
| latch_on_reset | lor | rw register, value is latched after first clock cycle after reset | Register is read and writable by SW |
| Read/write self clearing | rwsc | Register is used as input for the hw, the register will be cleared due to a HW mechanism. | Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW. |

**Table 36    Registers Clock Domains**

| Clock Short Name | Description |
|---|---|
| – | – |

## 5.1 EEPROM Basic Registers

**Signature Register**

| SIG | Offset | Reset Value |
|---|---|---|
| **Signature Register** | **00$_H$** | **4154$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | SIG | | | | | | | |

ro

| Field | Bits | Type | Description |
|---|---|---|---|
| SIG | 15:0 | ro | **Signature** <br> The value must be 4154$_H$ . ADM6996LC/LCX/LHX uses this value to check if the EEPROM is attached. If the value in the EEPROM does not equal to 4154$_H$ , ADM6996LC/LCX/LHX will stop loading the EEPROM even if the EEPROM is attached. ADM6996LC/LCX/LHX will use the default value to initialize. |

**P0 Basic Control Register**

| P0BC | Offset | Reset Value |
|---|---|---|
| **P0 Basic Control Register** | **01$_H$** | **040F$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Res | SELFX_EE | | PVID3_0 | | | | PP | PPE | IPVLAN | PD | OPTE | DA | SA | ANE | FCE |
| rw | rw | | rw | | | | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15 | rw | **Reserved** |
| SELFX_EE | 14 | rw | **Select FX** <br> This bit is used together with the value (p4fx_hw) on the pin **P4FX** during the power on reset to decide if the PHY operates on the fiber mode. This bit is useless in Port 5. Port 0, 1, 2, 3: selfx_ee Description Port 4: {p4fx_hw, selfx_ee} Description <br> 1x$_B$    Port 4: Port 4 will operate in the fiber mode <br> 00$_B$    Port 4: Port 4 will operate in the twisted mode <br> 01$_B$    Port 4: Port 4 will operate in the fiber mode |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| PVID3_0 | 13:10 | rw | **Private VID** <br> See $0028_H$ ~ $002C_H$ to find the other PVID [11:4] |
| PP | 9:8 | rw | **Port Priority** <br> $00_B$    Assign packets to Queue 0 <br> $01_B$    Assign packets to Queue 1 <br> $10_B$    Assign packets to Queue 2 <br> $11_B$    Assign packets to Queue 3 |
| PPE | 7 | rw | **Port Priority Enable** <br> $0_B$    The port priority is disabled <br> $1_B$    The port priority is enabled |
| IPVLAN | 6 | rw | **IP over VLAN PRI** <br> $0_B$    Use the priority bits in the tag header to assign the priority queue <br> $1_B$    Use the IP PRI to assign the priority queue |
| PD | 5 | rw | **Port Disable** <br> $0_B$    Port 0, 1, 2, 3, 4: PHY work s normally. Port 5: Port 5 works normally <br> $1_B$    Port 0, 1, 2, 3, 4. PHY is disabled. Port 5: Port 5 is forced to link down |
| OPTE | 4 | rw | **Output Packet Tagging Enable** <br> $0_B$    Untagged packets are transmitted <br> $1_B$    Tagged packets are transmitted |
| DA | 3 | rw | **Duplex Ability** <br> It is useless in Port 5. <br> $0_B$    Recommend PHY to work in the half duplex mode <br> $1_B$    Recommend PHY to work in the full duplex mode |
| SA | 2 | rw | **Speed Ability** <br> $0_B$    Recommend PHY to work in the 10M mode <br> $1_B$    Recommend PHY to work in the 100M mode |
| ANE | 1 | rw | **Auto Negotiation Enable** <br> $0_B$    Recommend PHY to work without Auto Negotiation <br> $1_B$    Recommend PHY to work with Auto Negotiation, when the value on the pin DUPCOL0 during the power on reset is 1 |
| FCE | 0 | rw | **Flow Control Enable** <br> $0_B$    Recommend MAC to work without Pause or Back Pressure <br> $1_B$    In full duplex, recommend MAC to work with Pause when the value on the TXD0 during the power on reset is 1. In half duplex, recommend MAC to work with Back Pressure when the value on the DUPCOL2 during the power on reset is 1 |

**Similar Registers**

**Table 37**    **Basic Control Registers 1 to 5**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|----------------|-------------|
| P1 | Basic Control Register 1 | $03_H$ | |
| P2 | Basic Control Register 2 | $05_H$ | |
| P3 | Basic Control Register 3 | $07_H$ | |

**Table 37     Basic Control Registers 1 to 5** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| P4 | Basic Control Register 4 | 08$_H$ | |
| P5 | Basic Control Register 5 | 09$_H$ | |

**Reserved Register 0**

**Res0**                                  **Offset**                            **Reset Value**
**Reserved Register 0**                   **02$_H$**                            **0000$_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Res

r
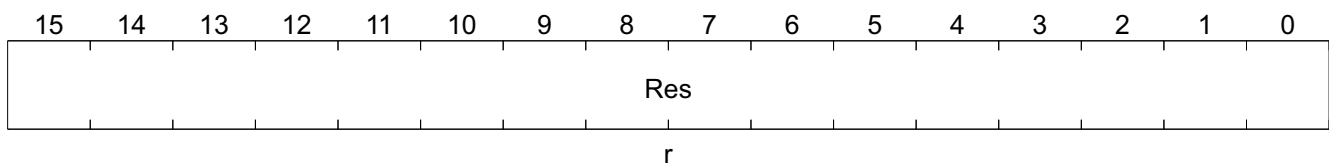
| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15:0 | r | **Reserved** |

**Similar Registers**

**Table 38     Reserved Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| Res1 | Reserved Register 1 | 04$_H$ | |
| Res2 | Reserved Register 2 | 06$_H$ | |
| Res3 | Reserved Register 3 | 0C$_H$ | |
| Res4 | Reserved Register 4 | 0D$_H$ | |
| Res5 | Reserved Register 5 | 23$_H$ | |
| Res6 | Reserved Register 6 | 24$_H$ | |
| Res7 | Reserved Register 7 | 3F$_H$ | |
| Res8 | Reserved Register 8 | 6C$_H$ | |
| Res9 | Reserved Register 9 | 6D$_H$ | |
| Res10 | Reserved Register 10 | 6E$_H$ | |
| Res11 | Reserved Register 11 | 6F$_H$ | |
| Res12 | Reserved Register 12 | 70$_H$ | |
| Res13 | Reserved Register 13 | 71$_H$ | |
| Res14 | Reserved Register 14 | 72$_H$ | |
| Res15 | Reserved Register 15 | 73$_H$ | |
| Res16 | Reserved Register 16 | 74$_H$ | |
| Res17 | Reserved Register 17 | 75$_H$ | |
| Res18 | Reserved Register 18 | 76$_H$ | |
| Res19 | Reserved Register 19 | 77$_H$ | |
| Res20 | Reserved Register 20 | 78$_H$ | |

**Table 38    Reserved Registers** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| Res21 | Reserved Register 21 | 79$_H$ | |
| Res22 | Reserved Register 22 | 7A$_H$ | |
| Res23 | Reserved Register 23 | 7B$_H$ | |
| Res24 | Reserved Register 24 | 7C$_H$ | |
| Res25 | Reserved Register 25 | 7D$_H$ | |
| Res26 | Reserved Register 26 | 7E$_H$ | |
| Res27 | Reserved Register 27 | 7F$_H$ | |
| Res28 | Reserved Register 28 | 80$_H$ | |
| Res29 | Reserved Register 29 | 81$_H$ | |
| Res30 | Reserved Register 30 | 82$_H$ | |
| Res31 | Reserved Register 31 | 83$_H$ | |
| Res32 | Reserved Register 32 | 84$_H$ | |
| Res33 | Reserved Register 33 | 85$_H$ | |
| Res34 | Reserved Register 34 | 86$_H$ | |
| Res35 | Reserved Register 35 | 87$_H$ | |
| Res36 | Reserved Register 36 | 88$_H$ | |
| Res37 | Reserved Register 37 | 89$_H$ | |
| Res38 | Reserved Register 38 | 8A$_H$ | |
| Res39 | Reserved Register 39 | 8B$_H$ | |
| Res40 | Reserved Register 40 | 99$_H$ | |
| Res41 | Reserved Register 41 | 9C$_H$ | |
| Res42 | Reserved Register 42 | A5$_H$ | |
| Res43 | Reserved Register 43 | A6$_H$ | |
| Res44 | Reserved Register 44 | A7$_H$ | |
| Res45 | Reserved Register 45 | 132$_H$ | |
| Res46 | Reserved Register 46 | 133$_H$ | |
| Res47 | Reserved Register 47 | 134$_H$ | |
| Res48 | Reserved Register 48 | 136$_H$ | |
| Res49 | Reserved Register 49 | 137$_H$ | |
| Res50 | Reserved Register 50 | 141$_H$ | |

**System Control Register 0**

**SC0**                              **Offset**                              **Reset Value**
**System Control Register 0**        **0A$_H$**                              **5902$_H$**
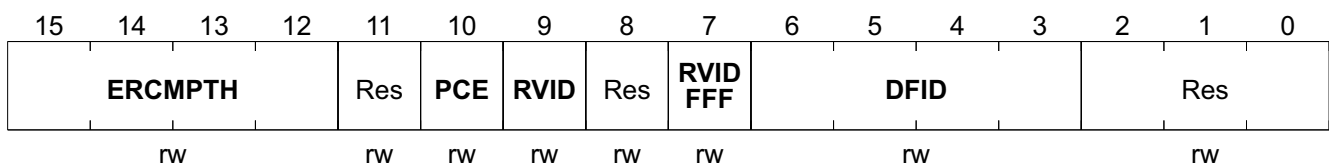
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ERCMPTH | | | | Res | PCE | RVID | Res | RVID FFF | | DFID | | | | Res | |
| | | | | rw | rw | rw | rw | rw | | rw | | | | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| ERCMPTH | 15:12 | rw | **Earlier Cycles for Transmission**<br>It means the earlier cycles for transmission used in ADM6996LC/LCX/LHX. It is for the engineer debug purpose. |
| Res | 11 | rw | **Reserved** |
| PCE | 10 | rw | **Priority Change Enable**<br>$0_B$   Do not change the priority in the tag header<br>$1_B$   Change the priority field in the tag header |
| RVID | 9 | rw | **Replace VID0 and VID1**<br>$0_B$   Do not replace<br>$1_B$   Replace |
| Res | 8 | rw | **Reserved** |
| RVIDFFF | 7 | rw | **Replace VIDFFF**<br>Always Drop |
| DFID | 6:3 | rw | **Default FID**<br>Always $0000_B$ |
| Res | 2:0 | rw | **Reserved** |

**System Control Register 1**

| SC1 | | | | | | | Offset | | | | | | | | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **System Control Register 1** | | | | | | | **$0B_H$** | | | | | | | | **$8001_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DFEFD | IF | | | Res | | | CMS | TE | TSIE | | | Res | | | NE |
| rw | rw | | | rw | | | rw | rw | rw | | | rw | | | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| DFEFD | 15 | rw | **Disable Far-End-Fault Detection**<br>$0_B$   Far-End-Fault detect ion is enabled<br>$1_B$   Far-End-Fault detect ion is disabled |
| IF | 14 | rw | **Input Filter**<br>$0_B$   Discard packets directly when storming or the lack of input buffers<br>$1_B$   Forward packets to the un-congested port when storming or the lack of input buffers |
| Res | 13:9 | rw | **Reserved** |
| CMS | 8 | rw | **Carrier Mask Select**<br>$0_B$   Mask CRS of 4 Cycles<br>$1_B$   Mask CRS of 5 Cycles |
| TE | 7 | rw | **Port 3 and Port 4 Trunk Enable**<br>$0_B$   No trunk is enabled<br>$1_B$   Port 3 and Port 4 are trunked |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| TSIE | 6 | rw | **Transmit Short IPG Enable**<br>$0_B$      96 bits time is used<br>$1_B$      88/96 bits time is used |
| Res | 5:1 | rw | **Reserved** |
| NE | 0 | rw | **New EEPROM**<br>$0_B$      Use old EEPROM functions<br>$1_B$      New EEPROM function is enabled |

**VLAN Priority Map Register**

| VPM | Offset | Reset Value |
|-----|--------|-------------|
| **VLAN Priority Map Register** | $0E_H$ | $FA50_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| PQ7 | | PQ6 | | PQ5 | | PQ4 | | PQ3 | | PQ2 | | PQ1 | | PQ0 | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| PQ7 | 15:14 | rw | **Priority Queue 7**<br>These 2 bits are used as the priority queue when the tagged packets with the user priority = $111_B$ are received on the port.<br>$00_B$    Queue 0<br>$01_B$    Queue 1<br>$10_B$    Queue 2<br>$11_B$    Queue 3 |
| PQ6 | 13:12 | rw | **Priority Queue 6**<br>These 2 bits are used as the priority queue when the tagged packets with the user priority = $110_B$ are received on the port. |
| PQ5 | 11:10 | rw | **Priority Queue 5**<br>These 2 bits are used as the priority queue when the tagged packets with the user priority = $101_B$ are received on the port. |
| PQ4 | 9:8 | rw | **Priority Queue 4**<br>These 2 bits are used as the priority queue when the tagged packets with the user priority = $100_B$ are received on the port. |
| PQ3 | 7:6 | rw | **Priority Queue 3**<br>These 2 bits are used as the priority queue when the tagged packets with the user priority = $011_B$ are received on the port. |
| PQ2 | 5:4 | rw | **Priority Queue 2**<br>These 2 bits are used as the priority queue when the tagged packets with the user priority = $010_B$ are received on the port. |
| PQ1 | 3:2 | rw | **Priority Queue 1**<br>These 2 bits are used as the priority queue when the tagged packets with the user priority = $001_B$ are received on the port. |

| Field | Bits | Type | Description |
|---|---|---|---|
| PQ0 | 1:0 | rw | **Priority Queue 0**<br>These 2 bits are used as the priority queue when the tagged packets with the user priority = $000_B$ are received on the port. |

**TOS Priority Map Register**

| TPM | Offset | Reset Value |
|---|---|---|
| **TOS Priority Map Register** | $0F_H$ | $FA50_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PQ7 | | PQ6 | | PQ5 | | PQ4 | | PQ3 | | PQ2 | | PQ1 | | PQ0 | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| PQ7 | 15:14 | rw | **Priority Queue 7**<br>These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are $111_B$<br>$00_B$ Queue 0<br>$01_B$ Queue 1<br>$10_B$ Queue 2<br>$11_B$ Queue 3 |
| PQ6 | 13:12 | rw | **Priority Queue 6**<br>These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are $110_B$ |
| PQ5 | 11:10 | rw | **Priority Queue 5**<br>These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are $101_B$ |
| PQ4 | 9:8 | rw | **Priority Queue 4**<br>These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are $100_B$ |
| PQ3 | 7:6 | rw | **Priority Queue 3**<br>These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are $011_B$ |
| PQ2 | 5:4 | rw | **Priority Queue 2**<br>These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are $010_B$ |
| PQ1 | 3:2 | rw | **Priority Queue 1**<br>These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are $001_B$ |
| PQ0 | 1:0 | rw | **Priority Queue 0**<br>These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are $000_B$ |

**System Control Register 2**

| SC2 | Offset | Reset Value |
|---|---|---|
| System Control Register 2 | $10_H$ | $0040_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Res | | | | | AD | CC | MP | CCD | BD | SE | ST | |
| | | | rw | | | | | rw | rw | rw | rw | rw | rw | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15:8 | rw | **Reserved** |
| AD | 7 | rw | **Aging Disable**<br>Useless in ADM6996LC/LCX/LHX<br>$0_B$ Age enable<br>$1_B$ Age disable |
| CC | 6 | rw | **Rx Clock Change to Tx Clock for GPSI Interface**<br>$0_B$ ADM6996LC/LCX/LHX does not use Tx clock to replace Rx clock when Rx clock stops.<br>$1_B$ ADM6996LC/LCX/LHX uses Tx clock to replace Rx clock when Rx clock stops |
| MP | 5 | rw | **Multicast Packet Counted into the Storm Counter**<br>$0_B$ Only broadcast packets are counted into the storming counter<br>$1_B$ Multicast and broadcast packets are counted into the storming counter |
| CCD | 4 | rw | **CRC Check Disable**<br>$0_B$ Check CRC<br>$1_B$ Do not check CRC |
| BD | 3 | rw | **Back Off Disable**<br>$0_B$ Back-off is enabled<br>$1_B$ Back-off is disabled |
| SE | 2 | rw | **Storming Enable**<br>It is used in ADM6996L/F style storm control.<br>$0_B$ Disable broadcast/multicast storm protection.<br>$1_B$ Enable boradcast/multicast storm protection. |
| ST | 1:0 | rw | **Storming Threshold[1:0]**<br>It is used in ADM6996L/F style storm control. |

**System Control Register 3**

| SC3 | Offset | Reset Value |
|---|---|---|
| System Control Register 3 | $11_H$ | $E300_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|-----|-----|-----|----|-----|----|----|
| CPN | | | Res | | P | MPL | | | NSE | TBV | MCE | QO | IPI | ATS | |
| rw | | | rw | | rw | rw | | | rw | rw | rw | rw | rw | rw | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| CPN | 15:13 | rw | **CPU Port Number**<br>$000_B$ The CPU is attached to Port 0<br>$001_B$ The CPU is attached to Port 1<br>$010_B$ The CPU is attached to Port 2<br>$011_B$ The CPU is attached to Port 3<br>$100_B$ The CPU is attached to Port 4<br>$101_B$ The CPU is attached to Port 5<br>$111_B$ No CPU exists |
| Res | 12:11 | rw | **Reserved** |
| P | 10 | rw | **Pause**<br>Also add s Speci a l Tag when Special TAG Transmit is enabled .<br>$0_B$ Do not add Special Tag on the PAUSE packets<br>$1_B$ Add Special Tag in the PAUSE packets |
| MPL | 9:7 | rw | **Max Packet Length**<br>$000_B$ 1518 bytes<br>$001_B$ 1536 bytes<br>$010_B$ 1664 bytes<br>$110_B$ 1522 bytes<br>$x11_B$ 1784 bytes<br>$10x_B$ 1784 bytes |
| NSE | 6 | rw | **New Storming Enable**<br>$0_B$ Use the ADM6996L/F style storming control<br>$1_B$ Use the ADM6996LC/LCX/LHX style storming control |
| TBV | 5 | rw | **Tag Base VLAN**<br>$0_B$ Port VLAN<br>$1_B$ Tagged VLAN |
| MCE | 4 | rw | **MAC Clone Enable**<br>$0_B$ MAC Clone is disabled<br>$1_B$ MAC Clone is enabled |
| QO | 3 | rw | **Queue Option**<br>It ' s the test for the designer in the queue control. |
| IPI | 2 | rw | **Interrupt Polarity Inverter**<br>$0_B$ The interrupt signal is active pull low<br>$1_B$ The interrupt signal is active pull high |
| ATS | 1:0 | rw | **Aging Timer Select**<br>$00_B$ 300 Seconds<br>$01_B$ 75 Seconds<br>$10_B$ 18 Seconds<br>$11_B$ 1 Second |

## System Control Register 4

| SC4 | Offset | Reset Value |
|---|---|---|
| **System Control Register 4** | **12$_H$** | **3600$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DP | DCS | Res | | TLE | Res | | O5FL | O4FL | O3FL | PI | O2FL | DUAL_CO* | O1FL | LED ENA* | O0FL |
| rw | rw | rw | | rw | rw | | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| DP | 15 | rw | **Drop Packet When Excessive Collision Happen**<br>0$_B$    Do not drop<br>1$_B$    Drop |
| DCS | 14 | rw | **Duplex and Col Separate**<br>0$_B$    Indicate the duplex and collision status at the same time<br>1$_B$    Indicate the duplex status only |
| Res | 13:12 | rw | **Reserved** |
| TLE | 11 | rw | **Ten Limit Enable**<br>This function works only when Full Flow Control/Half Back Pressure is enabled.<br>0$_B$    The switch will not ignore 10 Mbit/s paths even when the ten limit reaches<br>1$_B$    The switch will forward packets with Multicast, Broadcast, or Unicast but not learned DA addresses from 100 Mbit/s only to 100 Mbit/s ports and ignore the 10M paths when the ten limit reaches. This function allows the switch to balance the high and the low speed |
| Res | 10:9 | rw | **Reserved** |
| O5FL | 8 | rw | **OLD P5 First Lock**<br>0$_B$    First Lock is disabled<br>1$_B$    First Lock is enabled |
| O4FL | 7 | rw | **OLD P4 First Lock**<br>0$_B$    First Lock is disabled<br>1$_B$    First Lock is enabled |
| O3FL | 6 | rw | **OLD P3 First Lock**<br>0$_B$    First Lock is disabled<br>1$_B$    First Lock is enabled |
| PI | 5 | rw | **Pause Ignore**<br>0$_B$    Do not ignore Pause packets<br>1$_B$    Ignore Pause packets in half duplex or in full duplex when flow control is not enabled |
| O2FL | 4 | rw | **OLD P2 First Lock**<br>0$_B$    First Lock is disabled<br>1$_B$    First Lock is enabled |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| DUAL_COLOR_EE | 3 | rw | **Dual Color in MDC / MDIO with CPU**<br>See **Chapter 3.23 LED Display** for more detail information.<br>$0_B$    Single Color<br>$1_B$    Dual Color |
| O1FL | 2 | rw | **OLD P1 First Lock**<br>$0_B$    First Lock is disabled<br>$1_B$    First Lock is enabled |
| LED_ENABLE | 1 | rw | **LED Enable**<br>$0_B$    Disable<br>$1_B$    Enable |
| O0FL | 0 | rw | **OLD P0 First Lock**<br>$0_B$    First Lock is disabled<br>$1_B$    First Lock is enabled |

**Port 0 Security Option**

Port Spanning Tree State and Forward Group Port Map.
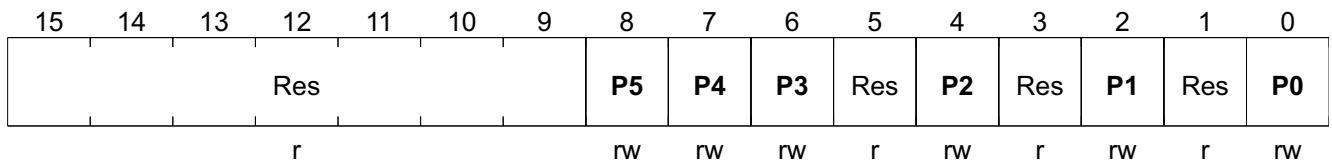
| P0SO | Offset | Reset Value |
|------|--------|-------------|
| Port 0 Security Option | $13_H$ | $01D5_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | Res | | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| | | | r | | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:9 | r | **Reserved** |
| P5 | 8 | rw | **Port 5 is a Member of the Forwarding Group**<br>$0_B$    Port 5 is not a member<br>$1_B$    Port 5 is a member |
| P4 | 7 | rw | **Port 4 is a Member of the Forwarding Group**<br>$0_B$    Port 4 is not a member<br>$1_B$    Port 4 is a member |
| P3 | 6 | rw | **Port 3 is a Member of the Forwarding Group**<br>$0_B$    Port 3 is not a member<br>$1_B$    Port 3 is a member |
| Res | 5 | r | **Reserved** |
| P2 | 4 | rw | **Port 2 is a Member of the Forwarding Group**<br>$0_B$    Port 2 is not a member<br>$1_B$    Port 2 is a member |
| Res | 3 | r | **Reserved** |
| P1 | 2 | rw | **Port 1 is a Member of the Forwarding Group**<br>$0_B$    Port 1 is not a member<br>$1_B$    Port 1 is a member |
| Res | 1 | r | **Reserved** |

| Field | Bits | Type | Description |
|---|---|---|---|
| P0 | 0 | rw | **Port 0 is a Member of the Forwarding Group**<br>$0_B$ Port 0 is not a member<br>$1_B$ Port 0 is a member |

**Similar Registers**

**Table 39 PxSO Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| P1SO | Port 1 Security Option | $14_H$ | |
| P2SO | Port 2 Security Option | $15_H$ | |
| P3SO | Port 3 Security Option | $16_H$ | |
| P4SO | Port 4 Security Option | $17_H$ | |
| P5SO | Port 5 Security Option | $18_H$ | |

**Unicast Port Map andForward Group Port Map**

| UFGPM | Offset | Reset Value |
|---|---|---|
| Unicast Port Map andForward Group Port Map | $19_H$ | $FFD5_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Res | | | | UP | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | | rw | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15 | r | **Reserved** |
| UP | 14:9 | rw | **Unicast Portmap**<br>See **Chapter 3.15.2** Packet Forwarding for more detail information. |
| P5 | 8 | rw | **Port 5 is a Member of the Forwarding Group**<br>$0_B$ Port 5 is not a member<br>$1_B$ Port 5 is a member |
| P4 | 7 | rw | **Port 4 is a Member of the Forwarding Group**<br>$0_B$ Port 4 is not a member<br>$1_B$ Port 4 is a member |
| P3 | 6 | rw | **Port 3 is a Member of the Forwarding Group**<br>$0_B$ Port 3 is not a member<br>$1_B$ Port 3 is a member |
| Res | 5 | r | **Reserved** |
| P2 | 4 | rw | **Port 2 is a Member of the Forwarding Group**<br>$0_B$ Port 2 is not a member<br>$1_B$ Port 2 is a member |
| Res | 3 | r | **Reserved** |

| Field | Bits | Type | Description |
|---|---|---|---|
| P1 | 2 | rw | **Port 1 is a Member of the Forwarding Group**<br>$0_B$     Port 1 is not a member<br>$1_B$     Port 1 is a member |
| Res | 1 | r | **Reserved** |
| P0 | 0 | rw | **Port 0 is a Member of the Forwarding Group**<br>$0_B$     Port 0 is not a member<br>$1_B$     Port 0 is a member |
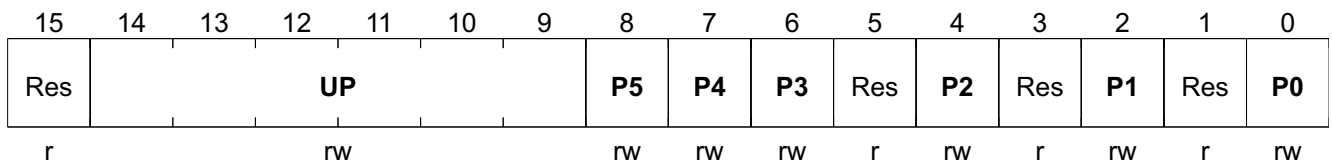
**Broadcast Port Map andForward Group Port Map**

| BFGPM | | Offset | | Reset Value |
|---|---|---|---|---|
| Broadcast Port Map andForward Group Port Map | | $1A_H$ | | $FFD5_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Res | | | BP | | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | rw | | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15 | r | **Reserved** |
| BP | 14:9 | rw | **Broadcast Portmap**<br>Always $111111_B$ |
| P5 | 8 | rw | **Port 5 is a Member of the Forwarding Group**<br>$0_B$     Port 5 is not a member<br>$1_B$     Port 5 is a member |
| P4 | 7 | rw | **Port 4 is a Member of the Forwarding Group**<br>$0_B$     Port 4 is not a member<br>$1_B$     Port 4 is a member |
| P3 | 6 | rw | **Port 3 is a Member of the Forwarding Group**<br>$0_B$     Port 3 is not a member<br>$1_B$     Port 3 is a member |
| Res | 5 | r | **Reserved** |
| P2 | 4 | rw | **Port 2 is a Member of the Forwarding Group**<br>$0_B$     Port 2 is not a member<br>$1_B$     Port 2 is a member |
| Res | 3 | r | **Reserved** |
| P1 | 2 | rw | **Port 1 is a Member of the Forwarding Group**<br>$0_B$     Port 1 is not a member<br>$1_B$     Port 1 is a member |
| Res | 1 | r | **Reserved** |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| P0 | 0 | rw | **Port 0 is a Member of the Forwarding Group**<br>$0_B$    Port 0 is not a member<br>$1_B$    Port 0 is a member |
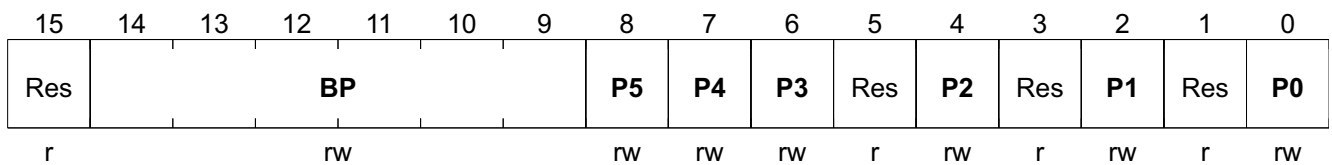
**Multicast Port Map and Forward Group Port Map**

**MFGPM**                                              **Offset**                         **Reset Value**
**Multicast Port Map and Forward Group Port**          $1B_H$                             $FFD5_H$
**Map**
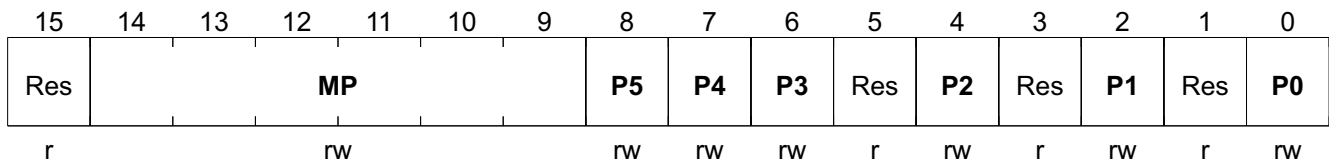
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Res | | | MP | | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | rw | | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15 | r | **Reserved** |
| MP | 14:9 | rw | **Multicast Portmap**<br>Always $111111_B$ |
| P5 | 8 | rw | **Port 5 is a member of the Forwarding Group**<br>$0_B$    Port 5 is not a member<br>$1_B$    Port 5 is a member |
| P4 | 7 | rw | **Port 4 is a member of the Forwarding Group**<br>$0_B$    Port 4 is not a member<br>$1_B$    Port 4 is a member |
| P3 | 6 | rw | **Port 3 is a member of the Forwarding Group**<br>$0_B$    Port 3 is not a member<br>$1_B$    Port 3 is a member |
| Res | 5 | r | **Reserved** |
| P2 | 4 | rw | **Port 2 is a member of the Forwarding Group**<br>$0_B$    Port 2 is not a member<br>$1_B$    Port 2 is a member |
| Res | 3 | r | **Reserved** |
| P1 | 2 | rw | **Port 1 is a member of the Forwarding Group**<br>$0_B$    Port 1 is not a member<br>$1_B$    Port 1 is a member |
| Res | 1 | r | **Reserved** |
| P0 | 0 | rw | **Port 0 is a member of the Forwarding Group**<br>$0_B$    Port 0 is not a member<br>$1_B$    Port 0 is a member |

**Reserve Port Map and Forward Group Port Map**

**RFGPM**             **Offset**             **Reset Value**

**Reserve Port Map and Forward Group Port Map**      $1C_H$           $FFD5_H$
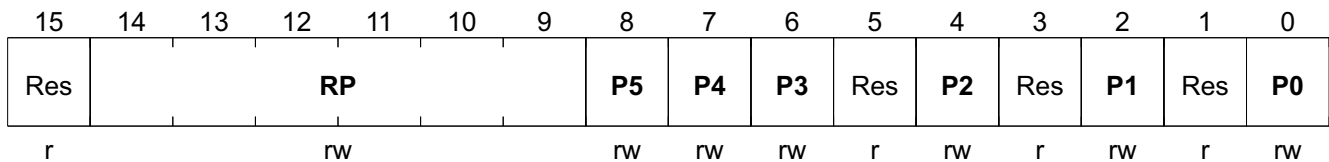
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Res | | | RP | | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | rw | | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15 | r | **Reserved** |
| RP | 14:9 | rw | **Reserve Portmap**<br>Always $111111_B$ |
| P5 | 8 | rw | **Port 5 is a member of the Forwarding Group**<br>$0_B$    Port 5 is not a member<br>$1_B$    Port 5 is a member |
| P4 | 7 | rw | **Port 4 is a member of the Forwarding Group**<br>$0_B$    Port 4 is not a member<br>$1_B$    Port 4 is a member |
| P3 | 6 | rw | **Port 3 is a member of the Forwarding Group**<br>$0_B$    Port 3 is not a member<br>$1_B$    Port 3 is a member |
| Res | 5 | r | **Reserved** |
| P2 | 4 | rw | **Port 2 is a member of the Forwarding Group**<br>$0_B$    Port 2 is not a member<br>$1_B$    Port 2 is a member |
| Res | 3 | r | **Reserved** |
| P1 | 2 | rw | **Port 1 is a member of the Forwarding Group**<br>$0_B$    Port 1 is not a member<br>$1_B$    Port 1 is a member |
| Res | 1 | r | **Reserved** |
| P0 | 0 | rw | **Port 0 is a member of the Forwarding Group**<br>$0_B$    Port 0 is not a member<br>$1_B$    Port 0 is a member |

**Packet Identification Option, Forward Group Port Map**

**PIOFGPM**           **Offset**           **Reset Value**

**Packet Identification Option, Forward Group Port Map**     $1D_H$         $FFD5_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Res | DIVS | DII6P | Res | | DIIP | Res | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| rw | rw | rw | rw | | rw | rw | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15 | rw | **Reserved** |
| DIVS | 14 | rw | **Do not Identify VLAN after SNAP**<br>$0_B$　　Identify<br>$1_B$　　Do not identify |
| DII6P | 13 | rw | **Do not Identify IPV6 in PPPOE**<br>$0_B$　　Identify<br>$1_B$　　Do not identify |
| Res | 12:11 | rw | **Reserved** |
| DIIP | 10 | rw | **Do not Identify IP in PPPOE**<br>$0_B$　　Identify<br>$1_B$　　Do not identify |
| Res | 9 | rw | **Reserved** |
| P5 | 8 | rw | **Port 5 is a member of the Forwarding Group**<br>$0_B$　　Port 5 is not a member<br>$1_B$　　Port 5 is a member |
| P4 | 7 | rw | **Port 4 is a member of the Forwarding Group**<br>$0_B$　　Port 4 is not a member<br>$1_B$　　Port 4 is a member |
| P3 | 6 | rw | **Port 3 is a member of the Forwarding Group**<br>$0_B$　　Port 3 is not a member<br>$1_B$　　Port 3 is a member |
| Res | 5 | r | **Reserved** |
| P2 | 4 | rw | **Port 2 is a member of the Forwarding Group**<br>$0_B$　　Port 2 is not a member<br>$1_B$　　Port 2 is a member |
| Res | 3 | r | **Reserved** |
| P1 | 2 | rw | **Port 1 is a member of the Forwarding Group**<br>$0_B$　　Port 1 is not a member<br>$1_B$　　Port 1 is a member |
| Res | 1 | r | **Reserved** |
| P0 | 0 | rw | **Port 0 is a member of the Forwarding Group**<br>$0_B$　　Port 0 is not a member<br>$1_B$　　Port 0 is a member |

**VLAN Priority Enable and Forward Group Port Map**

**VPEFGPM**            **Offset**            **Reset Value**

**VLAN Priority Enable and Forward Group**    $1E_H$            $FFD5_H$

**Port Map**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|----|
| Res | | | | VPE | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | rw | | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15 | r | **Reserved** |
| VPE | 14:9 | rw | **VLAN Priority Enable**<br>$0_B$     Do not care the PRI in the tag header<br>$1_B$     PRI in the tag header will be taken into priority determination consideration |
| P5 | 8 | rw | **Port 5 is a member of the Forwarding Group**<br>$0_B$     Port 5 is not a member<br>$1_B$     Port 5 is a member |
| P4 | 7 | rw | **Port 4 is a member of the Forwarding Group**<br>$0_B$     Port 4 is not a member<br>$1_B$     Port 4 is a member |
| P3 | 6 | rw | **Port 3 is a member of the Forwarding Group**<br>$0_B$     Port 3 is not a member<br>$1_B$     Port 3 is a member |
| Res | 5 | r | **Reserved** |
| P2 | 4 | rw | **Port 2 is a member of the Forwarding Group**<br>$0_B$     Port 2 is not a member<br>$1_B$     Port 2 is a membe |
| Res | 3 | r | **Reserved** |
| P1 | 2 | rw | **Port 1 is a member of the Forwarding Group**<br>$0_B$     Port 1 is not a member<br>$1_B$     Port 1 is a member |
| Res | 1 | r | **Reserved** |
| P0 | 0 | rw | **Port 0 is a member of the Forwarding Group**<br>$0_B$     Port 0 is not a member<br>$1_B$     Port 0 is a member |

**Service Priority Enable and Forward Group Port Map**

**SPEFGPM**            **Offset**            **Reset Value**

**Service Priority Enable and Forward Group**    $1F_H$            $FFD5_H$

**Port Map**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Res | | | SPE | | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | rw | | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15 | r | **Reserved** |
| SPE | 14:9 | rw | **Service Priority Enable**<br>$0_B$　　Don't care IPV4 TOS /IPV6 Traffic Class<br>$1_B$　　Care IPV4 TOS/IPV6 Traffic for priority decision |
| P5 | 8 | rw | **Port 5 is a member of the Forwarding Group**<br>$0_B$　　Port 5 is not a member<br>$1_B$　　Port 5 is a member |
| P4 | 7 | rw | **Port 4 is a member of the Forwarding Group**<br>$0_B$　　Port 4 is not a member<br>$1_B$　　Port 4 is a member |
| P3 | 6 | rw | **Port 3 is a member of the Forwarding Group**<br>$0_B$　　Port 3 is not a member<br>$1_B$　　Port 3 is a member |
| Res | 5 | r | **Reserved** |
| P2 | 4 | rw | **Port 2 is a member of the Forwarding Group**<br>$0_B$　　Port 2 is not a member<br>$1_B$　　Port 2 is a member |
| Res | 3 | r | **Reserved** |
| P1 | 2 | rw | **Port 1 is a member of the Forwarding Group**<br>$0_B$　　Port 1 is not a member<br>$1_B$　　Port 1 is a member |
| Res | 1 | r | **Reserved** |
| P0 | 0 | rw | **Port 0 is a member of the Forwarding Group**<br>$0_B$　　Port 0 is not a member<br>$1_B$　　Port 0 is a member |

**Input Force No Tag and Forward Group Port Map?**

| **IFNTFGPM** | **Offset** | **Reset Value** |
|---|---|---|
| **Input Force No Tag and Forward Group Port Map** | $20_H$ | $FFD5_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Res | | | IFNTE | | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | rw | | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15 | r | **Reserved** |
| IFNTE | 14:9 | rw | **Input Force No TAG Enable**<br>$0_B$ Disabled<br>$1_B$ Enabled |
| P5 | 8 | rw | **Port 5 is a member of the Forwarding Group**<br>$0_B$ Port 5 is not a member<br>$1_B$ Port 5 is a member |
| P4 | 7 | rw | **Port 4 is a member of the Forwarding Group**<br>$0_B$ Port 4 is not a member<br>$1_B$ Port 4 is a member |
| P3 | 6 | rw | **Port 3 is a member of the Forwarding Group**<br>$0_B$ Port 3 is not a member<br>$1_B$ Port 3 is a member |
| Res | 5 | r | **Reserved** |
| P2 | 4 | rw | **Port 2 is a member of the Forwarding Group**<br>$0_B$ Port 2 is not a member<br>$1_B$ Port 2 is a member |
| Res | 3 | r | **Reserved** |
| P1 | 2 | rw | **Port 1 is a member of the Forwarding Group**<br>$0_B$ Port 1 is not a member<br>$1_B$ Port 1 is a member |
| Res | 1 | r | **Reserved** |
| P0 | 0 | rw | **Port 0 is a member of the Forwarding Group**<br>$0_B$ Port 0 is not a member<br>$1_B$ Port 0 is a member |

**Ingress Filter andForward Group Port Map**

**IFFGPM**     Offset     **Reset Value**
**Ingress Filter andForward Group Port Map**     $21_H$     $FFD5_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Res | | | | IFE | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | | rw | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15 | r | **Reserved** |
| IFE | 14:9 | rw | **Ingress Filter Enable**<br>Always $111111_B$ |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| P5 | 8 | rw | **Port 5 is a member of the Forwarding Group**<br>$0_B$     Port 5 is not a member<br>$1_B$     Port 5 is a member |
| P4 | 7 | rw | **Port 4 is a member of the Forwarding Group**<br>$0_B$     Port 4 is not a member<br>$1_B$     Port 4 is a member |
| P3 | 6 | rw | **Port 3 is a member of the Forwarding Group**<br>$0_B$     Port 3 is not a member<br>$1_B$     Port 3 is a member |
| Res | 5 | r | **Reserved** |
| P2 | 4 | rw | **Port 2 is a member of the Forwarding Group**<br>$0_B$     Port 2 is not a member<br>$1_B$     Port 2 is a member |
| Res | 3 | r | **Reserved** |
| P1 | 2 | rw | **Port 1 is a member of the Forwarding Group**<br>$0_B$     Port 1 is not a member<br>$1_B$     Port 1 is a member |
| Res | 1 | r | **Reserved** |
| P0 | 0 | rw | **Port 0 is a member of the Forwarding Group**<br>$0_B$     Port 0 is not a member<br>$1_B$     Port 0 is a member |

**VLAN Security Disable and Forward Group Port Map**

**VSDFGPM**                                      **Offset**                                      **Reset Value**
**VLAN Security Disable and Forward Group**     $22_H$                                  $FFD5_H$
**Port Map**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Res | | | VSD | | | | P5 | P4 | P3 | Res | P2 | Res | P1 | Res | P0 |
| r | | | rw | | | | rw | rw | rw | r | rw | r | rw | r | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15 | r | **Reserved** |
| VSD | 14:9 | rw | **VLAN Security Disable**<br>Always $111111_B$ |
| P5 | 8 | rw | **Port 5 is a member of the Forwarding Group**<br>$0_B$     Port 5 is not a member<br>$1_B$     Port 5 is a member |
| P4 | 7 | rw | **Port 4 is a member of the Forwarding Group**<br>$0_B$     Port 4 is not a member<br>$1_B$     Port 4 is a member |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| P3 | 6 | rw | **Port 3 is a member of the Forwarding Group**<br>$0_B$     Port 3 is not a member<br>$1_B$     Port 3 is a member |
| Res | 5 | r | **Reserved** |
| P2 | 4 | rw | **Port 2 is a member of the Forwarding Group**<br>$0_B$     Port 2 is not a member<br>$1_B$     Port 2 is a member |
| Res | 3 | r | **Reserved** |
| P1 | 2 | rw | **Port 1 is a member of the Forwarding Group**<br>$0_B$     Port 1 is not a member<br>$1_B$     Port 1 is a member |
| Res | 1 | r | **Reserved** |
| P0 | 0 | rw | **Port 0 is a member of the Forwarding Group**<br>$0_B$     Port 0 is not a member<br>$1_B$     Port 0 is a member |

**IGMP/MLDTRAP Enable and Input Jam Threshold Register**

| IMEIJT | | Offset | | Reset Value |
|--------|--|--------|--|-------------|
| IGMP/MLDTRAP Enable and Input Jam Threshold Register | | $25_H$ | | $1000_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Q1W | | | | Res | | | | | | IJT | | | | | |
| rw | | | | rw | | | | | | rw | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Q1W | 15:12 | rw | **Queue 1 Weight**<br>See **Table 32 Priority Queue Weight Ratio** for more detail information. |
| Res | 11:6 | rw | **Reserved** |
| IJT | 5:0 | rw | **Input Jam Threshold** |
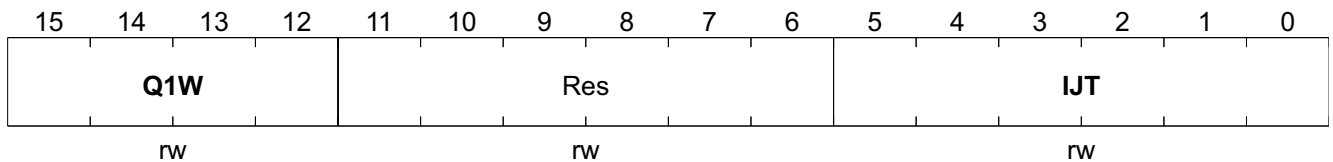
**Queue 2 Weight, VID Exist Check, and PPPOE Port Only**

| Q2WVECPO | | Offset | | Reset Value |
|----------|--|--------|--|-------------|
| Queue 2 Weight, VID Exist Check, and PPPOE Port Only | | $26_H$ | | $1000_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|

| Q2W | | | | VC | | | | | | Res | | | | | |
|-----|--|--|--|----|--|--|--|--|--|-----|--|--|--|--|--|
| rw | | | | rw | | | | | | rw | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Q2W | 15:12 | rw | **Queue 2 Weight** <br> See **Table 32** for more detail information. |
| VC | 11:6 | rw | **VID Check** <br> Always 000000$_B$ |
| Res | 5:0 | rw | **Reserved** |
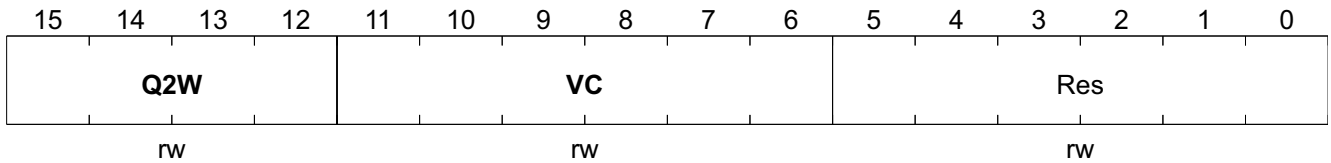
**Queue 3 Weight, Back to Port VLAN, and Admit Only VLAN-Tagged**

**Q3WBPVAO**        **Offset**        **Reset Value**
**Queue 3 Weight, Back to Port VLAN, and**    27$_H$        1000$_H$
**Admit Only VLAN-Tagged**
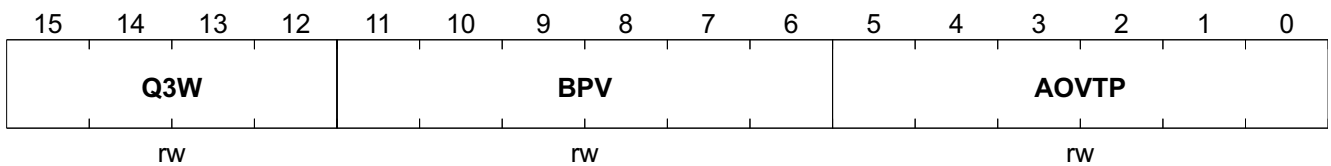
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|

| Q3W | | | | BPV | | | | | | AOVTP | | | | | |
|-----|--|--|--|-----|--|--|--|--|--|-------|--|--|--|--|--|
| rw | | | | rw | | | | | | rw | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Q3W | 15:12 | rw | **Queue 3 Weight** <br> See **Table 32** for more detail information. |
| BPV | 11:6 | rw | **Back To Port VLAN** <br> Always 000000$_B$ |
| AOVTP | 5:0 | rw | **Admit Only VLAN_Tagged Packet** <br> Always 000000$_B$ |

**Input Double Tag Enable, and P0VID[11:4]**

**IDTEP**        **Offset**        **Reset Value**
**Input Double Tag Enable, and P0VID[11:4]**    28$_H$        0000$_H$
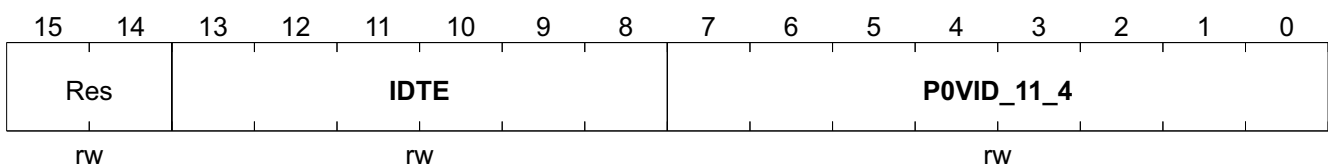
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|

| Res | | IDTE | | | | | | P0VID_11_4 | | | | | | | |
|-----|--|------|--|--|--|--|--|------------|--|--|--|--|--|--|--|
| rw | | rw | | | | | | rw | | | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:14 | rw | **Reserved** |
| IDTE | 13:8 | rw | **Input Double Tag Enable**<br>The register is reserved for internal use only and should be kept 0B |
| P0VID_11_4 | 7:0 | rw | **P0VID[11:4]**<br>VID bit 11 ~ 4 fo Port 0 |

**Output Double Tag Enable, and P1VID[11:4]**

| ODTEP | | Offset | | Reset Value |
|-------|--|--------|--|-------------|
| **Output Double Tag Enable, and P1VID[11:4]** | | **29$_H$** | | **0000$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Res | | | | | | | | P1VID_11_4 | | | | | | | |
| rw | | | | | | | | rw | | | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:8 | rw | **Reserved** |
| P1VID_11_4 | 7:0 | rw | **P1VID[11:4]**<br>VID bit 11 ~ 4 of Port 1. |
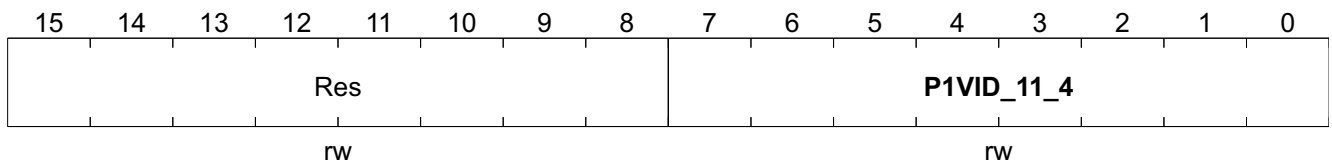
**Output Tag Bypass, and P2VID[11:4]**

| OTBP | | Offset | | Reset Value |
|------|--|--------|--|-------------|
| **Output Tag Bypass, and P2VID[11:4]** | | **2A$_H$** | | **3F00$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Res | | OTBE | | | | | | P2VID_11_4 | | | | | | | |
| rw | | rw | | | | | | rw | | | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:14 | rw | **Reserved** |
| OTBE | 13:8 | rw | **Output Tag Bypass Enable**<br>Always 000000$_B$ |
| P2VID_11_4 | 7:0 | rw | **P2VID[11:4]**<br>VID bit 11 ~ 4 of Port 2. |
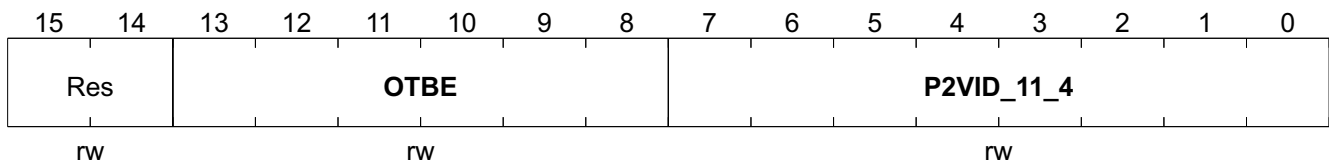
**P3VID[11:4], and P4VID[11:4]**
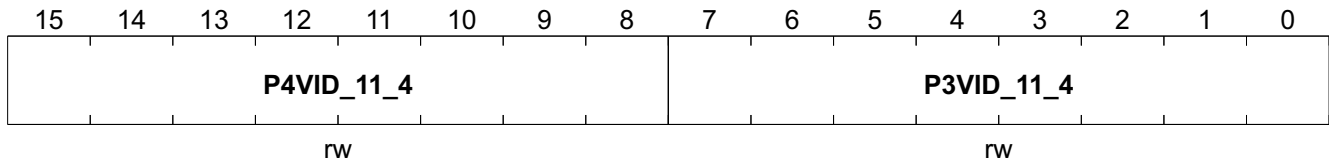
| P11_4 | | Offset | | | | | Reset Value |
|---|---|---|---|---|---|---|---|
| P3VID[11:4], and P4VID[11:4] | | 2B$_H$ | | | | | 0000$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | P4VID_11_4 | | | | | | | | P3VID_11_4 | | | | |
| | | | rw | | | | | | | | rw | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| P4VID_11_4 | 15:8 | rw | **P4VID[11:4]**<br>VID bit 11 ~ 4 of Port 4. |
| P3VID_11_4 | 7:0 | rw | **P3VID[11:4]**<br>VID bit 11 ~ 4 of Port 3. |

**Reserved Address Control, and P5VID[11:4]**
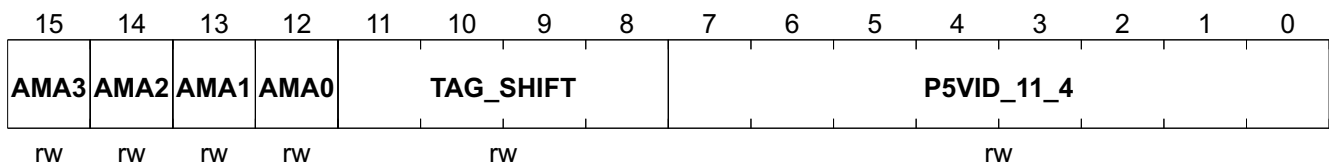
| RACP | | Offset | | | | | Reset Value |
|---|---|---|---|---|---|---|---|
| Reserved Address Control, and P5VID[11:4] | | 2C$_H$ | | | | | D000$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AMA3 | AMA2 | AMA1 | AMA0 | | TAG_SHIFT | | | | | | P5VID_11_4 | | | | |
| rw | rw | rw | rw | | rw | | | | | | rw | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| AMA3 | 15 | rw | **Action of MAC Address 3**<br>The Action of MAC Address = 0180C2000010$_H$ ~ 0180C20000FF$_H$ |
| AMA2 | 14 | rw | **Action of MAC Address 2**<br>The Action of MAC Address = 0180C2000002$_H$ ~ 0180C200000F$_H$ |
| AMA1 | 13 | rw | **Action of MAC Address 1**<br>The Action of MAC Address = 0180C2000001$_H$ |
| AMA0 | 12 | rw | **Action of MAC Address 0**<br>The Action of MAC Address = 0180C2000000$_H$ |
| TAG_SHIFT | 11:8 | rw | **Tag Shift** |
| P5VID_11_4 | 7:0 | rw | **P5VID[11:4]**<br>VID bit 11 ~ 4 of Port 5 |

**PHY Control Register**

**PHYC**              **Offset**             **Reset Value**
**PHY Control Register**             **2D$_H$**             **4442$_H$**
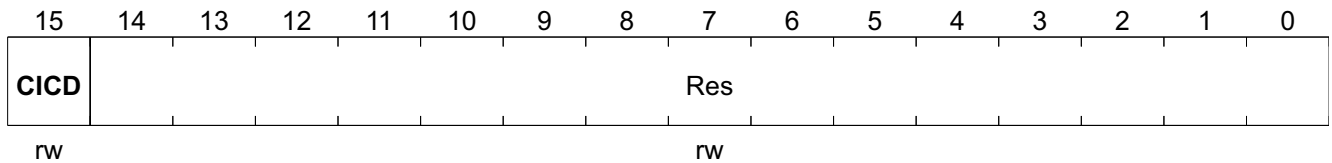
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CICD | | | | | | | | Res | | | | | | | |
| rw | | | | | | | | rw | | | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| CICD | 15 | rw | **Chip ID Check Disable**<br>$0_B$     Check CHIP ID in 32 bit SDC/SDO<br>$1_B$     Do not check CHIP ID in 32 bit SDC/SDIO |
| Res | 14:0 | rw | **Reserved** |

**ADM TAG Ether Type**

**ATET**             **Offset**             **Reset Value**
**ADM TAG Ether Type**             **2E$_H$**             **0000$_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | | | | | | ATET | | | | | | | | |
| | | | | | | | rw | | | | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| ATET | 15:0 | rw | **ADM TAG Ether Type**<br>This value is used by the user to define their Ether-Type. When Special Tag Receive is enabled, ADM6996LC/LCX/LHX checks the packets on the CPU port to see if the two bytes following the SA are the same as ADM TAG Ether Type . If they are different, ADM6996LC/LCX/LHX bypasses the Special Tag. If the same, ADM6996LC/LCX/LHX will use the value in the Special Tag to do switching decisions . |

**PHY Restart Register**

**PR**             **Offset**             **Reset Value**
**PHY Restart Register**             **2F$_H$**             **0000$_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **RESTART** | | | | | | | | |

rw
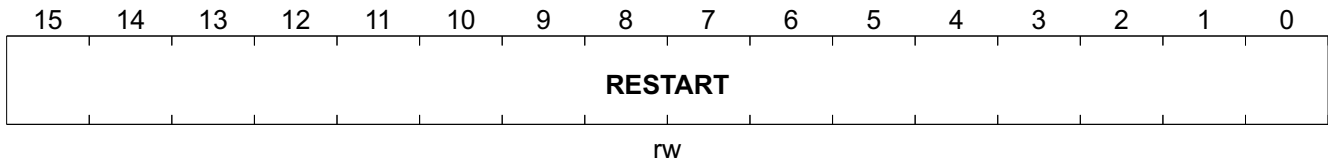
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| RESTART | 15:0 | rw | **Restart**<br>ADM6996LC/LCX/LHX writes this register to restart all the PHYs in the switch. The value written is not important. |

**Miscellaneous Register**
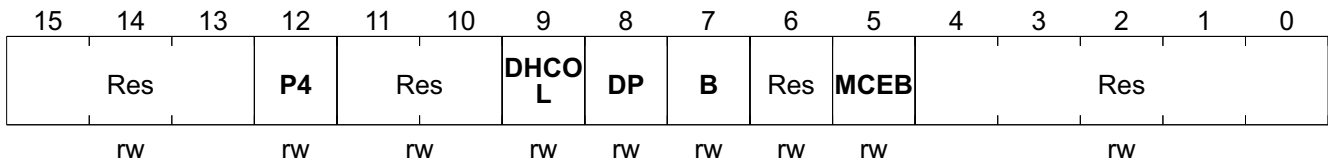
| **MISC** | | **Offset** | | **Reset Value** |
|----------|--|-----------|--|-----------------|
| **Miscellaneous Register** | | $30_H$ | | $0987_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Res | | | **P4** | Res | | **DHCOL** | **DP** | **B** | Res | **MCEB** | Res | | | | |
| rw | | | rw | rw | | rw | rw | rw | rw | rw | rw | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:13 | rw | **Reserved** |
| P4 | 12 | rw | **Port 4 LED Mode**<br>$0_B$   LinkAct/DupCol/Speed.<br>$1_B$   Link/Act/Speed. |
| Res | 11:10 | rw | **Reserved** |
| DHCOL | 9 | rw | **Dual Speed Hub COL_LED Enable**<br>$0_B$   Normal LED display.<br>$1_B$   Dual Speed Hub LED display. Port0 Col LED: 10M Col LED. Port1 Col LED: 100M Col LED. |
| DP | 8 | rw | **Drop Packets**<br>Drop packets when the link partner does not follow the PAUSE protocol.<br>$0_B$   Disable.<br>$1_B$   Enable to drop packets. |
| B | 7 | rw | **BYPASS**<br>Bypass Tag/Untag function.<br>$0_B$   Disable.<br>$1_B$   Enable to bypass Tag/Untag function |
| Res | 6 | rw | **Reserved** |
| MCEB | 5 | rw | **MAC Clone Enable Bits Select**<br>$0_B$   Select 1 bit MAC Clone function.<br>$1_B$   Select 2 bits MAC Clone function. |
| Res | 4:0 | rw | **Reserved** |

**Basic Bandwidth Control Register 0**

| BBC0 | Offset | Reset Value |
|---|---|---|
| Basic Bandwidth Control Register 0 | 31$_H$ | 0000$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R3BW_TH1 | R3BW_TH0 | | | R2BW_TH1 | R2BW_TH0 | | | R1BW_TH1 | R1BW_TH0 | | | R0BW_TH1 | R0BW_TH0 | | |
| rw | rw | | | rw | rw | | | rw | rw | | | rw | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| R3BW_TH1 | 15 | rw | **Port 3 Receive Bandwidth Maximum[3].** See register 0033$_H$, **P3RBCE** for more detail. |
| R3BW_TH0 | 14:12 | rw | **Port 3 Receive Bandwidth Configuration** See register 0033$_H$, **P3RBCE** for more detail. |
| R2BW_TH1 | 11 | rw | **Port 2 Receive Bandwidth Maximum[3].** See register 0033$_H$, **P2RBCE** for more detail. |
| R2BW_TH0 | 10:8 | rw | **Port 2 Receive Bandwidth Configuration** See register 0033$_H$, **P2RBCE** for more detail. |
| R1BW_TH1 | 7 | rw | **Port 1 Receive Bandwidth Maximum[3].** See register 0033$_H$, **P1RBCE** for more detail. |
| R1BW_TH0 | 6:4 | rw | **Port 1 Receive Bandwidth Configuration** See register 0033$_H$, **P1RBCE** for more detail. |
| R0BW_TH1 | 3 | rw | **Port 0 Receive Bandwidth Maximum[3].** See register 0033$_H$, **P0RBCE** for more detail. |
| R0BW_TH0 | 2:0 | rw | **Port 0 Receive Bandwidth Configuration** See register 0033$_H$, **P0RBCE** for more detail. |

**Basic Bandwidth Control Register 1**

| BBC1 | Offset | Reset Value |
|---|---|---|
| Basic Bandwidth Control Register 1 | 32$_H$ | 0000$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| T1BW_TH1 | T1BW_TH0 | | | T0BW_TH1 | T0BW_TH0 | | | R5BW_TH1 | R5BW_TH0 | | | R4BW_TH1 | R4BW_TH0 | | |
| rw | rw | | | rw | rw | | | rw | rw | | | rw | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| T1BW_TH1 | 15 | rw | **Port 1 Transmit Bandwidth Maximum[3].** See register 0033$_H$, **P1TBCE** for more detail. |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| T1BW_TH0 | 14:12 | rw | **Port 1 Transmit Bandwidth Maximum[2:0].** See register 0033$_H$, **P1TBCE** for more detail. |
| T0BW_TH1 | 11 | rw | **Port 0 Transmit Bandwidth Maximum[3].** See register 0033$_H$, **P0TBCE** for more detail. |
| T0BW_TH0 | 10:8 | rw | **Port 0 Transmit Bandwidth Maximum[2:0].** See register 0033$_H$, **P0TBCE** for more detail. |
| R5BW_TH1 | 7 | rw | **Port 5 Receive Bandwidth Maximum[3].** See register 0033$_H$, **P5RBCE** for more detail. |
| R5BW_TH0 | 6:4 | rw | **Port 5 Receive Bandwidth Configuration** See register 0033$_H$, **P5RBCE** for more detail. |
| R4BW_TH1 | 3 | rw | **Port 4 Receive Bandwidth Maximum[3].** See register 0033$_H$, **P4RBCE** for more detail. |
| R4BW_TH0 | 2:0 | rw | **Port 4 Receive Bandwidth Configuration** See register 0033$_H$, **P4RBCE** for more detail. |

**Bandwidth Control Enable Register**

**BCE**                                     **Offset**                              **Reset Value**
**Bandwidth Control Enable Register**        **33$_H$**                              **0000$_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| IPCP | CLC | Res | ANBCE | P5TBCE | P4TBCE | P3TBCE | P5RBCE | P4RBCE | P3RBCE | P2TBCE | P2RBCE | P1TBCE | P1RBCE | P0TBCE | P0RBCE |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| IPCP | 15 | rw | **Invert P4 Clock in PCS** 0$_D$  Disable  1$_D$  Enable |
| CLC | 14 | rw | **Check the Length of CRS** 0$_D$  Enable  1$_D$  Disable |
| Res | 13 | rw | **Reserved** |
| ANBCE | 12 | rw | **ADM6996LC/LCX/LHX New Bandwidth Control Enable** 0$_B$  Disable  1$_B$  Enable |
| P5TBCE | 11 | rw | **Port 5 Transmit Bandwidth Control Enable** The transmit bandwidth is {**T5BW_TH3**, **T5BW_TH2**, **T5BW_TH1**, **T5BW_TH0**, 000000$_B$} kbit/s. K = 1000. 0$_B$  Disable  1$_B$  Enable |

| Field | Bits | Type | Description |
|---|---|---|---|
| P4TBCE | 10 | rw | **Port 4 Transmit Bandwidth Control Enable**<br>The transmit bandwidth is {**T4BW_TH3**, **T4BW_TH2**, **T4BW_TH1**, **T4BW_TH0**, $000000_B$} kbit/s. K = 1000.<br>$0_B$ Disable<br>$1_B$ Enable |
| P3TBCE | 9 | rw | **Port 3 Transmit Bandwidth Control Enable**<br>The transmit bandwidth is {**T3BW_TH3**, **T3BW_TH2**, **T3BW_TH1**, **T3BW_TH0**, $000000_B$} kbit/s. K = 1000.<br>$0_B$ Disable<br>$1_B$ Enable |
| P5RBCE | 8 | rw | **Port 5 Receive Bandwidth Control Enable**<br>The receive bandwidth is {**R5BW_TH3**, **R5BW_TH2**, **R5BW_TH1**, **R5BW_TH0**, $000000_B$} kbit/s. K = 1000.<br>$0_B$ Disable<br>$1_B$ Enable |
| P4RBCE | 7 | rw | **Port 4 Receive Bandwidth Control Enable**<br>The receive bandwidth is {**R4BW_TH3**, **R4BW_TH2**, **R4BW_TH1**, **R4BW_TH0**, $000000_B$} kbit/s. K = 1000.<br>$0_B$ Disable<br>$1_B$ Enable |
| P3RBCE | 6 | rw | **Port 3 Receive Bandwidth Control Enable**<br>The receive bandwidth is {**R3BW_TH3**, **R3BW_TH2**, **R3BW_TH1**, **R3BW_TH0**, $000000_B$} kbit/s. K = 1000.<br>$0_B$ Disable<br>$1_B$ Enable |
| P2TBCE | 5 | rw | **Port 2 Transmit Bandwidth Control Enable**<br>The transmit bandwidth is {**T2BW_TH3**, **T2BW_TH2**, **T2BW_TH1**, **T2BW_TH0**, $000000_B$} kbit/s. K = 1000.<br>$0_B$ Disable<br>$1_B$ Enable |
| P2RBCE | 4 | rw | **Port 2 Receive Bandwidth Control Enable**<br>The receive bandwidth is {**R2BW_TH3**, **R2BW_TH2**, **R2BW_TH1**, **R2BW_TH0**, $000000_B$} kbit/s. K = 1000.<br>$0_B$ Disable<br>$1_B$ Enable |
| P1TBCE | 3 | rw | **Port 1 Transmit Bandwidth Control Enable**<br>The transmit bandwidth is {**T1BW_TH3**, **T1BW_TH2**, **T1BW_TH1**, **T1BW_TH0**, $000000_B$} kbit/s. K = 1000.<br>$0_B$ Disable<br>$1_B$ Enable |
| P1RBCE | 2 | rw | **Port 1 Receive Bandwidth Control Enable**<br>The receive bandwidth is {**R1BW_TH3**, **R1BW_TH2**, **R1BW_TH1**, **R1BW_TH0**, $000000_B$} kbit/s. K = 1000.<br>$0_B$ Disable<br>$1_B$ Enable |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| P0TBCE | 1 | rw | **Port 0 Transmit Bandwidth Control Enable**<br>The transmit bandwidth is {**T0BW_TH3**, **T0BW_TH2**, **T0BW_TH1**, **T0BW_TH0**, $000000_B$} kbit/s. K = 1000.<br>$0_B$   Disable<br>$1_B$   Enable |
| P0RBCE | 0 | rw | **Port 0 Receive Bandwidth Control Enable**<br>The receive bandwidth is {**R0BW_TH3**, **R0BW_TH2**, **R0BW_TH1**, **R0BW_TH0**, $000000_B$} kbit/s. K = 1000.<br>$0_B$   Disable<br>$1_B$   Enable |

**Extended Bandwidth Control Register 0**

| EBC0 | Offset | Reset Value |
|------|--------|-------------|
| Extended Bandwidth Control Register 0 | $34_H$ | $0000_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| T5BW_TH1 | T5BW_TH0 | | | T4BW_TH1 | T4BW_TH0 | | | T3BW_TH1 | T3BW_TH0 | | | T2BW_TH1 | T2BW_TH0 | | |
| rw | rw | | | rw | rw | | | rw | rw | | | rw | rw | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| T5BW_TH1 | 15 | rw | **Port 5 Transmit Bandwidth Maximum[3].**<br>See register $0033_H$, **P5TBCE** for more detail. |
| T5BW_TH0 | 14:12 | rw | **Port 5 Transmit Bandwidth Maximum[2:0].**<br>See register $0033_H$, **P5TBCE** for more detail. |
| T4BW_TH1 | 11 | rw | **Port 4 Transmit Bandwidth Maximum[3].**<br>See register $0033_H$, **P4TBCE** for more detail. |
| T4BW_TH0 | 10:8 | rw | **Port 4 Transmit Bandwidth Maximum[2:0].**<br>See register $0033_H$, **P4TBCE** for more detail. |
| T3BW_TH1 | 7 | rw | **Port 3 Transmit Bandwidth Maximum[3].**<br>See register $0033_H$, **P3TBCE** for more detail. |
| T3BW_TH0 | 6:4 | rw | **Port 3 Transmit Bandwidth Maximum[2:0].**<br>See register $0033_H$, **P3TBCE** for more detail. |
| T2BW_TH1 | 3 | rw | **Port 2 Transmit Bandwidth Maximum[3].**<br>See register $0033_H$, **P2TBCE** for more detail. |
| T2BW_TH0 | 2:0 | rw | **Port 2 Transmit Bandwidth Maximum[2:0].**<br>See register $0033_H$, **P2TBCE** for more detail. |

**Extended Bandwidth Control Register 1**

**EBC1**          **Offset**          **Reset Value**

**Extended Bandwidth Control Register 1**      **35$_H$**          **0000$_H$**
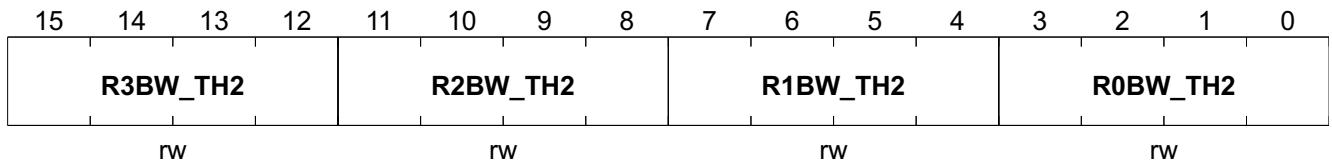
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| R3BW_TH2 | | | | R2BW_TH2 | | | | R1BW_TH2 | | | | R0BW_TH2 | | | |
| rw | | | | rw | | | | rw | | | | rw | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| R3BW_TH2 | 15:12 | rw | **Port 3 Receive Bandwidth Maximum[7:4].** See register 0033$_H$, **P3RBCE** for more detail. |
| R2BW_TH2 | 11:8 | rw | **Port 2 Receive Bandwidth Maximum[7:4].** See register 0033$_H$, **P2RBCE** for more detail. |
| R1BW_TH2 | 7:4 | rw | **Port 1 Receive Bandwidth Maximum[7:4].** See register 0033$_H$, **P1RBCE** for more detail. |
| R0BW_TH2 | 3:0 | rw | **Port 0 Receive Bandwidth Maximum[7:4].** See register 0033$_H$, **P0RBCE** for more detail. |

**Extended Bandwidth Control Register 2**

**EBC2**          **Offset**          **Reset Value**

**Extended Bandwidth Control Register 2**      **36$_H$**          **0000$_H$**
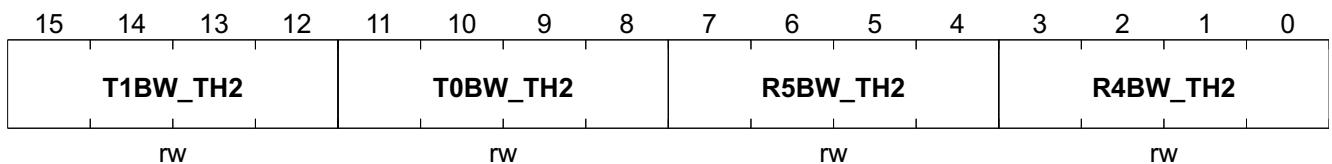
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| T1BW_TH2 | | | | T0BW_TH2 | | | | R5BW_TH2 | | | | R4BW_TH2 | | | |
| rw | | | | rw | | | | rw | | | | rw | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| T1BW_TH2 | 15:12 | rw | **Port 1 Transmit Bandwidth Maximum[7:4]** See register 0033$_H$, **P1TBCE** for more detail. |
| T0BW_TH2 | 11:8 | rw | **Port 0 Transmit Bandwidth Maximum[7:4].** See register 0033$_H$, **P0TBCE** for more detail. |
| R5BW_TH2 | 7:4 | rw | **Port 5 Receive Bandwidth Maximum[7:4].** See register 0033$_H$, **P5RBCE** for more detail. |
| R4BW_TH2 | 3:0 | rw | **Port 4 Receive Bandwidth Maximum[7:4].** See register 0033$_H$, **P4RBCE** for more detail. |

**Extended Bandwidth Control Register 3**

**EBC3**                                    **Offset**                **Reset Value**
**Extended Bandwidth Control Register 3**   **37**$_H$                **0000**$_H$
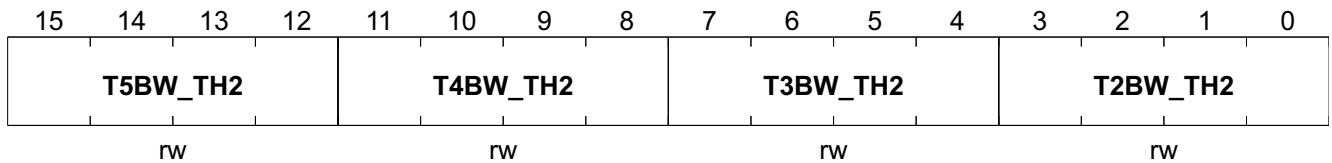
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| T5BW_TH2 | | | | T4BW_TH2 | | | | T3BW_TH2 | | | | T2BW_TH2 | | | |
| rw | | | | rw | | | | rw | | | | rw | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| T5BW_TH2 | 15:12 | rw | **Port 5 Transmit Bandwidth Maximum[7:4].** See register 0033$_H$, **P5TBCE** for more detail. |
| T4BW_TH2 | 11:8 | rw | **Port 4 Transmit Bandwidth Maximum[7:4].** See register 0033$_H$, **P4TBCE** for more detail. |
| T3BW_TH2 | 7:4 | rw | **Port 3 Transmit Bandwidth Maximum[7:4].** See register 0033$_H$, **P3TBCE** for more detail. |
| T2BW_TH2 | 3:0 | rw | **Port 2 Transmit Bandwidth Maximum[7:4].** See register 0033$_H$, **P2TBCE** for more detail. |

**Extended Bandwidth Control Register 4**

**EBC4**                                    **Offset**                **Reset Value**
**Extended Bandwidth Control Register 4**   **38**$_H$                **0000**$_H$
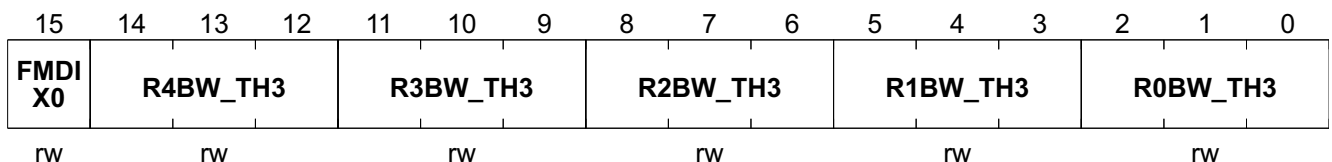
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FMDIX0 | R4BW_TH3 | | | R3BW_TH3 | | | R2BW_TH3 | | | R1BW_TH3 | | | R0BW_TH3 | | |
| rw | rw | | | rw | | | rw | | | rw | | | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| FMDIX0 | 15 | rw | **Port 0 MDIX Control** This bit can be used for Port 0 MDI/MDIX selection. It is useful when Port 0 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. $0_B$    Using MDI $1_B$    Using MDIX |
| R4BW_TH3 | 14:12 | rw | **Port 4 Receive Bandwidth Maximum[10:8].** See register 0033$_H$, **P4RBCE** for more detail. |
| R3BW_TH3 | 11:9 | rw | **Port 3 Receive Bandwidth Maximum[10:8].** See register 0033$_H$, **P3RBCE** for more detail. |
| R2BW_TH3 | 8:6 | rw | **Port 2 Receive Bandwidth Maximum[10:8].** See register 0033$_H$, **P2RBCE** for more detail. |
| R1BW_TH3 | 5:3 | rw | **Port 1 Receive Bandwidth Maximum[10:8].** See register 0033$_H$, **P1RBCE** for more detail. |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| R0BW_TH3 | 2:0 | rw | **Port 0 Receive Bandwidth Maximum[10:8].**<br>See register 0033$_H$, **P0RBCE** for more detail. |

**Extended Bandwidth Control Register 5**

**EBC5**                        **Offset**                  **Reset Value**
**Extended Bandwidth Control Register 5**      **39$_H$**                 **0000$_H$**
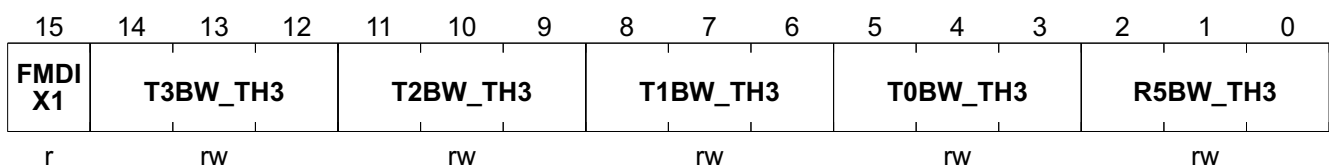
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| FMDIX1 | T3BW_TH3 | | | T2BW_TH3 | | | T1BW_TH3 | | | T0BW_TH3 | | | R5BW_TH3 | | |
| r | rw | | | rw | | | rw | | | rw | | | rw | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| FMDIX1 | 15 | r | **Port 1 MDIX Control**<br>This bit can be used for Port 1 MDI/MDIX selection. It is useful when Port 1 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used.<br>0$_B$      Using MDI<br>1$_B$      Using MDIX |
| T3BW_TH3 | 14:12 | rw | **Port 3 Transmit Bandwidth Maximum[10:8].**<br>See register 0033$_H$, **P3TBCE** for more detail. |
| T2BW_TH3 | 11:9 | rw | **Port 2 Transmit Bandwidth Maximum[10:8].**<br>See register 0033$_H$, **P2TBCE** for more detail. |
| T1BW_TH3 | 8:6 | rw | **Port 1 Transmit Bandwidth Maximum[10:8].**<br>See register 0033$_H$, **P1TBCE** for more detail. |
| T0BW_TH3 | 5:3 | rw | **Port 0 Transmit Bandwidth Maximum[10:8].**<br>See register 0033$_H$, **P0TBCE** for more detail. |
| R5BW_TH3 | 2:0 | rw | **Port 5 Receive Bandwidth Maximum[10:8].**<br>See register 0033$_H$, **P5RBCE** for more detail. |

**Default VLAN Member and Extended Bandwidth Control Register 6**

**DVMEBC6**                     **Offset**                  **Reset Value**
**Default VLAN Member and Extended**        **3A$_H$**                 **0FC0$_H$**
**Bandwidth Control Register 6**
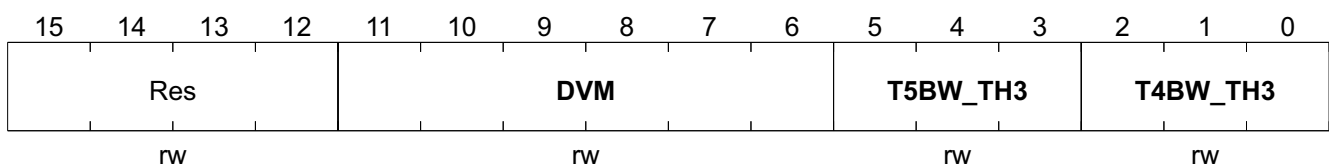
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Res | | | | DVM | | | | | | T5BW_TH3 | | | T4BW_TH3 | | |
| rw | | | | rw | | | | | | rw | | | rw | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15:12 | rw | **Reserved** |
| DVM | 11:6 | rw | **Default VLAN Member** <br> Always 111111$_B$ |
| T5BW_TH3 | 5:3 | rw | **Port 5 Transmit Bandwidth Maximum[10:8].** <br> See register 0033$_H$, **P5TBCE** for more detail. |
| T4BW_TH3 | 2:0 | rw | **Port 4 Transmit Bandwidth Maximum[10:8].** <br> See register 0033$_H$, **P4TBCE** for more detail. |

**New Storm Register 0**

| NS0 | Offset | Reset Value |
|---|---|---|
| New Storm Register 0 | 3B$_H$ | 0000$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Res | STOR M_D* | STOR M_EN | STORM_100_TH | | | | | | | | | | | | |
| r | rw | rw | rw | | | | | | | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15 | r | **Reserved** |
| STORM_DRO P_EN | 14 | rw | **Storm Drop Enable** <br> 0$_B$   Do not drop in the storming period <br> 1$_B$   Drop in the storming period |
| STORM_EN | 13 | rw | **Storm Enable** <br> 0$_B$   Disable ADM6996LC/LCX/LHX style broadcast storm protection <br> 1$_B$   Enable ADM6996LC/LCX/LHX style broadcast storm protection |
| STORM_100_ TH | 12:0 | rw | **100M Threshold** <br> See **Table 31** for more detail information. It is used when all ports link up in the 100M. The upper bound is reached when the number of the packets received during the 50 ms is over 100M Threshold. |

**New Storm Register 1**
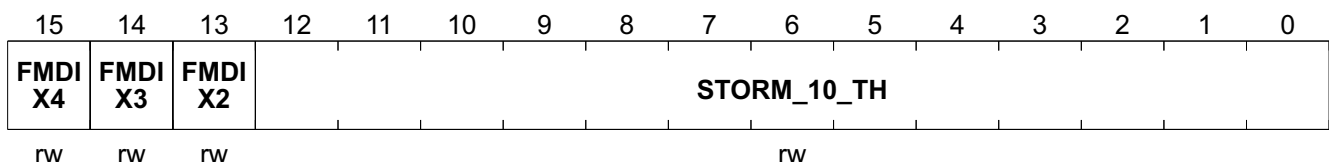
| NS1 | Offset | Reset Value |
|---|---|---|
| New Storm Register 1 | 3C$_H$ | 0000$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FMDI X4 | FMDI X3 | FMDI X2 | STORM_10_TH | | | | | | | | | | | | |
| rw | rw | rw | rw | | | | | | | | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| FMDIX4 | 15 | rw | **Port 4 MDIX Control**<br>This bit can be used for Port 4 MDI/MDIX selection. It is useful when Port 4 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used.<br>$0_B$     Using MDI<br>$1_B$     Using MDIX |
| FMDIX3 | 14 | rw | **Port 3 MDIX Control**<br>This bit can be used for Port 3 MDI/MDIX selection. It is useful when Port 3 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used.<br>$0_B$     Using MDI<br>$1_B$     Using MDIX |
| FMDIX2 | 13 | rw | **Port 2 MDIX Control**<br>This bit can be used for Port 2 MDI/MDIX selection. It is useful when Port 2 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used.<br>$0_B$     Using MDI<br>$1_B$     Using MDIX |
| STORM_10_TH | 12:0 | rw | **10M Threshold**<br>See **Table 31** for more detail information. It is used when one of ports link up in the 10M. The upper bound is reached when the number of the packets received during the 50 ms is over 10M Threshold. |

**New Reserve Address Control Register 0**

| NRAC0 | Offset | Reset Value |
|-------|--------|-------------|
| New Reserve Address Control Register 0 | $3D_H$ | $00FD_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| NRTB | | PG | | PRI_S | | PRI_B | | R3PP | R2PP | GPP | R1PP | R0PP | PPP | SPP | BPP |
| rw | | rw | | rw | | rw | | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| NRTB | 15:14 | rw | **New Reserve TXTAG for BPDU**<br>$00_B$     System Default Tag<br>$01_B$     Unmodified<br>$10_B$     Always Tagged<br>$11_B$     Always Untagged |
| PG | 13:12 | rw | **PRI for GXRP**<br>$00_B$     Queue 0<br>$01_B$     Queue 1<br>$10_B$     Queue 2<br>$11_B$     Queue 3 |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| PRI_S | 11:10 | rw | **PRI for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3**<br>$00_B$   Queue 0<br>$01_B$   Queue 1<br>$10_B$   Queue 2<br>$11_B$   Queue 3 |
| PRI_B | 9:8 | rw | **PRI for BPDU**<br>$00_B$   Queue 0<br>$01_B$   Queue 1<br>$10_B$   Queue 2<br>$11_B$   Queue 3 |
| R3PP | 7 | rw | **RESER_R3 Pass Portmap**<br>$0_B$   RESER_R3 Pass Portmap is $000000_B$<br>$1_B$   RESER_R3 Pass Pormap is $111111_B$ |
| R2PP | 6 | rw | **RESER_R2 Pass Portmap**<br>$0_B$   RESER_R2 Pass Portmap is $000000_B$<br>$1_B$   RESER_R2 Pass Pormap is $111111_B$ |
| GPP | 5 | rw | **GXRP Pass Portmap**<br>$0_B$   GXRP Pass Portmap is $000000_B$<br>$1_B$   GXRP Pass Pormpap is $111111_B$ |
| R1PP | 4 | rw | **RESER_R1 Pass Portmap**<br>$0_B$   RESER_R1 Pass Portmap is $000000_B$<br>$1_B$   RESER_R1 Pass Portmap is $111111_B$ |
| R0PP | 3 | rw | **RESER_R0 Pass Portmap**<br>$0_B$   RESER_R0 Pass Portmap is $000000_B$<br>$1_B$   RESER_R0 Pass Portmap is $111111_B$ |
| PPP | 2 | rw | **PAE Pass Portmap**<br>$0_B$   PAE Pass Portmap is $000000_B$<br>$1_B$   PAE Pass Portpap is $111111_B$ |
| SPP | 1 | rw | **Slow Pass Portmap**<br>$0_B$   SLOW Pass Portmap is $000000_B$<br>$1_B$   SLOW Pass Portpap is $111111_B$ |
| BPP | 0 | rw | **BPDU Pass Portmap**<br>$0_B$   BPDU Pass Portmap is $000000_B$<br>$1_B$   BPDU Pass Portpap is $111111_B$ |

**New Reserve Address Control Register 1**

| NRAC1 | | Offset | | Reset Value |
|-------|--|--------|--|-------------|
| **New Reserve Address Control Register 1** | | $3E_H$ | | $0000_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Res | | | NRMG | NRMS | MRMB | NRSG | NRSS | NRSB | NRCG | NRCS | NRCB | NRTG | | NRTS | |
| | | | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15:13 | rw | **Reserved** |
| NRMG | 12 | rw | **New Reserve Management for GXRP**<br>$0_B$ Do not identify as management packets<br>$1_B$ Identify as management packets |
| NRMS | 11 | rw | **New Reserve Management for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3**<br>$0_B$ Do not identify as management packets<br>$1_B$ Identify as management packets |
| MRMB | 10 | rw | **New Reserve Management for BPDU**<br>$0_B$ Do not identify as management packets<br>$1_B$ Identify as management packets |
| NRSG | 9 | rw | **New Reserve Span.for GXRP**<br>$0_B$ Do not identify as management packets<br>$1_B$ Identify as management packets |
| NRSS | 8 | rw | **New Reserve Span for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3**<br>$0_B$ Do not identify as span packets<br>$1_B$ Identify as span packets |
| NRSB | 7 | rw | **New Reserve SPAN for BPDU**<br>$0_B$ Do not identify as span packets<br>$1_B$ Identify as span packets |
| NRCG | 6 | rw | **New Reserve Cross_VLAN for GXRP**<br>$0_B$ Follow VLAN<br>$1_B$ Cross VLAN |
| NRCS | 5 | rw | **New Reserve Cross_VLAN. for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3**<br>$0_B$ Follow VLAN<br>$1_B$ Cross VLAN |
| NRCB | 4 | rw | **New Reserve Cross_VLAN for BPDU**<br>$0_B$ Follow VLAN<br>$1_B$ Cross VLAN |
| NRTG | 3:2 | rw | **New Reserve TXTAG for GXRP**<br>$00_B$ System Default Tag<br>$01_B$ Unmodified<br>$10_B$ Always Tagged<br>$11_B$ Always Untagged |
| NRTS | 1:0 | rw | **New Reserve TXTAG for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3**<br>$00_B$ System Default Tag<br>$01_B$ Unmodified<br>$10_B$ Always Tagged<br>$11_B$ Always Untagged |

## 5.2 EEPROM Extended Registers

**VLAN Filter 0 Low**

| VF0L | Offset | Reset Value |
|---|---|---|
| VLAN Filter 0 Low | 40$_H$ | 003F$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | FID | | | | | TM | | | | | | M | | | |
| | rw | | | | | rw | | | | | | rw | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| FID | 15:12 | rw | **FID** <br> The forwarding or learning group that the VID is assigned. |
| TM | 11:6 | rw | **Tagged Member** <br> These bits indicate which ports associated with the VID should transmit tagged packets.Tagged Member[x] Description. <br> 0$_B$      Port x should transmit untagged packets <br> 1$_B$      Port x should transmit tagged packets |
| M | 5:0 | rw | **Member** <br> These bits indicate which ports are the members of the VLAN.Member[x] Description. <br> 0$_B$      Port x is not a VLAN member <br> 1$_B$      Port x is a VLAN member |
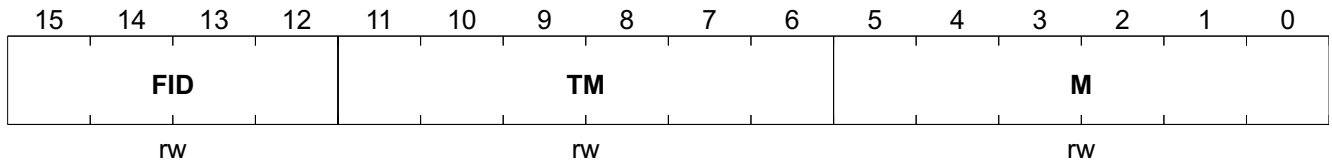
**Similar Registers**

**Table 40     VFxL Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| VF1L | VLAN Filter 1 Low | 42$_H$ | |
| VF2L | VLAN Filter 2 Low | 44$_H$ | |
| VF3L | VLAN Filter 3Low | 46$_H$ | |
| VF4L | VLAN Filter 4 Low | 48$_H$ | |
| VF5L | VLAN Filter 5 Low | 4A$_H$ | |
| VF6L | VLAN Filter 6 Low | 4C$_H$ | |
| VF7L | VLAN Filter 7 Low | 4E$_H$ | |
| VF8L | VLAN Filter 8 Low | 50$_H$ | |
| VF9L | VLAN Filter 9 Low | 52$_H$ | |
| VF10L | VLAN Filter 10 Low | 54$_H$ | |
| VF11L | VLAN Filter 11 Low | 56$_H$ | |
| VF12L | VLAN Filter 12 Low | 58$_H$ | |
| VF13L | VLAN Filter 13 Low | 5A$_H$ | |
| VF14L | VLAN Filter 14 Low | 5C$_H$ | |
| VF15L | VLAN Filter 15 Low | 5E$_H$ | |

**VLAN Filter 0 High**

| VF0H | Offset | Reset Value |
|---|---|---|
| VLAN Filter 0 High | 41$_H$ | 8001$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| VV | | VP | | VID | | | | | | | | | | | |
| rw | | rw | | | | | | | rw | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| VV | 15 | rw | **VLAN_Valid**<br>0$_B$    VLAN filter is not valid<br>1$_B$    VLAN Filter is valid |
| VP | 14:12 | rw | **VLAN PRI**<br>It indicates the VLAN priority associated with VID. |
| VID | 11:0 | rw | **VID**<br>It indicates the VLAN ID that is associated with FID, Tagged Member, Member and VLAN PRI. |

**Similar Registers**

All VFxH registers have the same structure and characteristics, see **VF0H**.
The offset addresses of the other VFxH registers are listed in **Table 41**.

**Table 41    VFxH Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| VF1H | VLAN Filter 1 High | 43$_H$ | |
| VF2H | VLAN Filter 2 High | 45$_H$ | |
| VF3H | VLAN Filter 3 High | 47$_H$ | |
| VF4H | VLAN Filter 4 High | 49$_H$ | |
| VF5H | VLAN Filter 5 High | 4B$_H$ | |
| VF6H | VLAN Filter 6 High | 4D$_H$ | |
| VF7H | VLAN Filter 7 High | 4F$_H$ | |
| VF8H | VLAN Filter 8 High | 51$_H$ | |
| VF9H | VLAN Filter 9 High | 53$_H$ | |
| VF10H | VLAN Filter 10 High | 55$_H$ | |
| VF11H | VLAN Filter 11 High | 57$_H$ | |
| VF12H | VLAN Filter 12 High | 59$_H$ | |
| VF13H | VLAN Filter 13 High | 5B$_H$ | |
| VF14H | VLAN Filter 14 High | 5D$_H$ | |
| VF15H | VLAN Filter 15 High | 5F$_H$ | |

**Type Filter 0**

| TF0 | Offset | Reset Value |
|---|---|---|
| Type Filter 0 | 60$_H$ | 0000$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | VC | ET | | | | | | | |

rw

| Field | Bits | Type | Description |
|---|---|---|---|
| VCET | 15:0 | rw | **Value Compared with Ether-Type** |

**Similar Registers**

All TFx registers have the same structure and characteristics, see **TF0**.
The offset addresses of the other TFx registers are listed in **Table 42**.

**Table 42    TFx Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| TF1 | Type Filter 1 | 61$_H$ | |
| TF2 | Type Filter 2 | 62$_H$ | |
| TF3 | Type Filter 3 | 63$_H$ | |
| TF4 | Type Filter 4 | 64$_H$ | |
| TF5 | Type Filter 5 | 65$_H$ | |
| TF6 | Type Filter 6 | 66$_H$ | |
| TF7 | Type Filter 7 | 67$_H$ | |

**Protocol Filter 1 and 0**

| PF_1_0 | Offset | Reset Value |
|---|---|---|
| Protocol Filter 1 and 0 | 68$_H$ | 0000$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | PF | R1 | | | | | | | PF | R0 | | | |

rw                                              rw
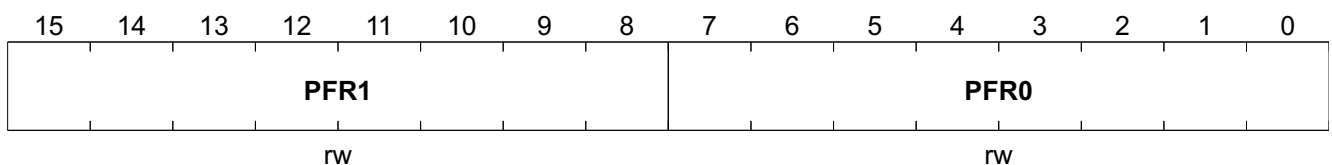
| Field | Bits | Type | Description |
|---|---|---|---|
| PFR1 | 15:8 | rw | **Value Compared with Protocol in IP Header**<br>(Protocol Filter 1, 3, 5, 7) |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| PFR0 | 7:0 | rw | **Value Compared with Protocol in IP Header**<br>(Protocol Filter 0, 2, 4, 6) |

**Similar Registers**

All PFx registers have the same structure and characteristics, see **PF_1_0**.
The offset addresses of the other PFx registers are listed in **Table 43**.

**Table 43      PFx Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|----------------|-------------|
| PF_3_2 | Protocol Filter 3 and 2 | $68_H$ | |
| PF_5_4 | Protocol Filter 5 and 4 | $69_H$ | |
| PF_7_6 | Protocol Filter 7 and 6 | $6A_H$ | |

**TCP/UDP Filter 0**

| **TUF0** | **Offset** | **Reset Value** |
|----------|-----------|-----------------|
| **TCP/UDP Filter 0** | **$8C_H$** | **$0000_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | VAL_COMP | | | | | | | | |

rw

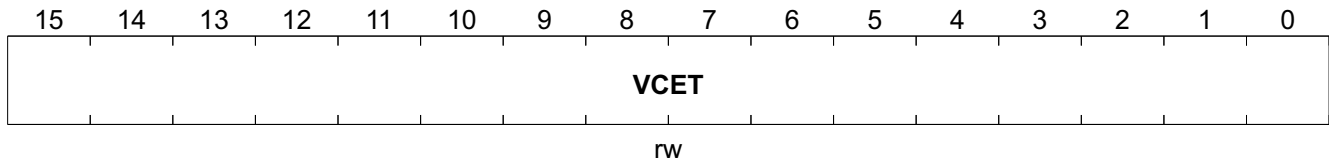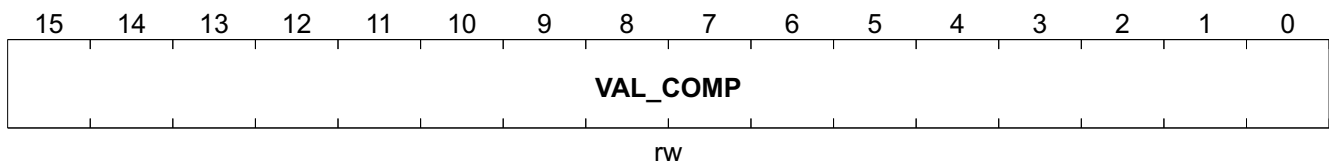| Field | Bits | Type | Description |
|-------|------|------|-------------|
| VAL_COMP | 15:0 | rw | **Value Compared with the Destination Port Number in the TCP/UDP Header** |

**Similar Registers**

All TUFx registers have the same structure and characteristics, see **TUF0**.
The offset addresses of the other TUFx registers are listed in **Table 46**.

**Table 44      TUFx Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|----------------|-------------|
| TUF1 | TCP/UDP Filter 1 | $8D_H$ | |
| TUF2 | TCP/UDP Filter 2 | $8E_H$ | |
| TUF3 | TCP/UDP Filter 3 | $8F_H$ | |
| TUF4 | TCP/UDP Filter 4 | $90_H$ | |
| TUF5 | TCP/UDP Filter 5 | $91_H$ | |
| TUF6 | TCP/UDP Filter 6 | $92_H$ | |
| TUF7 | TCP/UDP Filter 7 | $93_H$ | |

**Type Filter Action**

| TFA | Offset | Reset Value |
|-----|--------|-------------|
| Type Filter Action | 94$_H$ | 0000$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ATF7 | | ATF6 | | ATF5 | | ATF4 | | ATF3 | | ATF2 | | ATF1 | | ATF0 | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| ATF7 | 15:14 | rw | **Action for Type Filter 7**<br>See register 0094$_H$, **ATF0** for more detail. |
| ATF6 | 13:12 | rw | **Action for Type Filter 6**<br>See register 0094$_H$, **ATF0** for more detail. |
| ATF5 | 11:10 | rw | **Action for Type Filter 5**<br>See register 0094$_H$, **ATF0** for more detail. |
| ATF4 | 9:8 | rw | **Action for Type Filter 4**<br>See register 0094$_H$, **ATF0** for more detail. |
| ATF3 | 7:6 | rw | **Action for Type Filter 3**<br>See register 0094$_H$, **ATF0** for more detail. |
| ATF2 | 5:4 | rw | **Action for Type Filter 2**<br>See register 0094$_H$, **ATF0** for more detail. |
| ATF1 | 3:2 | rw | **Action for Type Filter 1**<br>See register 0094$_H$, **ATF0** for more detail. |
| ATF0 | 1:0 | rw | **Action for Type Filter 0**<br>00$_B$　　Type Portmap is Default Output Ports<br>01$_B$　　Type Portmap is 000000$_B$<br>10$_B$　　Type Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Type Portmap contains Defa ult Output Ports , excluding the CPU port<br>11$_B$　　Type Portmap contains Defa ult Output Ports , excluding the CPU port |

**Protocol Filter Action**

| PFA | Offset | Reset Value |
|-----|--------|-------------|
| Protocol Filter Action | 95$_H$ | 0000$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| APF7 | | APF6 | | APF5 | | APF4 | | APF3 | | APF2 | | APF1 | | APF0 | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| APF7 | 15:14 | rw | **Action for Protocol Filter 7**<br>See register 0095$_H$, **APF0** for more detail. |
| APF6 | 13:12 | rw | **Action for Protocol Filter 6**<br>See register 0095$_H$, **APF0** for more detail. |
| APF5 | 11:10 | rw | **Action for Protocol Filter 5**<br>See register 0095$_H$, **APF0** for more detail. |
| APF4 | 9:8 | rw | **Action for Protocol Filter 4**<br>See register 0095$_H$, **APF0** for more detail. |
| APF3 | 7:6 | rw | **Action for Protocol Filter 3**<br>See register 0095$_H$, **APF0** for more detail. |
| APF2 | 5:4 | rw | **Action for Protocol Filter 2**<br>See register 0095$_H$, **APF0** for more detail. |
| APF1 | 3:2 | rw | **Action for Protocol Filter 1**<br>See register 0095$_H$, **APF0** for more detail. |
| APF0 | 1:0 | rw | **Action for Protocol Filter 0**<br>$00_B$  Protocol Portmap is Default Output Ports<br>$01_B$  Protocol Portmap is $000000_B$<br>$10_B$  Protocol Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Type Portmap contains Defa ult Output Ports , excluding the CPU port<br>$11_B$  Protocol Portmap contains Defa ult Output Ports , excluding the CPU port |

**TCP/UDP Action 0**
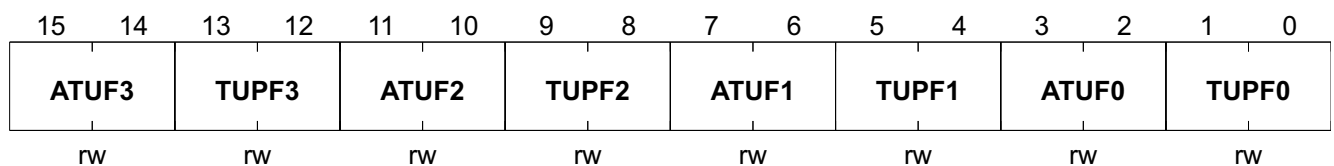
| TUA0 | Offset | Reset Value |
|------|--------|-------------|
| **TCP/UDP Action 0** | **96$_H$** | **0000$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ATUF3 | | TUPF3 | | ATUF2 | | TUPF2 | | ATUF1 | | TUPF1 | | ATUF0 | | TUPF0 | |

| ATUF3 | TUPF3 | ATUF2 | TUPF2 | ATUF1 | TUPF1 | ATUF0 | TUPF0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| ATUF3 | 15:14 | rw | **Action for TCP/UDP Filter 3.**<br>See register 0096$_H$, **ATUF0** for more detail. |
| TUPF3 | 13:12 | rw | **TCP/UDP PRI for TCP/UDP Filter 3**<br>See register 0096$_H$, **TUPF0** for more detail. |
| ATUF2 | 11:10 | rw | **Action for TCP/UDP Filter 2**<br>See register 0096$_H$, **ATUF0** for more detail. |
| TUPF2 | 9:8 | rw | **TCP/UDP PRI for TCP/UDP Filter 2**<br>See register 0096$_H$, **TUPF0** for more detail. |

| Field | Bits | Type | Description |
|---|---|---|---|
| ATUF1 | 7:6 | rw | **Action for TCP/UDP Filter 1**<br>See register 0096$_H$, **ATUF0** for more detail. |
| TUPF1 | 5:4 | rw | **TCP/UDP PRI for TCP/UDP Filter 1**<br>See register 0096$_H$, **TUPF0** for more detail. |
| ATUF0 | 3:2 | rw | **Action for TCP/UDP Filter 0**<br>00$_B$    Protocol Portmap is Default Output Ports<br>01$_B$    Protocol Portmap is 000000$_B$<br>10$_B$    Protocol Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Type Portmap contains Defa ult Output Ports , excluding the CPU port<br>11$_B$    Protocol Portmap contains Defa ult Output Ports , excluding the CPU port |
| TUPF0 | 1:0 | rw | **TCP/UDP PRI for TCP/UDP Filter 0**<br>00$_B$    Queue 0<br>01$_B$    Queue 1<br>10$_B$    Queue 2<br>11$_B$    Queue 3 |

**TCP/UDP Action 1**

| TUA1 | Offset | Reset Value |
|---|---|---|
| TCP/UDP Action 1 | 97$_H$ | 0000$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ATUF7 | | TUPF7 | | ATUF6 | | TUPF6 | | ATUF5 | | TUPF5 | | ATUF4 | | TUPF4 | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| ATUF7 | 15:14 | rw | **Action for TCP/UDP Filter 7**<br>See register 0096$_H$, **ATUF0** for more detail. |
| TUPF7 | 13:12 | rw | **TCP/UDP PRI for TCP/UDP Filter 7**<br>See register 0096$_H$, **TUPF0** for more detail. |
| ATUF6 | 11:10 | rw | **Action for TCP/UDP Filter 6**<br>See register 0096$_H$, **ATUF0** for more detail. |
| TUPF6 | 9:8 | rw | **TCP/UDP PRI for TCP/UDP Filter 6**<br>See register 0096$_H$, **TUPF0** for more detail. |
| ATUF5 | 7:6 | rw | **Action for TCP/UDP Filter 5**<br>See register 0096$_H$, **ATUF0** for more detail. |
| TUPF5 | 5:4 | rw | **TCP/UDP PRI for TCP/UDP Filter 5**<br>See register 0096$_H$, **TUPF0** for more detail. |
| ATUF4 | 3:2 | rw | **Action for TCP/UDP Filter 4**<br>See register 0096$_H$, **ATUF0** for more detail. |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| TUPF4 | 1:0 | rw | **TCP/UDP PRI for TCP/UDP Filter 4**<br>See register 0096$_H$, **TUPF0** for more detail. |
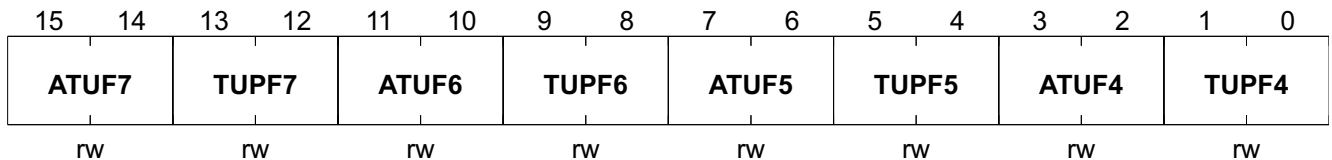
**TCP/UDP Action 2**

| TUA2 | Offset | Reset Value |
|------|--------|-------------|
| **TCP/UDP Action 2** | **98$_H$** | **0000$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Res | | COMP | | P5I | P4I | P3I | P2I | P1I | P0I | P5T | P4T | P3T | P2T | P1T | P0T |
| r | | rw | | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:14 | r | **Reserved** |
| COMP | 13:12 | rw | **Compare TCP/UDP Source Port or Destination Port**<br>00$_B$    Do not Compare<br>01$_B$    Compare Destination Port<br>10$_B$    Compare Source Port<br>11$_B$    Compare Destination Port or Source Port |
| P5I | 11 | rw | **Port 5 IP over TCP/UDP**<br>0$_B$    Use TCP/UDP field when packets contain both TCP/UDP and IP<br>1$_B$    Use IP field when packets contain both TCP/UDP and IP |
| P4I | 10 | rw | **Port 4 IP over TCP/UDP**<br>0$_B$    Use TCP/UDP field when packets contain both TCP/UDP and IP<br>1$_B$    Use IP field when packets contain both TCP/UDP and IP |
| P3I | 9 | rw | **Port 3 IP over TCP/UDP**<br>0$_B$    Use TCP/UDP field when packets contain both TCP/UDP and IP<br>1$_B$    Use IP field when packets contain both TCP/UDP and IP |
| P2I | 8 | rw | **Port 2 IP over TCP/UDP**<br>0$_B$    Use TCP/UDP field when packets contain both TCP/UDP and IP<br>1$_B$    Use IP field when packets contain both TCP/UDP and IP |
| P1I | 7 | rw | **Port 1 IP over TCP/UDP**<br>0$_B$    Use TCP/UDP field when packets contain both TCP/UDP and IP<br>1$_B$    Use IP field when packets contain both TCP/UDP and IP |
| P0I | 6 | rw | **Port 0 IP over TCP/UDP**<br>0$_B$    Use TCP/UDP field when packets contain both TCP/UDP and IP<br>1$_B$    Use IP field when packets contain both TCP/UDP and IP |
| P5T | 5 | rw | **Port 5 TCP/UDP PRIEN**<br>0$_B$    Do not use TCP/UDP priority<br>1$_B$    Use TCP/UDP priority |
| P4T | 4 | rw | **Port 4 TCP/UDP PRIEN**<br>0$_B$    Do not use TCP/UDP priority<br>1$_B$    Use TCP/UDP priority |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| P3T | 3 | rw | **Port 3 TCP/UDP PRIEN** <br> $0_B$    Do not use TCP/UDP priority <br> $1_B$    Use TCP/UDP priority |
| P2T | 2 | rw | **Port 2 TCP/UDP PRIEN** <br> $0_B$    Do not use TCP/UDP priority <br> $1_B$    Use TCP/UDP priority |
| P1T | 1 | rw | **Port 1 TCP/UDP PRIEN** <br> $0_B$    Do not use TCP/UDP priority <br> $1_B$    Use TCP/UDP priority |
| P0T | 0 | rw | **Port 0 TCP/UDP PRIEN** <br> $0_B$    Do not use TCP/UDP priority <br> $1_B$    Use TCP/UDP priority |

**Interrupt Enable Register**
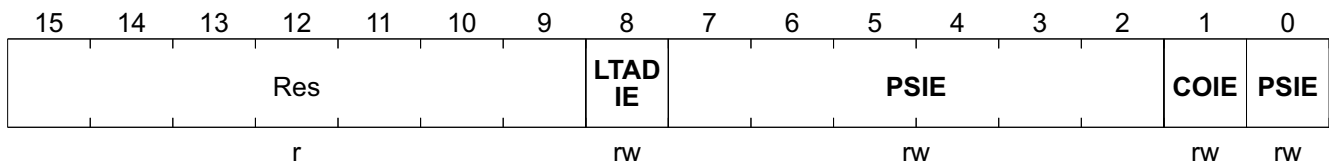
| IE | | Offset | Reset Value |
|----|--|--------|-------------|
| **Interrupt Enable Register** | | $9A_H$ | $0000_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | Res | | | | LTAD IE | | | | PSIE | | | COIE | PSIE |
| | | | r | | | | rw | | | | rw | | | rw | rw |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:9 | r | **Reserved** |
| LTADIE | 8 | rw | **Leaning Table Access Done Interrupt Enable** <br> $0_B$    Interrupt disable <br> $1_B$    Interrupt enable |
| PSIE | 7:2 | rw | **Port Security Interrupt Enable** <br> It's a per port setting <br> $0_B$    Interrupt disable <br> $1_B$    Interrupt enable |
| COIE | 1 | rw | **Counter Overflow Interrupt Enable** <br> $0_B$    Interrupt disable <br> $1_B$    Interrupt enable |
| PSIE | 0 | rw | **Port Status Interrupt Enable** <br> $0_B$    Interrupt disable <br> $1_B$    Interrupt enable |

**Interrupt Status Register**
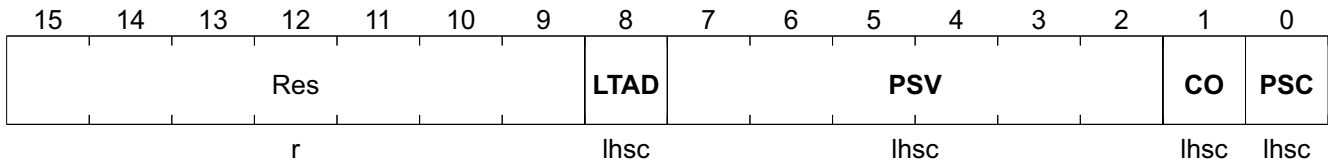
| IS | | Offset | Reset Value |
|----|--|--------|-------------|
| **Interrupt Status Register** | | $9B_H$ | $0000_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | Res | | | | LTAD | | | PSV | | | | CO | PSC |
| | | | r | | | | lhsc | | | lhsc | | | | lhsc | lhsc |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:9 | r | **Reserved** |
| LTAD | 8 | lhsc | **Leaning Table Access Done**<br>$0_B$    Access does not end<br>$1_B$    Access end |
| PSV | 7:2 | lhsc | **Port Security Violation**<br>It's a per port setting<br>$0_B$    Security did not violate<br>$1_B$    Security violated |
| CO | 1 | lhsc | **Counter Overflow**<br>$0_B$    Overflow did not happen<br>$1_B$    Overflow happened for any of the counters |
| PSC | 0 | lhsc | **Port Status Change**<br>$0_B$    No status (link, speed, duplex, flow control) changed for any port<br>$1_B$    Status changed for any of 6 ports |

## 5.3 Counter and Switch Status Registers

**Chip Identifier 0**

| CI0 | Offset | Reset Value |
|-----|--------|-------------|
| **Chip Identifier 0** | $A0_H$ | $1022_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | PC | | | | | | | | | VN | |
| | | | | | ro | | | | | | | | | ro | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| PC | 15:4 | ro | **Product Code[11:0]** |
| VN | 3:0 | ro | **Version Number** |
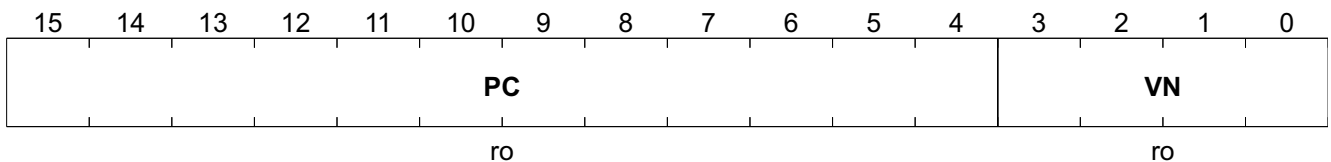
**Chip Identifier 1**

| CI1 | Offset | Reset Value |
|-----|--------|-------------|
| **Chip Identifier 1** | $A1_H$ | $0007_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Res | | | | | | | | | | | | PC | | | |
| ro | | | | | | | | | | | | ro | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:4 | ro | **Reserved** |
| PC | 3:0 | ro | **Product Code[ 15:12 ]** |
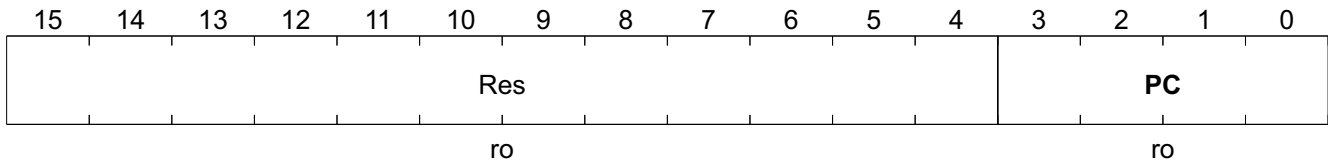
**Port Status 0**

**PS0**                          **Offset**                          **Reset Value**
**Port Status 0**                 **A2$_H$**                          **0000$_H$**
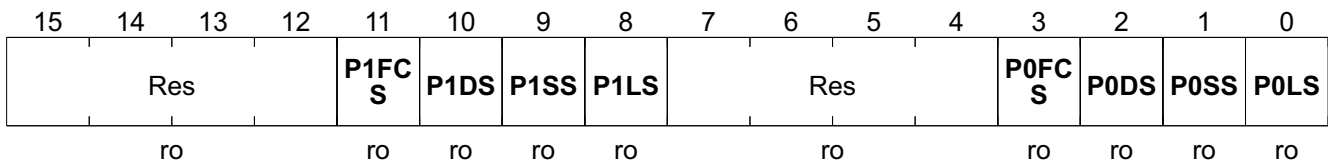
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Res | | | | P1FCS | P1DS | P1SS | P1LS | Res | | | | P0FCS | P0DS | P0SS | P0LS |
| ro | | | | ro | ro | ro | ro | ro | | | | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:12 | ro | **Reserved** |
| P1FCS | 11 | ro | **Port 1 Flow Control Status**<br>0$_B$    Port 1 disables the Full Flow Control/Half Back Pressure Function<br>1$_B$    Port 1 enabled the Full Flow Control/Half Back Pressure Function |
| P1DS | 10 | ro | **Port 1 Duplex Status**<br>0$_B$    Port 1 operates in the Half Duplex<br>1$_B$    Port 1 operates in the Full Duplex |
| P1SS | 9 | ro | **Port 1 Speed Status**<br>0$_B$    Port 1 operates in the 10M<br>1$_B$    Port 1 operates in the 100M |
| P1LS | 8 | ro | **Port 1 Link Status**<br>0$_B$    Port 1 links down<br>1$_B$    Port 1 links up |
| Res | 7:4 | ro | **Reserved** |
| P0FCS | 3 | ro | **Port 0 Flow Control Status**<br>0$_B$    Port 0 disables the Full Flow Control/Half Back Pressure Function<br>1$_B$    Port 0 enabled the Full Flow Control/Half Back Pressure Function |
| P0DS | 2 | ro | **Port 0 Duplex Status**<br>0$_B$    Port 0 operates in the Half Duplex<br>1$_B$    Port 0 operates in the Full Duplex |
| P0SS | 1 | ro | **Port 0 Speed Status**<br>0$_B$    Port 0 operates in the 10M<br>1$_B$    Port 0 operates in the 100M |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| P0LS | 0 | ro | **Port 0 Link Status**<br>$0_B$     Port 0 links down<br>$1_B$     Port 0 links up |

**Port Status 1**

| PS1 | Offset | Reset Value |
|-----|--------|-------------|
| Port Status 1 | $A3_H$ | $0000_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| P4FCS | P4DS | P4SS | P4LS | P3FCS | P3DS | P3SS | P3LS | | | Res | | P2FCS | P2DS | P2SS | P2LS |
| ro | ro | ro | ro | ro | ro | ro | ro | | | ro | | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| P4FCS | 15 | ro | **Port 4 Flow Control Status**<br>$0_B$     Port 4 disables the Full Flow Control/Half Back Pressure Function<br>$1_B$     Port 4 enabled the Full Flow Control/Half Back Pressure Function |
| P4DS | 14 | ro | **Port 4 Duplex Status**<br>$0_B$     Port 4 operates in the Half Duplex<br>$1_B$     Port 4 operates in the Full Duplex |
| P4SS | 13 | ro | **Port 4 Speed Status**<br>$0_B$     Port 4 operates in the 10M<br>$1_B$     Port 4 operates in the 100M |
| P4LS | 12 | ro | **Port 4 Link Status**<br>$0_B$     Port 4 links down<br>$1_B$     Port 4 links up |
| P3FCS | 11 | ro | **Port 3 Flow Control Status**<br>$0_B$     Port 3 disables the Full Flow Control/Half Back Pressure Function<br>$1_B$     Port 3 enabled the Full Flow Control/Half Back Pressure Function |
| P3DS | 10 | ro | **Port 3 Duplex Status**<br>$0_B$     Port 3 operates in the Half Duplex<br>$1_B$     Port 3 operates in the Full Duplex |
| P3SS | 9 | ro | **Port 3 Speed Status**<br>$0_B$     Port 3 operates in the 10M<br>$1_B$     Port 3 operates in the 100M |
| P3LS | 8 | ro | **Port 3 Link Status**<br>$0_B$     Port 3 links down<br>$1_B$     Port 3 links up. |
| Res | 7:4 | ro | **Reserved** |
| P2FCS | 3 | ro | **Port 2 Flow Control Status**<br>$0_B$     Port 2 disables the Full Flow Control/Half Back Pressure Function<br>$1_B$     Port 2 enabled the Full Flow Control/Half Back Pressure Function |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| P2DS | 2 | ro | **Port 2 Duplex Status** <br> $0_B$  Port 2 operates in the Half Duplex <br> $1_B$  Port 2 operates in the Full Duplex |
| P2SS | 1 | ro | **Port 2 Speed Status** <br> $0_B$  Port 2 operates in the 10M <br> $1_B$  Port 2 operates in the 100M |
| P2LS | 0 | ro | **Port 2 Link Status** <br> $0_B$  Port 2 links down <br> $1_B$  Port 2 links up |

**Port Status 2**
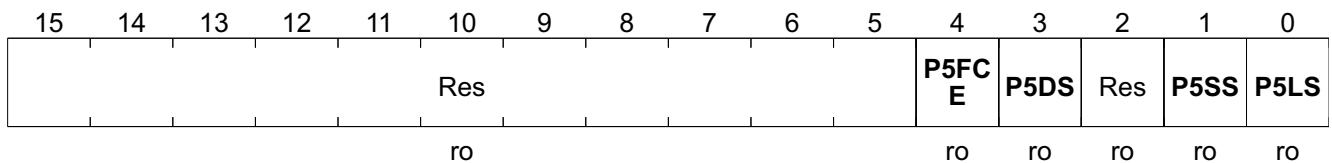
| **PS2** | **Offset** | **Reset Value** |
|---------|-----------|-----------------|
| **Port Status 2** | **A4$_H$** | **0000$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | Res | | | | | | P5FCE | P5DS | Res | P5SS | P5LS |
| | | | | | ro | | | | | | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:5 | ro | **Reserved** |
| P5FCE | 4 | ro | **Port 5 Flow Control Enable** <br> $0_B$  Port 5 disables the Full Flow Control/Half Back Pressure Function <br> $1_B$  Port 5 enabled the Full Flow Control/Half Back Pressure Function |
| P5DS | 3 | ro | **Port 5 Duplex Status** <br> $0_B$  Port 5 operates in the Half Duplex <br> $1_B$  Port 5 operates in the Full Duplex |
| Res | 2 | ro | **Reserved** |
| P5SS | 1 | ro | **Port 5 Speed Status** <br> $0_B$  Port 5 operates in the 10M <br> $1_B$  Port 5 operates in the 100M |
| P5LS | 0 | ro | **Port 5 Link Status** <br> $0_B$  Port 5 links down <br> $1_B$  Port 5 links up |

**Counter Low 0**

| **CL0** | **Offset** | **Reset Value** |
|---------|-----------|-----------------|
| **Port 0 Receive Packet Counter Low** | **A8$_H$** | **0000$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | COUNTER | | | | | | | | |

rw
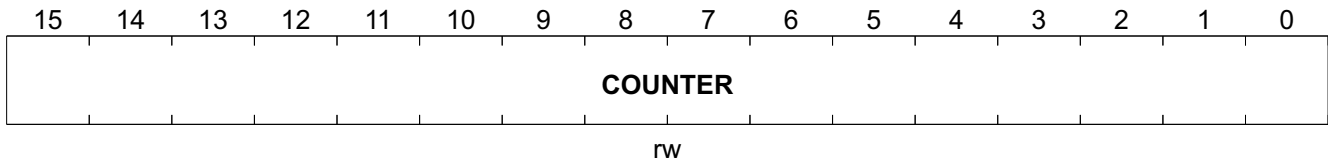
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| COUNTER | 15:0 | rw | **Counter[15:0]** |

**Similar Registers**

All CLx registers have the same structure and characteristics, see **CL0**.
The offset addresses of the other CLx registers are listed in **Table 45**.

**Table 45    CLx Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|----------------|-------------|
| CL1 | Port 1 Receive Packet Counter Low | $AC_H$ | |
| CL2 | Port 2 Receive Packet Counter Low | $B0_H$ | |
| CL3 | Port 3 Receive Packet Counter Low | $B4_H$ | |
| CL4 | Port 4 Receive Packet Counter Low | $B6_H$ | |
| CL5 | Port 5 Receive Packet Counter Low | $B8_H$ | |
| CL6 | Port 0 Receive Packet Byte Count Low | $BA_H$ | |
| CL7 | Port 1 Receive Packet Byte Count Low | $BE_H$ | |
| CL8 | Port 2 Receive Packet Byte Count Low | $C2_H$ | |
| CL9 | Port 3 Receive Packet Byte Count Low | $C6_H$ | |
| CL10 | Port 4 Receive Packet Byte Count Low | $C8_H$ | |
| CL11 | Port 5 Receive Packet Byte Count Low | $CA_H$ | |
| CL12 | Port 0 Transmit Packet Count Low | $CC_H$ | |
| CL13 | Port 1 Transmit Packet Count Low | $D0_H$ | |
| CL14 | Port 2 Transmit Packet Count Low | $D4_H$ | |
| CL15 | Port 3 Transmit Packet Count Low | $D8_H$ | |
| CL16 | Port 4 Transmit Packet Count Low | $DA_H$ | |
| CL17 | Port 5 Transmit Packet Count Low | $DC_H$ | |
| CL18 | Port 0 Transmit Packet Byte Count Low | $DE_H$ | |
| CL19 | Port 1 Transmit Packet Byte Count Low | $E2_H$ | |
| CL20 | Port 2 Transmit Packet Byte Count Low | $E6_H$ | |
| CL21 | Port 3 Transmit Packet Byte Count Low | $EA_H$ | |
| CL22 | Port 4 Transmit Packet Byte Count Low | $EC_H$ | |
| CL23 | Port 5 Transmit Packet Byte Count Low | $EE_H$ | |
| CL24 | Port 0 Collision Count Low | $F0_H$ | |
| CL25 | Port 1 Collision Count Low | $F4_H$ | |
| CL26 | Port 2 Collision Count Low | $F8_H$ | |
| CL27 | Port 3 Collision Count Low | $FC_H$ | |
| CL28 | Port 4 Collision Count Low | $FE_H$ | |
| CL29 | Port 5 Collision Count Low | $100_H$ | |

**Table 45    CLx Registers** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| CL30 | Port 0 Error Count Low | 102$_H$ | |
| CL31 | Port 1 Error Count Low | 106$_H$ | |
| CL32 | Port 2 Error Count Low | 10A$_H$ | |
| CL33 | Port 3 Error Count Low | 10E$_H$ | |
| CL34 | Port 4 Error Count Low | 110$_H$ | |
| CL35 | Port 5 Error Count Low | 112$_H$ | |

**Counter High 0**

| **CH0** | | **Offset** | | **Reset Value** |
|---|---|---|---|---|
| **Port 0 Receive Packet Counter High** | | **A9$_H$** | | **0000$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | COUNTER | | | | | | | | |

rw
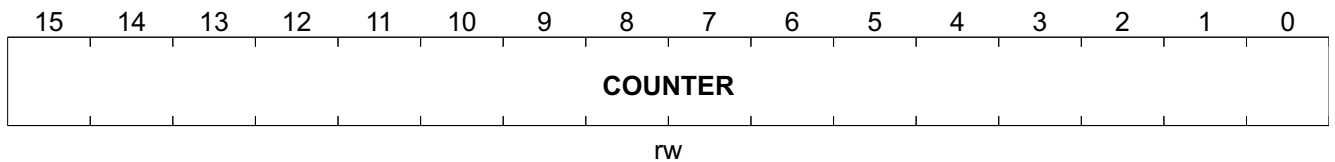
| Field | Bits | Type | Description |
|---|---|---|---|
| COUNTER | 15:0 | rw | **Counter[31:16]** |

**Similar Registers**

All CHx registers have the same structure and characteristics, see **CH0**.
The offset addresses of the other CLH registers are listed in **Table 46**.

**Table 46    CHx Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| CH1 | Port 1 Receive Packet Counter High | AD$_H$ | |
| CH2 | Port 2 Receive Packet Counter High | B1$_H$ | |
| CH3 | Port 3 Receive Packet Counter High | B5$_H$ | |
| CH4 | Port 4 Receive Packet Counter High | B7$_H$ | |
| CH5 | Port 5 Receive Packet Counter High | B9$_H$ | |
| CH6 | Port 0 Receive Packet Byte Count High | BB$_H$ | |
| CH7 | Port 1 Receive Packet Byte Count High | BF$_H$ | |
| CH8 | Port 2 Receive Packet Byte Count High | C3$_H$ | |
| CH9 | Port 3 Receive Packet Byte Count High | C7$_H$ | |
| CH10 | Port 4 Receive Packet Byte Count High | C9$_H$ | |
| CH11 | Port 5 Receive Packet Byte Count High | CB$_H$ | |
| CH12 | Port 0 Transmit Packet Count High | CD$_H$ | |
| CH13 | Port 1 Transmit Packet Count High | D1$_H$ | |
| CH14 | Port 2 Transmit Packet Count High | D5$_H$ | |

**Table 46    CHx Registers** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| CH15 | Port 3 Transmit Packet Count High | D9$_H$ | |
| CH16 | Port 4 Transmit Packet Count High | DB$_H$ | |
| CH17 | Port 5 Transmit Packet Count High | DD$_H$ | |
| CH18 | Port 0 Transmit Packet Byte Count High | DF$_H$ | |
| CH19 | Port 1 Transmit Packet Byte Count High | E3$_H$ | |
| CH20 | Port 2 Transmit Packet Byte Count High | E7$_H$ | |
| CH21 | Port 3 Transmit Packet Byte Count High | EB$_H$ | |
| CH22 | Port 4 Transmit Packet Byte Count High | ED$_H$ | |
| CH23 | Port 5 Transmit Packet Byte Count High | EF$_H$ | |
| CH24 | Port 0 Collision Count High | F1$_H$ | |
| CH25 | Port 1 Collision Count High | F5$_H$ | |
| CH26 | Port 2 Collision Count High | F9$_H$ | |
| CH27 | Port 3 Collision Count High | FD$_H$ | |
| CH28 | Port 4 Collision Count High | FF$_H$ | |
| CH29 | Port 5 Collision Count High | 101$_H$ | |
| CH30 | Port 0 Error Count High | 103$_H$ | |
| CH31 | Port 1 Error Count High | 107$_H$ | |
| CH32 | Port 2 Error Count High | 10B$_H$ | |
| CH33 | Port 3 Error Count High | 10F$_H$ | |
| CH34 | Port 4 Error Count High | 111$_H$ | |
| CH35 | Port 5 Error Count High | 113$_H$ | |

**Over-Flow Flag 0**

| **OFF0** | **Offset** | **Reset Value** |
|---|---|---|
| **Over-Flow Flag 0** | **114$_H$** | **0000$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **P3_BC** | Res | **P2_BC** | Res | **P1_BC** | Res | **P0_BC** | **P5_C** | **P4_C** | **P3_C** | Res | **P2_C** | Res | **P1_C** | Res | **P0_C** |
| lhsc | ro | lhsc | ro | lhsc | ro | lhsc | lhsc | lhsc | lhsc | ro | lhsc | ro | lhsc | ro | lhsc |

| Field | Bits | Type | Description |
|---|---|---|---|
| P3_BC | 15 | lhsc | **Overflow of Port 3 Receive Packet Byte Count**<br>0$_B$    No overflow<br>1$_B$    Overflow |
| Res | 14 | ro | **Reserved** |
| P2_BC | 13 | lhsc | **Overflow of Port 2 Receive Packet Byte Count**<br>0$_B$    No overflow<br>1$_B$    Overflow |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 12 | ro | **Reserved** |
| P1_BC | 11 | lhsc | **Overflow of Port 1 Receive Packet Byte Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| Res | 10 | ro | **Reserved** |
| P0_BC | 9 | lhsc | **Overflow of Port 0 Receive Packet Byte Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| P5_C | 8 | lhsc | **Overflow of Port 5 Receive Packet Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| P4_C | 7 | lhsc | **Overflow of Port 4 Receive Packet Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| P3_C | 6 | lhsc | **Overflow of Port 3 Receive Packet Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| Res | 5 | ro | **Reserved** |
| P2_C | 4 | lhsc | **Overflow of Port 2 Receive Packet Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| Res | 3 | ro | **Reserved** |
| P1_C | 2 | lhsc | **Overflow of Port 1 Receive Packet Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| Res | 1 | ro | **Reserved** |
| P0_C | 0 | lhsc | **Overflow of Port 0 Receive Packet Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |

**Over-Flow Flag 1**

**OFF1**          **Offset**          **Reset Value**
**Over-Flow Flag 1**          $115_H$          $0000_H$
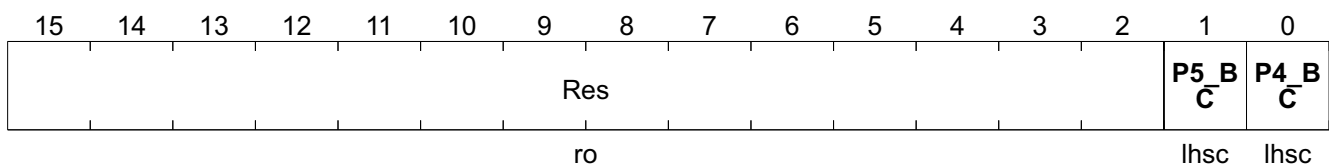
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Res | | | | | | | | P5_B C | P4_B C |
| | | | | | | ro | | | | | | | | lhsc | lhsc |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15:2 | ro | **Reserved** |

| Field | Bits | Type | Description |
|---|---|---|---|
| P5_BC | 1 | lhsc | **Overflow of Port 5 Receive Packet Byte Count**<br>$0_B$　No overflow<br>$1_B$　Overflow |
| P4_BC | 0 | lhsc | **Overflow of Port 4 Receive Packet Byte Count**<br>$0_B$　No overflow<br>$1_B$　Overflow |

**Over-Flow Flag 2**

**OFF2**            **Offset**            **Reset Value**
**Over-Flow Flag 2**            **116$_H$**            **0000$_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P3_BC | Res | P2_BC | Res | P1_BC | Res | P0_BC | P5_C | P4_C | P3_C | Res | P2_C | Res | P1_C | Res | P0_C |
| lhsc | ro | lhsc | ro | lhsc | ro | lhsc | lhsc | lhsc | lhsc | ro | lhsc | ro | lhsc | ro | lhsc |

| Field | Bits | Type | Description |
|---|---|---|---|
| P3_BC | 15 | lhsc | **Overflow of Port 3 Transmit Packet Byte Count**<br>$0_B$　No overflow<br>$1_B$　Overflow |
| Res | 14 | ro | **Reserved** |
| P2_BC | 13 | lhsc | **Overflow of Port 2 Transmit Packet Byte Count**<br>$0_B$　No overflow<br>$1_B$　Overflow |
| Res | 12 | ro | **Reserved** |
| P1_BC | 11 | lhsc | **Overflow of Port 1 Transmit Packet Byte Count**<br>$0_B$　No overflow<br>$1_B$　Overflow |
| Res | 10 | ro | **Reserved** |
| P0_BC | 9 | lhsc | **Overflow of Port 0 Transmit Packet Byte Count**<br>$0_B$　No overflow<br>$1_B$　Overflow |
| P5_C | 8 | lhsc | **Overflow of Port 5 Transmit Packet Count**<br>$0_B$　No overflow<br>$1_B$　Overflow |
| P4_C | 7 | lhsc | **Overflow of Port 4 Transmit Packet Count**<br>$0_B$　No overflow<br>$1_B$　Overflow |
| P3_C | 6 | lhsc | **Overflow of Port 3 Transmit Packet Count**<br>$0_B$　No overflow<br>$1_B$　Overflow |
| Res | 5 | ro | **Reserved** |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| P2_C | 4 | lhsc | **Overflow of Port 2 Transmit Packet Count** <br> $0_B$ No overflow <br> $1_B$ Overflow |
| Res | 3 | ro | **Reserved** |
| P1_C | 2 | lhsc | **Overflow of Port 1 Transmit Packet Count** <br> $0_B$ No overflow <br> $1_B$ Overflow |
| Res | 1 | ro | **Reserved** |
| P0_C | 0 | lhsc | **Overflow of Port 0 Transmit Packet Count** <br> $0_B$ No overflow <br> $1_B$ Overflow |

**Over-Flow Flag 3**

**OFF3**     **Offset**     **Reset Value**

**Over-Flow Flag 3**     $117_H$     $0000_H$
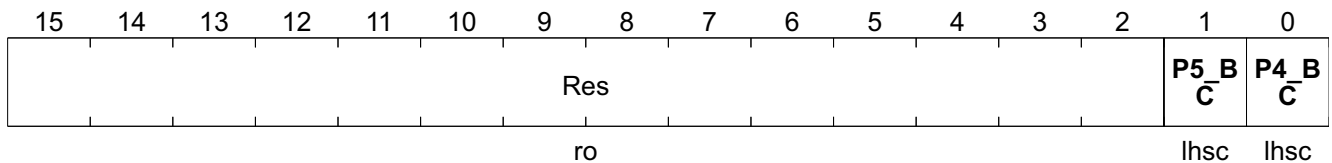
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Res | | | | | | | P5_B<br>C | P4_B<br>C |
| | | | | | | | ro | | | | | | | lhsc | lhsc |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:2 | ro | **Reserved** |
| P5_BC | 1 | lhsc | **Overflow of Port 5 Transmit Packet Byte Count** <br> $0_B$ No overflow <br> $1_B$ Overflow |
| P4_BC | 0 | lhsc | **Overflow of Port 4 Transmit Packet Byte Count** <br> $0_B$ No overflow <br> $1_B$ Overflow |

**Over-Flow Flag 4**

**OFF4**     **Offset**     **Reset Value**

**Over-Flow Flag 4**     $118_H$     $0000_H$
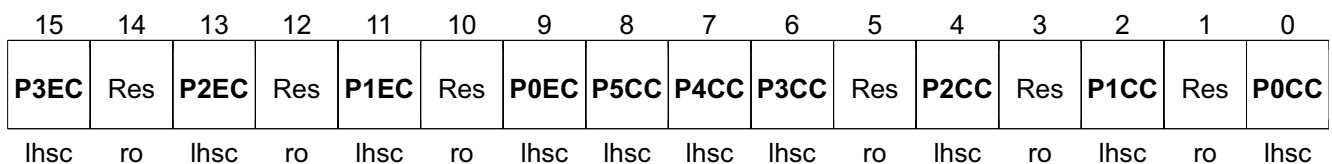
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| **P3EC** | Res | **P2EC** | Res | **P1EC** | Res | **P0EC** | **P5CC** | **P4CC** | **P3CC** | Res | **P2CC** | Res | **P1CC** | Res | **P0CC** |
| lhsc | ro | lhsc | ro | lhsc | ro | lhsc | lhsc | lhsc | lhsc | ro | lhsc | ro | lhsc | ro | lhsc |

| Field | Bits | Type | Description |
|---|---|---|---|
| P3EC | 15 | lhsc | **Overflow of Port 3 Error Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| Res | 14 | ro | **Reserved** |
| P2EC | 13 | lhsc | **Overflow of Port 2 Error Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| Res | 12 | ro | **Reserved** |
| P1EC | 11 | lhsc | **Overflow of Port 1 Error Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| Res | 10 | ro | **Reserved** |
| P0EC | 9 | lhsc | **Overflow of Port 0 Error Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| P5CC | 8 | lhsc | **Overflow of Port 5 Collision Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| P4CC | 7 | lhsc | **Overflow of Port 4 Collision Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| P3CC | 6 | lhsc | **Overflow of Port 3 Collision Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| Res | 5 | ro | **Reserved** |
| P2CC | 4 | lhsc | **Overflow of Port 2 Collision Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| Res | 3 | ro | **Reserved** |
| P1CC | 2 | lhsc | **Overflow of Port 1 Collision Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| Res | 1 | ro | **Reserved** |
| P0CC | 0 | lhsc | **Overflow of Port 0 Collision Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |

**Over-Flow Flag 5**

| **OFF5** | **Offset** | **Reset Value** |
|---|---|---|
| **Over-Flow Flag 5** | $119_H$ | $0000_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | | | | Res | | | | | | | | | P5EC | P4EC |
| | | | | | ro | | | | | | | | | lhsc | lhsc |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:2 | ro | **Reserved** |
| P5EC | 1 | lhsc | **Overflow of Port 5 Error Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
| P4EC | 0 | lhsc | **Overflow of Port 4 Error Count**<br>$0_B$ No overflow<br>$1_B$ Overflow |
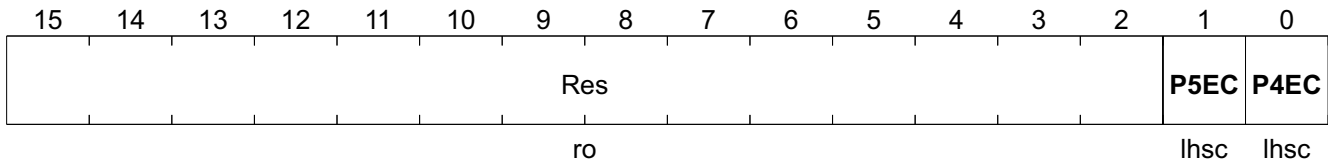
**Hardware Setting Low Register**

| HSL | Offset | Reset Value |
|-----|--------|-------------|
| Hardware Setting Low Register | $130_H$ | $0000_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| H | BO | DAF | BP | DB | GM | RM | P4IT | | GFC | P4FM | DC | CA | | AC | AN |
| ro | ro | ro | ro | ro | ro | ro | ro | | ro | ro | ro | ro | | ro | ro |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| H | 15 | ro | **Resreved** |
| BO | 14 | ro | **Bond** |
| DAF | 13 | ro | **Disable ADM6996LC/LCX/LHX Function** |
| BP | 12 | ro | **BPEN** |
| DB | 11 | ro | **16/32 Bit Data Bus** |
| GM | 10 | ro | **GPSI Mode** |
| RM | 9 | ro | **RMII Mode** |
| P4IT | 8:7 | ro | **Port 4 Interface Type** |
| GFC | 6 | ro | **Global Flow Control** |
| P4FM | 5 | ro | **Port 4 Fiber Mode** |
| DC | 4 | ro | **Dual Color** |
| CA | 3:2 | ro | **Chip Address** |
| AC | 1 | ro | **Auto-Crossover** |
| AN | 0 | ro | **Auto-Negotiation** |
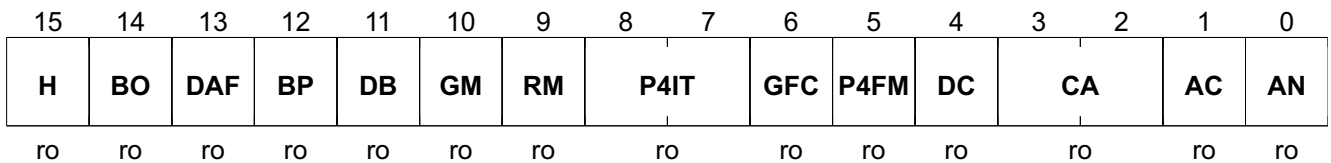
**Hardware Setting High Register**
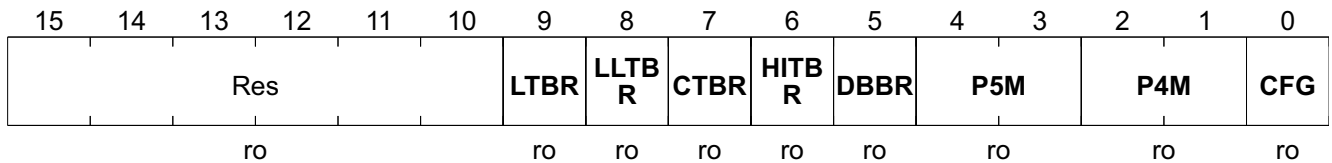
| **HSH** | **Offset** | **Reset Value** |
|---|---|---|
| **Hardware Setting High Register** | **131$_H$** | **0000$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Res | | | LTBR | LLTBR | CTBR | HITBR | DBBR | P5M | | P4M | | CFG |
| | | ro | | | | ro | ro | ro | ro | ro | ro | | ro | | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| Res | 15:10 | ro | **Reserved** |
| LTBR | 9 | ro | **Learning Table Bist Result**<br>0$_B$   Work<br>1$_B$   Do not Work |
| LLTBR | 8 | ro | **Linklist Table Bist Result**<br>(Linklist Table does not do bist test in normal mode)<br>0$_B$   Work<br>1$_B$   Do not Work |
| CTBR | 7 | ro | **Control Table Bist Result**<br>0$_B$   Work<br>1$_B$   Do not Work |
| HITBR | 6 | ro | **Hardware IGMP Table Bist Result**<br>0$_B$   Work<br>1$_B$   Do not Work |
| DBBR | 5 | ro | **Data Buffer Bist Result**<br>0$_B$   Work<br>1$_B$   Do not Work |
| P5M | 4:3 | ro | **P5 Mode**<br>00$_B$   GPSI<br>01$_B$   RMII<br>10$_B$   MII |
| P4M | 2:1 | ro | **P4 Mode**<br>00$_B$   Port 4 uses inner PHY<br>01$_B$   Port 4 uses MII<br>11$_B$   Port 4 isolated PHY |
| CFG | 0 | ro | **CFG** |

**Assign Option Register**
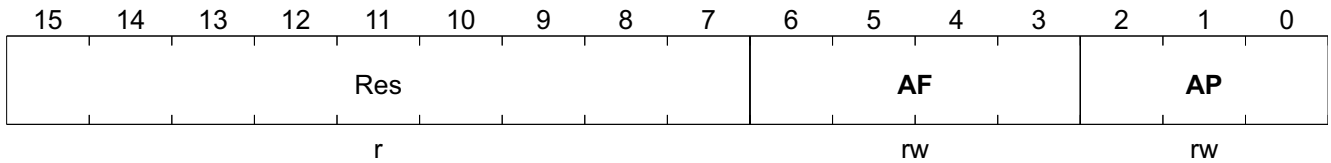
| **AO** | **Offset** | **Reset Value** |
|---|---|---|
| **Assign Option Register** | **135$_H$** | **0000$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | | Res | | | | | | | AF | | | | AP | |
| | | | r | | | | | | | rw | | | | rw | |

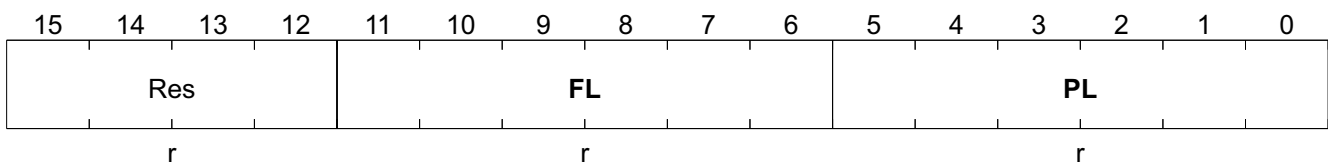| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:7 | r | **Reserved** |
| AF | 6:3 | rw | **Assign Fid** <br> It is used for assign lock FID. |
| AP | 2:0 | rw | **Assign Port** <br> It is used for the port that the user wants to assign or for the monitor port. |

**Security Violation Port**
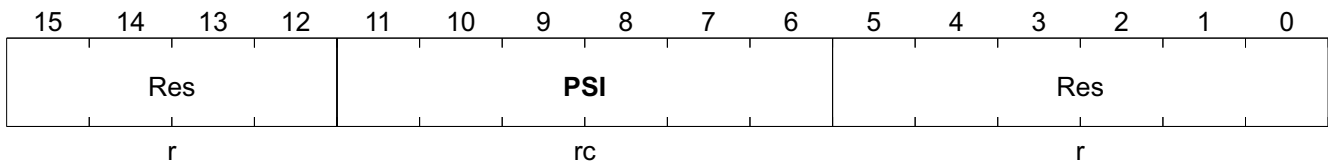
| **SVP** | **Offset** | **Reset Value** |
|---------|-----------|-----------------|
| **Security Violation Port** | **138**$_H$ | **0000**$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | Res | | | | | PSI | | | | | | Res | | | |
| | r | | | | | rc | | | | | | r | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:12 | r | **Reserved** |
| PSI | 11:6 | rc | **Port Source Intrusion** <br> $0_B$      Source Intrusion did not happen <br> $1_B$      Source Intrusion happened |
| Res | 5:0 | r | **Reserved** |

**Security Status 0**

| **SS0** | **Offset** | **Reset Value** |
|---------|-----------|-----------------|
| **Security Status 0** | **139**$_H$ | **0000**$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | Res | | | | | FL | | | | | | PL | | | |
| | r | | | | | r | | | | | | r | | | |

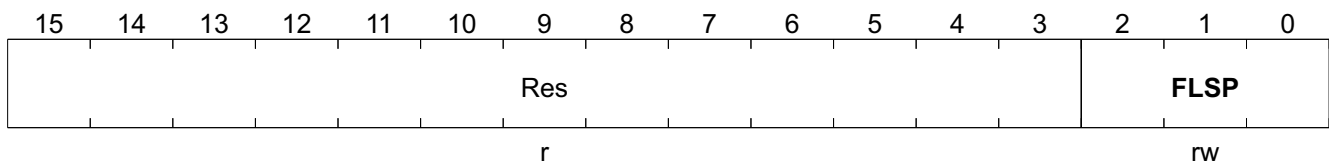| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:12 | r | **Reserved** |
| FL | 11:6 | r | **First Lock**<br>$0_B$     Port did not lock the address<br>$1_B$     Port locked the address |
| PL | 5:0 | r | **Port Locked**<br>$0_B$     Port did not close<br>$1_B$     Port closed because of source violation |

**Security Status 1**
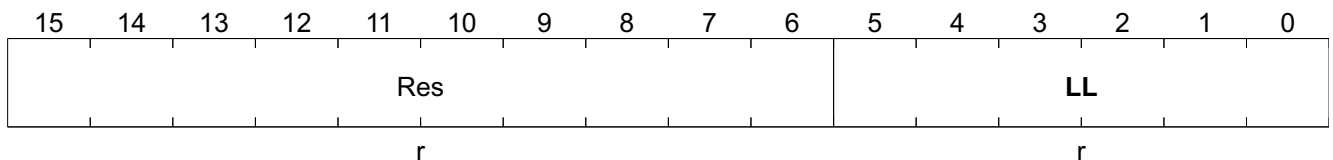
| **SS1** | **Offset** | **Reset Value** |
|---------|------------|-----------------|
| **Security Status 1** | **$13A_H$** | **$0000_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | | | | Res | | | | | | | | LL | | |
| | | | | | r | | | | | | | | r | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:6 | r | **Reserved** |
| LL | 5:0 | r | **Link Lock**<br>$0_B$     Link Lock did not happen<br>$1_B$     Link Lock happened |

**First Lock Address Search**

| **FLAS** | **Offset** | **Reset Value** |
|----------|------------|-----------------|
| **First Lock Address Search** | **$13B_H$** | **$0000_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | | | | | Res | | | | | | | | FLSP | |
| | | | | | | r | | | | | | | | rw | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:3 | r | **Reserved** |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| FLSP | 2:0 | rw | **First Lock Search Port**<br>Users could write this register to get the lock address and the lock FID (returned in the $13C_H$, $13D_H$, $13E_H$, $13F_H$) associated with the port.<br>$000_B$  Search the address and FID locked on the port 0<br>$001_B$  Search the address and FID locked on the port 1<br>$010_B$  Search the address and FID locked on the port 1<br>$011_B$  Search the address and FID locked on the port 1<br>$100_B$  Search the address and FID locked on the port 1<br>$101_B$  Search the address and FID locked on the port 1 |

**First Lock Address [15:0]**

| **FLA1** | | | | | | | | **Offset** | | | | | | **Reset Value** | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **First Lock Address [15:0]** | | | | | | | | $13C_H$ | | | | | | $0000_H$ | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **FLA** | | | | | | | | |
| | | | | | | | r | | | | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| FLA | 15:0 | r | **First Lock Address [15:0]** |

**First Lock Address [31:16]**

| **FLA2** | | | | | | | | **Offset** | | | | | | **Reset Value** | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **First Lock Address [31:16]** | | | | | | | | $13D_H$ | | | | | | $0000_H$ | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | **FLA** | | | | | | | | |
| | | | | | | | r | | | | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| FLA | 15:0 | r | **First Lock Address [31:16]** |

**First Lock Address [47:32]**

| **FLA3** | **Offset** | **Reset Value** |
|---|---|---|
| **First Lock Address [47:32]** | $13E_H$ | $0000_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | FLA | | | | | | | | |

r
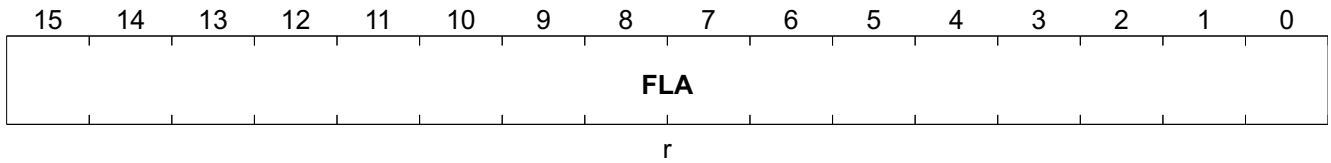
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| FLA | 15:0 | r | **First Lock Address [47:32]** |

**First Lock FID**

| **FLF** | | **Offset** | | **Reset Value** |
|---------|---|-----------|---|----------------|
| **First Lock FID** | | **13F$_H$** | | **0000$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | Res | | | | | | | | | FLF | | |

r                                                                r
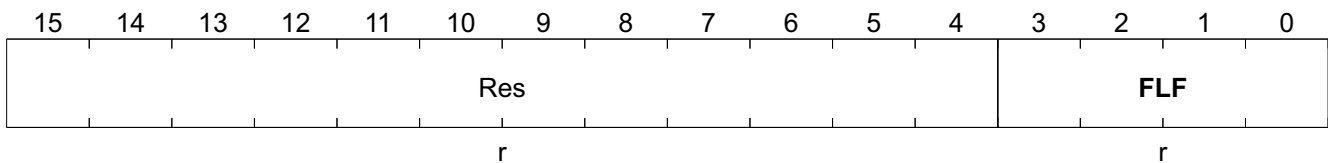
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:4 | r | **Reserved** |
| FLF | 3:0 | r | **First Lock FID** |

**Counter Control Low Register**

| **CCL** | | **Offset** | | **Reset Value** |
|---------|---|-----------|---|----------------|
| **Counter Control Low Register** | | **140$_H$** | | **0000$_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | Res | | | | | BAS | C | | | IRC_RPC | | | |

r                                              rw    rw              rw
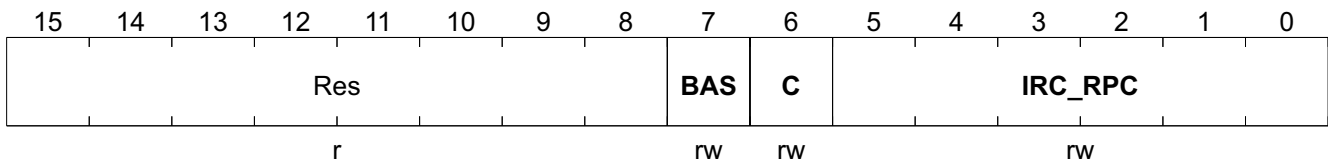
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| Res | 15:8 | r | **Reserved** |
| BAS | 7 | rw | **Busy/Access Start**<br>$0_B$    The counter control is free<br>$1_B$    The counter control is busy, or users should write $1_B$ into this bit to start the access when the engine is free |

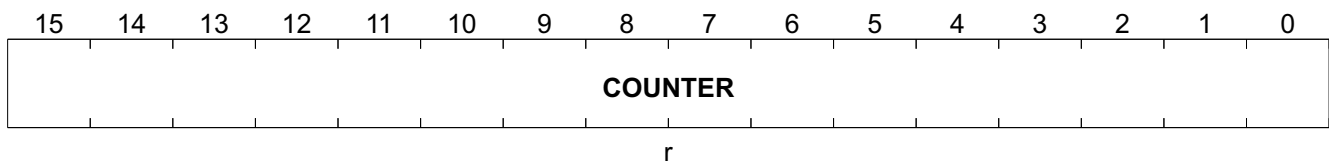| Field | Bits | Type | Description |
|-------|------|------|-------------|
| C | 6 | rw | **Counter** <br> $0_B$     Indirect Read Counter <br> $1_B$     Renew Port Counter |
| IRC_RPC | 5:0 | rw | **Indirect Read Counter** <br> It means the counter address <br> **Renew Port Counter** <br> It means the counters on each port to renew |

**Counter Status Low Register**

| CSL | Offset | Reset Value |
|-----|--------|-------------|
| **Counter Status Low Register** | **$142_H$** | **$0000_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | | | | | | COUNTER | | | | | | | | |

r
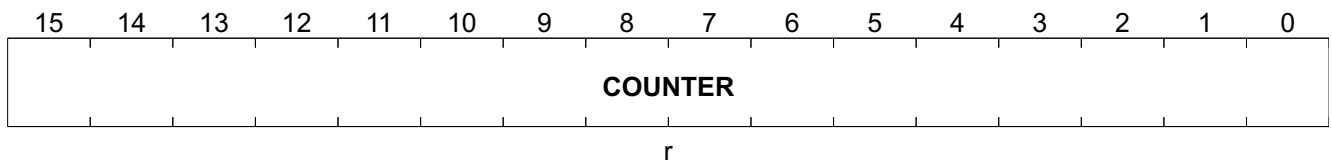
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| COUNTER | 15:0 | r | **Counter [15:0]** |

**Counter Status High Register**

| CSH | Offset | Reset Value |
|-----|--------|-------------|
| **Counter Status High Register** | **$143_H$** | **$0000_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | | | | | | COUNTER | | | | | | | | |

r

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| COUNTER | 15:0 | r | **Counter [31:16]** |

## 5.4 PHY Registers

**PHY Control Register of Port 0**

| PHY_C0 | Offset | Reset Value |
|---|---|---|
| PHY Control Register of Port 0 | 200$_H$ | 3100$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RST | LPBK | SPEED_L* | ANEN | PDN | ISO | ANEN_RST | DPLX | COLT ST | SPEED_M* | | | Res | | | |
| rwsc | rw | rw | rw | rw | rw | rwsc | rw | rw | ro | | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| RST | 15 | rwsc | **RESET**<br>Setting this bit initiates the software reset function that resets the selected port, except for the phase-locked loop circuit. It will re-latch in all hardware configuration pin values The software reset process takes 25 µs to complete. This bit, which is self-clearing, returns a value of 1 until the reset process is complete.<br>0$_B$ Normal operation<br>1$_B$ PHY Reset |
| LPBK | 14 | rw | **Loop Back Enable**<br>This bit controls the PHY loopback operation that isolates the network transmitter outputs (TXP and TXN) and routes the MII transmit data to the MII receive data path. This function should only be used when auto negotiation is disabled (bit 12 = 0). The specific PHY (10Base-T or 100Base-X) used for this operation is determined by bits 12 and 13 of this register<br>0$_B$ Disable Loopback mode<br>1$_B$ Enable loopback mode |
| SPEED_LSB | 13 | rw | **Speed Selection LSB, 0.6, 0.13**<br>Link speed is selected by this bit or by auto negotiation if bit 12 of this register is set (in which case, the value of this bit is ignored).If it is fiber mode, 0.13 is always 1. Any write to this bit will have no effect.<br>00$_B$ 10 Mbit/s<br>01$_B$ 100 Mbit/s<br>10$_B$ 1000 Mbit/s<br>11$_B$ Reserved |
| ANEN | 12 | rw | **Auto Negotiation Enable**<br>This bit determines whether the link speed should set up by the auto negotiation process or not. It is set at power up or reset if the RECANEN pin detects a logic 1 input level in Twisted-Pair Mode.If it is set when fiber mode is configured, any write to this bit will be ignored .<br>0$_B$ Disable Auto negotiation process<br>1$_B$ Enable auto negotiation process |

| Field | Bits | Type | Description |
|---|---|---|---|
| PDN | 11 | rw | **Power Down Enable**<br>Ored result with PI_PWRDN pin. Setting this bit high or asserting the PI_PWRDN puts the PHY into power down mode. During the power down mode, TXP/TXN and all LED outputs are tristated and the MII interfaces are isolated.<br>$0_B$    Normal Operation<br>$1_B$    Power Down |
| ISO | 10 | rw | **Isolate PHY from Network**<br>Setting this control bit isolates the part from the MII, with the exception of the serial management interface. When this bit is asserted, the PHY does not respond to TXD, TXEN and TXER inputs, and it presents a high impedence on its TXC, RXC, CRSDV, RXER, RXD , COL and CRS outputs.<br>$0_B$    Normal Operation<br>$1_B$    Isolate PHY from MII |
| ANEN_RST | 9 | rwsc | **Restart Auto Negotiation**<br>Setting this bit while auto negotiation is enabled forces a new auto negotiation process to start. This bit is self-clearing and returns to 0 after the auto negotiation process has commenced.<br>$0_B$    Normal Operation<br>$1_B$    Restart Auto Negotiation Process |
| DPLX | 8 | rw | **Duplex Mode**<br>If auto negotiation is disabled, this bit determines the duplex mode for the link.<br>$0_B$    Half Duplex mode<br>$1_B$    Full Duplex mode |
| COLTST | 7 | rw | **Collision Test**<br>When set, this bit will cause the COL signal of MII interface to be asserted in response to the assertion of TXEN.<br>$0_B$    Disable COL signal test<br>$1_B$    Enable COL signal test |
| SPEED_MSB | 6 | ro | **Speed Selection MSB**<br>Set to 0 all the time indicate that the PHY does not support 1000 Mbit/s function. |

**Similar Registers**

All PHY_Cx registers have the same structure and characteristics, see **PHY_C0**.
The offset addresses of the other PHY_Cx registers are listed in **Table 47**.

**Table 47    PHY_Cx Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| PHY_C1 | PHY Control Register of Port 1 | $220_H$ | |
| PHY_C2 | PHY Control Register of Port 2 | $240_H$ | |
| PHY_C3 | PHY Control Register of Port 3 | $260_H$ | |
| PHY_C4 | PHY Control Register of Port 4 | $280_H$ | |

**PHY Status Register of Port 0**

| PHY_S0 | Offset | Reset Value |
|---|---|---|
| PHY Status Register of Port 0 | 201$_H$ | 7849$_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CAP_T4 | CAP_TXF | CAP_TXH | CAP_TF | CAP_TH | CAP_T2 | | Res | | CAP_SUPR | AN_COMP | REM_FLT | CAP_ANEG | LINK | JAB | EXTR EG |
| ro | ro | ro | ro | ro | ro | | | | ro | ro | ro | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| CAP_T4 | 15 | ro | **100Base-T4 Capable** <br> Set to 0 all the time to indicate that the PHY does not support 100Base-T4 |
| CAP_TXF | 14 | ro | **100Base-X Full Duplex Capable** <br> Set to 1 all the time to indicate that the PHY does support Full Duplex mode |
| CAP_TXH | 13 | ro | **100Base-X Half Duplex Capable** <br> Set to 1 all the time to indicate that the PHY does support Half Duplex mode |
| CAP_TF | 12 | ro | **10M Full Duplex Capable** <br> TP : Set to 1 all the time to indicate that the PHY does support 10M Full Duplex mode FX : Set to 0 all the time to indicate that the PHY does not support 10M Full Duplex mode |
| CAP_TH | 11 | ro | **10M Half Duplex Capable** <br> TP : Set to 1 all the time to indicate that the PHY does support 10M Half Duplex mode FX : Set to 0 all the time to indicate that the PHY does not support 10M Half Duplex mode |
| CAP_T2 | 10 | ro | **100Base-T2 Capable** <br> Set to 0 all the time to indicate that the PHY does not support 100Base-T2 |
| CAP_SUPR | 6 | ro | **MF Preamble Suppression Capable** <br> This bit is hardwired to 1 indicating that the PHY accepts management frame without preamble. Minimum 32 preamble bits are required following power-on or hardware reset. One idle bit is required between any two management transactions as per IEEE 802.3u specification. |
| AN_COMP | 5 | ro | **Auto Negotiation Complete** <br> If auto negotiation is enabled, this bit indicates whether the auto negotiation process has been completed or not. Set to 0 all the time when Fiber Mode is selected. <br> 0$_B$      Auto Negotiation process not completed <br> 1$_B$      Auto Negotiation process completed |

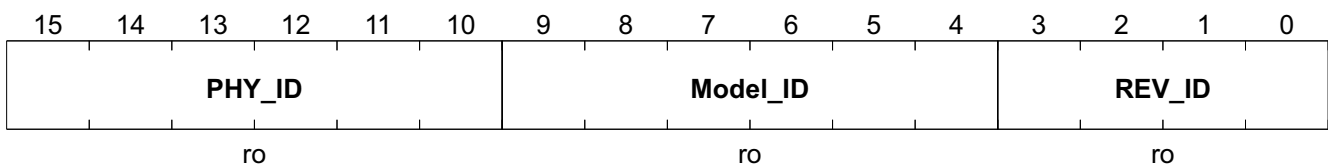| Field | Bits | Type | Description |
|-------|------|------|-------------|
| REM_FLT | 4 | ro | **Remote Fault Detect**<br>This bit is latched to 1 if the RF bit in the auto negotiation link partner ability register (bit 13, register address $05_H$) is set or the receive channel meets the far end fault indication function criteria. It is unlatched when this register is read.<br>$0_B$    Remote Fault not detected<br>$1_B$    Remote Fault detected |
| CAP_ANEG | 3 | ro | **Auto Negotiation Ability**<br>TP : This bit is set to 1 all the time, indicating that PHY is capable of auto negotiation. FX : This bit is set to 0 all the time, indicating that PHY is not capable of auto negotiation in Fiber Mode.<br>$0_B$    Not capable of auto negotiation<br>$1_B$    Capable of auto negotiation |
| LINK | 2 | ro | **Link Status**<br>This bit reflects the current state of the link – test-fail state machine. Loss of a valid link causes a 0 latched into this bit. It remains 0 until this register is read by the serial management interface. Whenever Linkup, this bit should be read twice to get link up status<br>$0_B$    Link is down<br>$1_B$    Link is up |
| JAB | 1 | ro | **Jabber Detect**<br>$0_B$    Jabber condition not detected<br>$1_B$    Jabber condition detected |
| EXTREG | 0 | ro | **Extended Capability**<br>This bit defaults to 1, indicating that the PHY implements extended registers.<br>$0_B$    No extended register set<br>$1_B$    Extended register set |

**Similar Registers**

All PHY_Sx registers have the same structure and characteristics, see **PHY_S0**.
The offset addresses of the other PHY_Sx registers are listed in **Table 48**.

**Table 48    PHY_Sx Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|----------------|-------------|
| PHY_S1 | PHY Status Register of Port 1 | $221_H$ | |
| PHY_S2 | PHY Status Register of Port 2 | $241_H$ | |
| PHY_S3 | PHY Status Register of Port 3 | $261_H$ | |
| PHY_S4 | PHY Status Register of Port 4 | $281_H$ | |

**PHY Identifier Register of Port 0 (A)**

| **PHY_I0_A** | **Offset** | **Reset Value** |
|---|---|---|
| **PHY Identifier Register of Port 0 (A)** | $202_H$ | $0302_H$ |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | PHY_ID | | | | | | | | |

ro
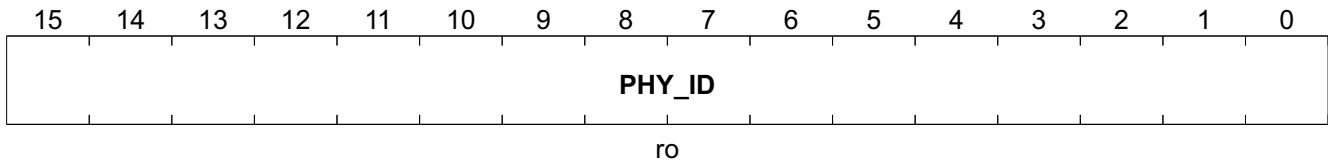
| Field | Bits | Type | Description |
|-------|------|------|-------------|
| PHY_ID | 15:0 | ro | **IEEE Address** |

**Similar Registers**

All PHY_Ix_A registers have the same structure and characteristics, see **PHY_I0_A**.
The offset addresses of the other PHY_Ix_A registers are listed in **Table 49**.

**Table 49     PHY_Ix_A Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|----------------|-------------|
| PHY_I1_A | PHY Identifier Register of Port 1 (A) | $222_H$ | |
| PHY_I2_A | PHY Identifier Register of Port 2 (A) | $242_H$ | |
| PHY_I3_A | PHY Identifier Register of Port 3 (A) | $262_H$ | |
| PHY_I4_A | PHY Identifier Register of Port 4 (A) | $282_H$ | |

**PHY Identifier Register of Port 0 (B)**

**PHY_I0_B**                                        Offset                                        Reset Value
**PHY Identifier Register of Port 0 (B)**          $203_H$                                        $6071_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | PHY_ID | | | | | | Model_ID | | | | | REV_ID | | |

ro                                     ro                                     ro

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| PHY_ID | 15:10 | ro | **IEEE Address** |
| Model_ID | 9:4 | ro | **IEEE Model No.** |
| REV_ID | 3:0 | ro | **IEEE Revision No.** |

**Similar Registers**

All PHY_Ix_B registers have the same structure and characteristics, see **PHY_I0_B**.
The offset addresses of the other PHY_Ix_B registers are listed in **Table 50**.

**Table 50     PHY_Ix_B Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|----------------|-------------|
| PHY_I1_B | PHY Identifier Register of Port 1 (B) | $223_H$ | |
| PHY_I2_B | PHY Identifier Register of Port 2 (B) | $243_H$ | |

**Table 50    PHY_Ix_B Registers** (cont'd)

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| PHY_I3_B | PHY Identifier Register of Port 3 (B) | 263$_H$ | |
| PHY_I4_B | PHY Identifier Register of Port 4 (B) | 283$_H$ | |

**Auto Negotiation Advertisement Register of Port 0**

**ANAP0**                                                **Offset**                                                **Reset Value**
**Auto Negotiation Advertisement Register of**          **204$_H$**                                                **05E1$_H$**
**Port 0**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NP | Res | RF | Res | ASM_DIR | PAUSE | T4 | TX_FDX | TX_HDX | 10_FDX | 10_HDX | | | SF | | |
| ro | | ro | | rw | rw | ro | rw | rw | rw | rw | | | ro | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| NP | 15 | ro | **Next Page**<br>This bit is defaults to 1, indicating that PHY is next page capable |
| RF | 13 | ro | **Remote Fault**<br>This bit is written by serial management interface for the purpose of communicating the remote fault condition to the auto negotiation link partner.<br>$0_B$    No remote fault has been detected<br>$1_B$    Remote Fault has been detected |
| ASM_DIR | 11 | rw | **Asymmetric Pause Direction**<br>Bit[ 11:10 ] Capability<br>$00_B$    No Pause<br>$01_B$    Symmetric PAUSE<br>$10_B$    Asymmetric PAUSE toward Link Partner<br>$11_B$    Both Symmetric PAUSE and Asymmetric PAUSE toward local device |
| PAUSE | 10 | rw | **Pause Operation for Full Duplex**<br>Value on PAUREC will be stored in this bit during power on reset. |
| T4 | 9 | ro | **Technology Ability for 100Base-T4**<br>Defaults to 0. |
| TX_FDX | 8 | rw | **100Base-TX Full Duplex**<br>$0_B$    Not capable of 100M Full duplex operation<br>$1_B$    Capable of 100M Full duplex operation |
| TX_HDX | 7 | rw | **100Base-TX Half Duplex**<br>$0_B$    Not capable of 100M operation<br>$1_B$    Capable of 100M operation |
| 10_FDX | 6 | rw | **10BASE-T Full Duplex**<br>$0_B$    Not capable of 10M full duplex operation<br>$1_B$    Capable of 10M Full Duplex operation |

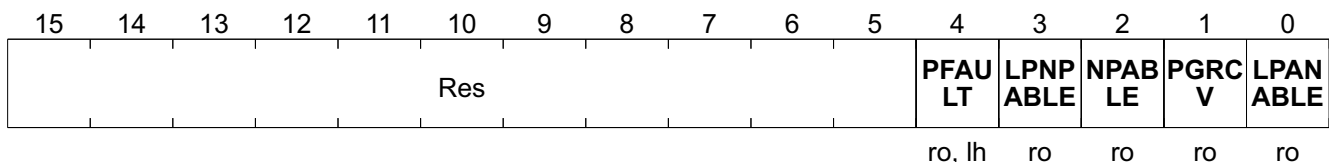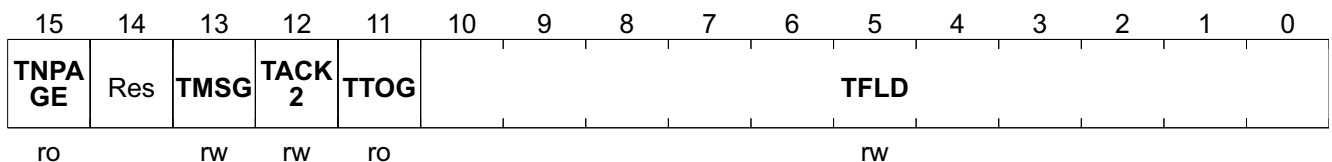| Field | Bits | Type | Description |
|-------|------|------|-------------|
| 10_HDX | 5 | rw | **10Base-T Half Duplex** <br><br> *Note: Bit 8:5 should be combined with REC100, RECFUL pin input to determine the finalized speed and duplex mode.* <br><br> $0_B$     Not capable of 10M operation <br> $1_B$     Capable of 10M operation |
| SF | 4:0 | ro | **Selector Field** <br> These 5 bits are hardwired to $00001_B$, indicating that the PHY supports IEEE 802.3 CSMA/CD. |

**Similar Registers**

All ANAPx registers have the same structure and characteristics, see **ANAP0**.
The offset addresses of the other ANAPx registers are listed in **Table 51**.

**Table 51    ANAPx Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|----------------|-------------|
| ANAP1 | Auto Negotiation Advertisement Register of Port 1 | $224_H$ | |
| ANAP2 | Auto Negotiation Advertisement Register of Port 2 | $244_H$ | |
| ANAP3 | Auto Negotiation Advertisement Register of Port 3 | $264_H$ | |
| ANAP4 | Auto Negotiation Advertisement Register of Port 4 | $284_H$ | |

**Auto Negotiation Link Partner Ability Register of Port 0**

**ANLPA0**                  **Offset**                **Reset Value**
**Auto Negotiation Link Partner Ability**      **$205_H$**              **$01E1_H$**
**Register of Port 0**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| NPAGE | ACK | RF | Res | LP_DIR | LP_PAU | LP_T4 | LP_FDX | LP_HDX | LP_F10 | LP_H10 | | | SF | | |
| ro | ro | ro | | ro | ro | ro | ro | ro | ro | ro | | | ro | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| NPAGE | 15 | ro | **Next Page** <br> $0_B$     Not capable of next page function <br> $1_B$     Capable of next page function |
| ACK | 14 | ro | **Acknowledge** <br> $0_B$     Not acknowledged <br> $1_B$     Link Partner acknowledges reception of the ability data word |
| RF | 13 | ro | **Remote Fault** <br> $0_B$     No remote fault has been detected <br> $1_B$     Remote Fault has been detected |
| LP_DIR | 11 | ro | **Link Partner Asymmetric Pause Direction** |

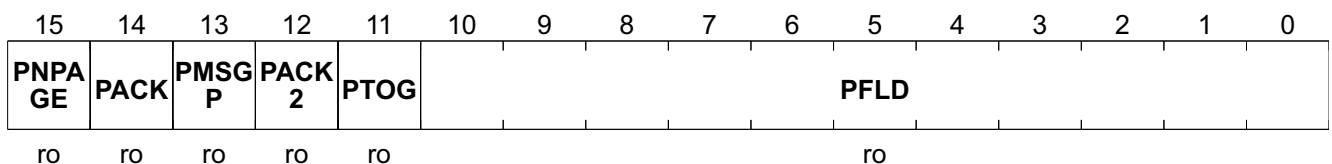| Field | Bits | Type | Description |
|-------|------|------|-------------|
| LP_PAU | 10 | ro | **Link Partner Pause CapabilityValue on PAUREC**<br>Will be stored in this bit during power on reset. |
| LP_T4 | 9 | ro | **Link Partner Technology Ability**<br>For 100Base-T4Defaults to 0. |
| LP_FDX | 8 | ro | **100Base-TX Full Duplex**<br>$0_B$    Not capable of 100M Full duplex operation<br>$1_B$    Capable of 100M Full duplex operation |
| LP_HDX | 7 | ro | **100Base-TX Half Duplex**<br>$0_B$    Not capable of 100M operation<br>$1_B$    Capable of 100M operation |
| LP_F10 | 6 | ro | **10BASE-T Full Duplex**<br>$0_B$    Not capable of 10M full duplex operation<br>$1_B$    Capable of 10M Full Duplex operation |
| LP_H10 | 5 | ro | **10Base-T Half Duplex**<br>$0_B$    Not capable of 10M operation<br>$1_B$    Capable of 10M operation |
| SF | 4:0 | ro | **Selector Field**<br>Encoding Definitions |

**Similar Registers**

All ANLPAx registers have the same structure and characteristics, see **ANLPA0**.
The offset addresses of the other ANLPAx registers are listed in **Table 52**.

**Table 52    ANLPAx Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|----------------|-------------|
| ANLPA1 | Auto Negotiation Link Partner Ability Register of Port 1 | $225_H$ | |
| ANLPA2 | Auto Negotiation Link Partner Ability Register of Port 2 | $245_H$ | |
| ANLPA3 | Auto Negotiation Link Partner Ability Register of Port 3 | $265_H$ | |
| ANLPA4 | Auto Negotiation Link Partner Ability Register of Port 4 | $285_H$ | |

**Auto Negotiation Expansion Register of Port 0**

| ANE0 | | Offset | | Reset Value |
|------|--|--------|--|-------------|
| **Auto Negotiation Expansion Register of Port 0** | | **$206_H$** | | **$0000_H$** |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | Res | | | | | | PFAULT | LPNPABLE | NPABLE | PGRCV | LPANABLE |
| | | | | | | | | | | | ro, lh | ro | ro | ro | ro |

| Field | Bits | Type | Description |
|---|---|---|---|
| PFAULT | 4 | ro, lh | **Parallel Detection Fault** |
| | | | $0_B$     No Fault Detect |
| | | | $1_B$     Fault has been detected |
| LPNPABLE | 3 | ro | **Link Partner Next Page Able** |
| | | | $0_B$     Link Partner is not next page capable |
| | | | $1_B$     Link Partner is next page capable |
| NPABLE | 2 | ro | **Next Page Able** |
| | | | Defaults to 0, indicating PHY is not capable of next page. |
| PGRCV | 1 | ro | **Page Received** |
| | | | $0_B$     No new page has been received |
| | | | $1_B$     A new page has been received |
| LPANABLE | 0 | ro | **Link Partner Auto Negotiation Able** |
| | | | $0_B$     Link Partner is not auto negotiable |
| | | | $1_B$     Link Partner is auto negotiable |

**Similar Registers**

All ANEx registers have the same structure and characteristics, see **ANE0**.
The offset addresses of the other ANEx registers are listed in **Table 53**.

**Table 53     ANEx Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| ANE1 | Auto Negotiation Expansion Register of Port 1 | $226_H$ | |
| ANE2 | Auto Negotiation Expansion Register of Port 2 | $246_H$ | |
| ANE3 | Auto Negotiation Expansion Register of Port 3 | $266_H$ | |
| ANE4 | Auto Negotiation Expansion Register of Port 4 | $286_H$ | |

**Next Page Transmit Register of Port 0**

**NPT0**                        **Offset**                                    **Reset Value**
**Next Page Transmit Register of Port 0**         $207_H$                        $2001_H$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TNPAGE | Res | TMSG | TACK2 | TTOG | | | | | | TFLD | | | | | |
| ro | | rw | rw | ro | | | | | | rw | | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| TNPAGE | 15 | ro | **Transmit Next Page** |
| | | | Transmit Code Word Bit 15 |
| TMSG | 13 | rw | **Transmit Message Page** |
| | | | Transmit Code Word Bit 13 |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| TACK2 | 12 | rw | **Transmit Acknowledge 2**<br>Transmit Code Word Bit 12 |
| TTOG | 11 | ro | **Transmit Toggle**<br>Transmit Code Word Bit 11 |
| TFLD | 10:0 | rw | **Transmit Message Field**<br>Transmit Code Word Bit 10..0 |

**Similar Registers**

All NPTx registers have the same structure and characteristics, see **NPT0**.
The offset addresses of the other NPTx registers are listed in **Table 54**.

**Table 54     NPTx Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---------------------|--------------------|----------------|-------------|
| NPT1 | Next Page Transmit Register of Port 1 | 227$_H$ | |
| NPT2 | Next Page Transmit Register of Port 2 | 247$_H$ | |
| NPT3 | Next Page Transmit Register of Port 3 | 267$_H$ | |
| NPT4 | Next Page Transmit Register of Port 4 | 287$_H$ | |

**Link Partner Next Page Register of Port 0**

| LPNP0 | | | | | Offset | | | | | | | Reset Value | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Link Partner Next Page Register of Port 0 | | | | | 208$_H$ | | | | | | | 0000$_H$ | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| PNPAGE | PACK | PMSGP | PACK2 | PTOG | | | | | PFLD | | | | | | |
| ro | ro | ro | ro | ro | | | | | ro | | | | | | |

| Field | Bits | Type | Description |
|-------|------|------|-------------|
| PNPAGE | 15 | ro | **Link Partner Next Page**<br>Receive Code Word Bit 15 |
| PACK | 14 | ro | **Link Partner Acknowledge**<br>Receive Code Word Bit 14 |
| PMSGP | 13 | ro | **Link Partner Message Page**<br>Receive Code Word Bit 13 |
| PACK2 | 12 | ro | **Link Partner Acknowledge 2**<br>Receive Code Word Bit 12 |
| PTOG | 11 | ro | **Link Partner Toggle**<br>Receive Code Word Bit 11 |
| PFLD | 10:0 | ro | **Link Partner Message Field**<br>Receive Code Word Bit 11 |

**Similar Registers**

All LPNPx registers have the same structure and characteristics, see **LPNP0**.

The offset addresses of the other LPNPx registers are listed in **Table 55**.

**Table 55    LPNPx Registers**

| Register Short Name | Register Long Name | Offset Address | Page Number |
|---|---|---|---|
| LPNP1 | Link Partner Next Page Register of Port 1 | $228_H$ | |
| LPNP2 | Link Partner Next Page Register of Port 2 | $248_H$ | |
| LPNP3 | Link Partner Next Page Register of Port 3 | $268_H$ | |
| LPNP4 | Link Partner Next Page Register of Port 4 | $288_H$ | |

# 6    Hardware, EEPROM and SMI Interface for Configuration

Three ways are supported to configure the setting in the ADM6996LC/LCX/LHX: (1) Hardware Setting (2) EEPROM Interface (3) SMI Interface. Users could use EEPROM and SMI interfaces combined with the CPU port to provide proprietary functions. Four pins are needed when using these two interfaces. See **Figure 14** for the description.
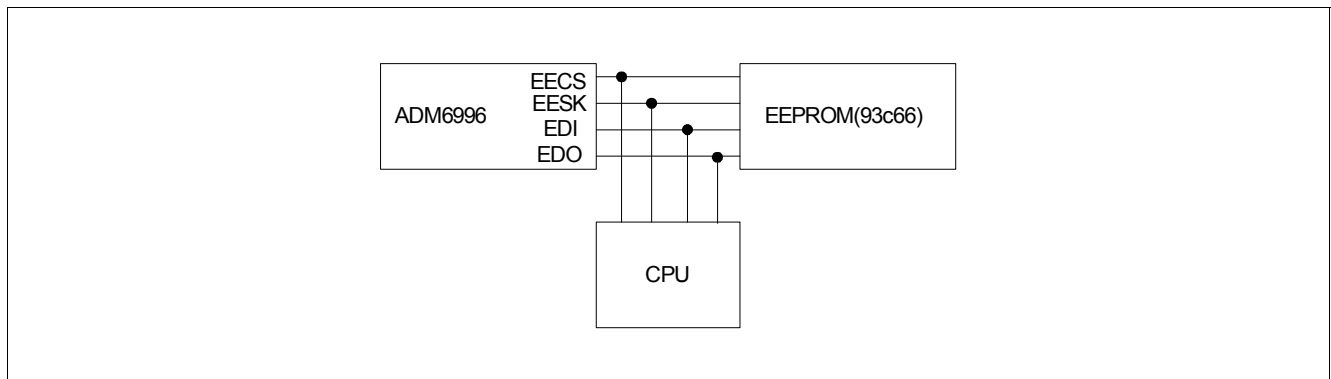


**Figure 14    Interconnection between ADM6996LC/LCX/LHX, EEPROM and CPU**

## 6.1    Hardware Setting

The ADM6996LC/LCX/LHX provides some hardware pins, where values reside on will be strapped for the default setting during the power on or reset.

**Table 56    Hardware Setting**

| Setting Name | Description |
|---|---|
| GFCEN | Global Flow Control Enable.<br>$0_B$    Flow Control Capability is depended upon the register setting in corresponding EEPROM register<br>$1_B$    All ports flow control capability is enabled. |
| SDIO_MD | SDC/SDIO mode selection.<br>$0_B$    16 bits mode<br>$1_B$    32 bits mode |

**Table 56    Hardware Setting** (cont'd)

| Setting Name | Description |
|---|---|
| P5_BUSMD[1:0] | Port 5 bus mode selection bit 0.<br>P5_BUSMD[1:0] ,Interface<br>$00_B$    MII<br>$01_B$    GPSI<br>$10_B$    RMII<br>$11_B$    Reserved and Not Allowed. |
| BPEN | Recommend Back-Pressure in half-duplex.<br>$0_B$    Disable Back-Pressure.<br>$1_B$    Enable Back-Pressure |
| RECANEN | Recommend Auto Negotiation Enable. Only valid for Twisted pair interface. Programmed this bit to 1 has no effect to Fiber port.<br>$0_B$    Disable all TP port auto negotiation capability<br>$1_B$    Enable all TP port auto negotiation capability |
| XOVEN | Cross Over Enable.  Only available in TP interface.<br>$0_B$    Disable<br>$1_B$    Enable |
| LED_MODE | Enable Mac to choose LED Display Mode.<br>$0_B$    Single color LED<br>$1_B$    Dual color LED |

## 6.2    EEPROM Interface

The EEPROM Interface is provided so the users could easily configure the setting without CPU's help. Because the EEPROM Interface is the same as the 93c66, it also allows the CPU to write the EEPROM register and renew the 93c66 at the same time. After the power up or reset (default value from the hardware pins fetched in this stage), the ADM6996LC/LCX/LHX will automatically detect the presence of the EEPROM by reading the address 0 in the 96c66. If the value = $4154_H$, it will load all the data in the 93c66. If not, the ADM6996LC/LCX/LHX will stop loading the 93c66. The user also could pull down the EDO to force the ADM6996LC/LCX/LHX not to load the 93c66. The 93c66 loading time is around 30ms. Then CPU should drive the high-z value in the EECS, EESK and EDI pins in this period if existing the CPU to read or write the registers in the ADM6996LC/LCX/LHX.

The EEPROM Interface needs only one Write command to complete a "Write" operation to the ADM6996LC/LCX/LHX. If users would like to update the 93c66 at the same time, then three commands, Write Enable, Write, and Write Disable, are needed to complete this operation (See 93c66 Spec. for the reference). User should note that the EERPOM interface only allows the CPU to write the EEPROM register in the ADM6996LC/LCX/LHX and doesn't support the READ command. If CPU sends out the Read Command, then 93c66 will respond with the value inside, instead of ADM6996LC/LCX/LHX. Users should also note that one additional EESK cycle is needed between any continuous commands (Read or Write).

(1) Read 93c66 via the EEPROM Interface (Index = 2, Data = $1111_H$).
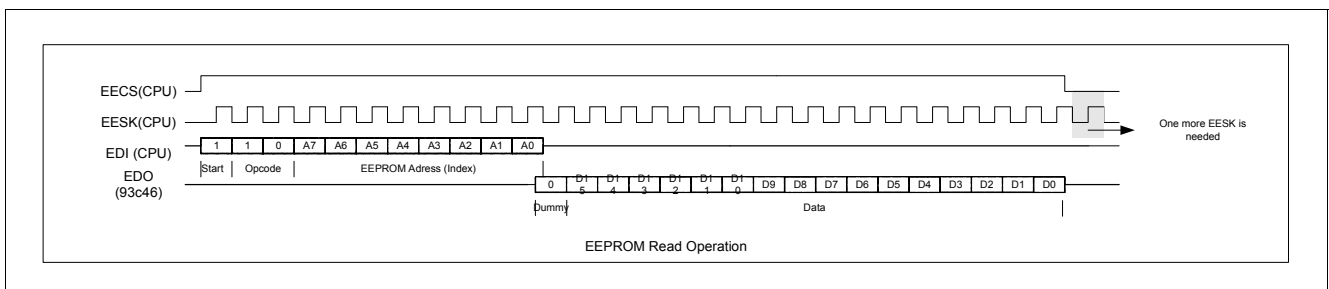
(2) Write EEPROM registers in the ADM6996LC/LCX/LHX (Index = 2, Data =16'h2222).



EEPROM Write Operation
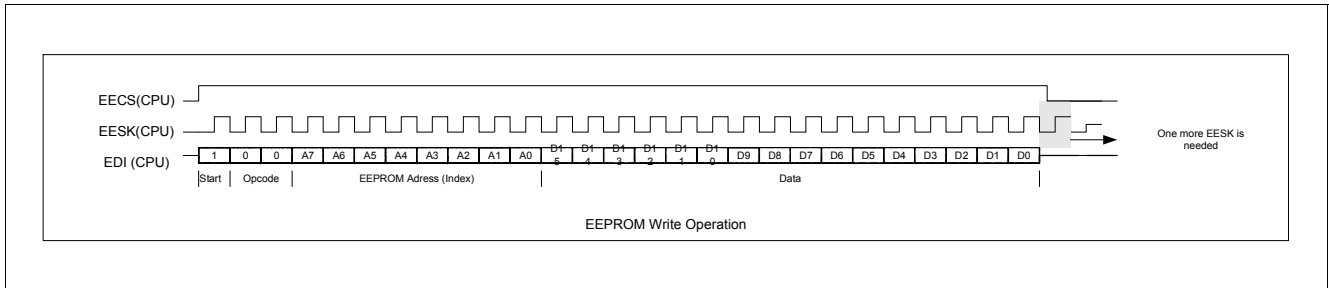
## 6.3 SMI Interface

The SMI consists of two pins, management data clock (EESK) and management data input/output (EDI). The ADM6996LC/LCX/LHX is designed to support an EESK frequency up to 25 MHz. The EDI pin is bi-directional and may be shared with other devices. EECS pin is needed to pull low if EEPROM interface is also used.

The EDI pin requires a 1.5 KΩ pull-up which, during idle and turnaround periods, will pull EDI to a logic one state. ADM6996LC/LCX/LHX requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. The first 32 bits are preamble consisting of 32 contiguous logic one bits on EDI and 32 corresponding cycles on EESK. Following preamble is the start-of-frame field indicated by a $<01_B>$ pattern. The next field signals the operation code (OP): $<10_B>$ indicates read from management register operation, and $<01_B>$ indicates write to management register operation. The next field is the management register address. It is 10 bits wide and the most significant bit is transferred first.

During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the EDI to avoid contention. Following the turnaround time, a 16-bit data stream is read from or written into the management registers of the ADM6996LC/LCX/LHX.

**(A) Preamble Suppression**

The SMI of ADM6996LC/LCX/LHX supports a preamble suppression mode. The ADM6996LC/LCX/LHX requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. This requirement is generally met by pulling-up the resistor of EDI While the ADM6996LC/LCX/LHX will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required.

When ADM6996LC/LCX/LHX detects that there is address match, then it will enable Read/Write capability for external access. When address is mismatched, then ADM6996LC/LCX/LHX will tri-state the EDI pin.

**(B) Read Switch Register via SMI Interface (Offset Hex = 10'h2, Data = 16'h2600)**



SMI Read Operation
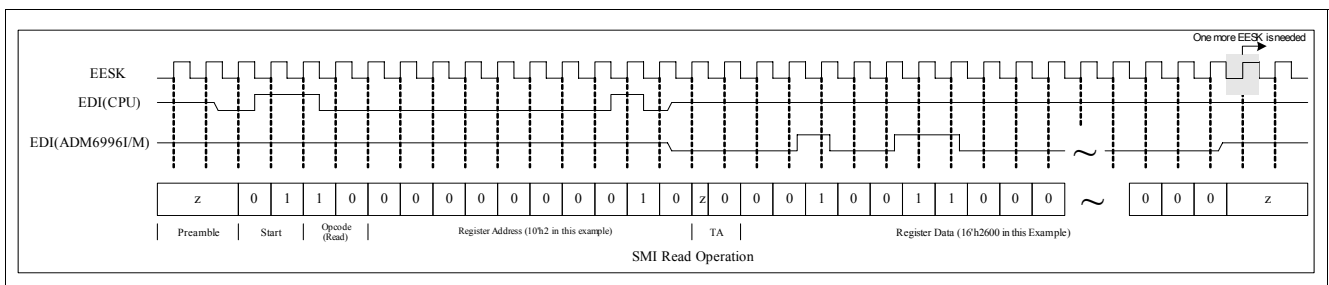
**(C) Write Switch Register via SMI Interface (Offset Hex = 10'h180, Data = 16'h1300)**

One more EESK is needed

EESK
EDI (CPU)

| z | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | ~ | 0 | 0 | 0 | z |

Preamble | Start | Opcode (Write) | Register Address ( 10'h180 in this example) | TA | Register Data (16'h1300 in this Example)
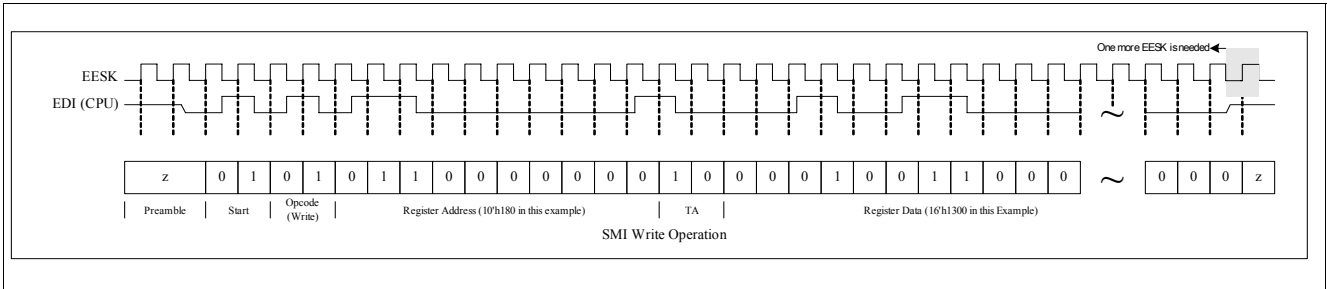
SMI Write Operation

**Table 57    (D) The Pin Type of EECS, EESK, EDI and EDO during the Operation**

| Pin Name | Reset Operation | Load EEPROM | Write Operation | Read Operation |
|---|---|---|---|---|
| EECS | Input | Output | Input | Input |
| EESK | Input | Output | Input | Input |
| EDI | Input | Output | Input | Input/Output |
| EDO | Input | Input | Input | Input |

# 7 Electrical Specification

## 7.1 TX/FX Interface

## 7.1.1 TP Interface
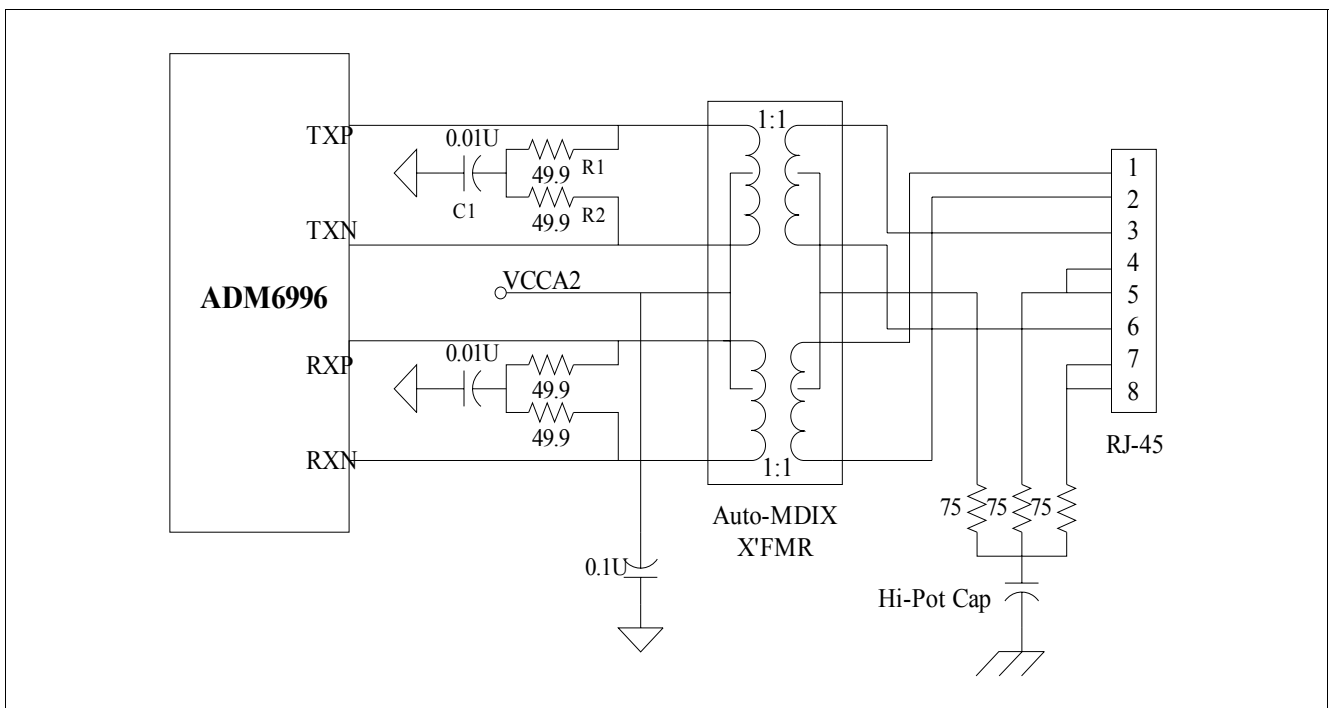


**Figure 15 TP Interface**

Transformer requirements:

• TX/RX rate 1:1
• TX/RX central tap connect together to VCCA2

Users can change the TX/RX pin for easy layout but do not change the polarity. ADM6996LC/LCX/LHX supports auto polarity on the receiving side.

## 7.1.2 FX Interface
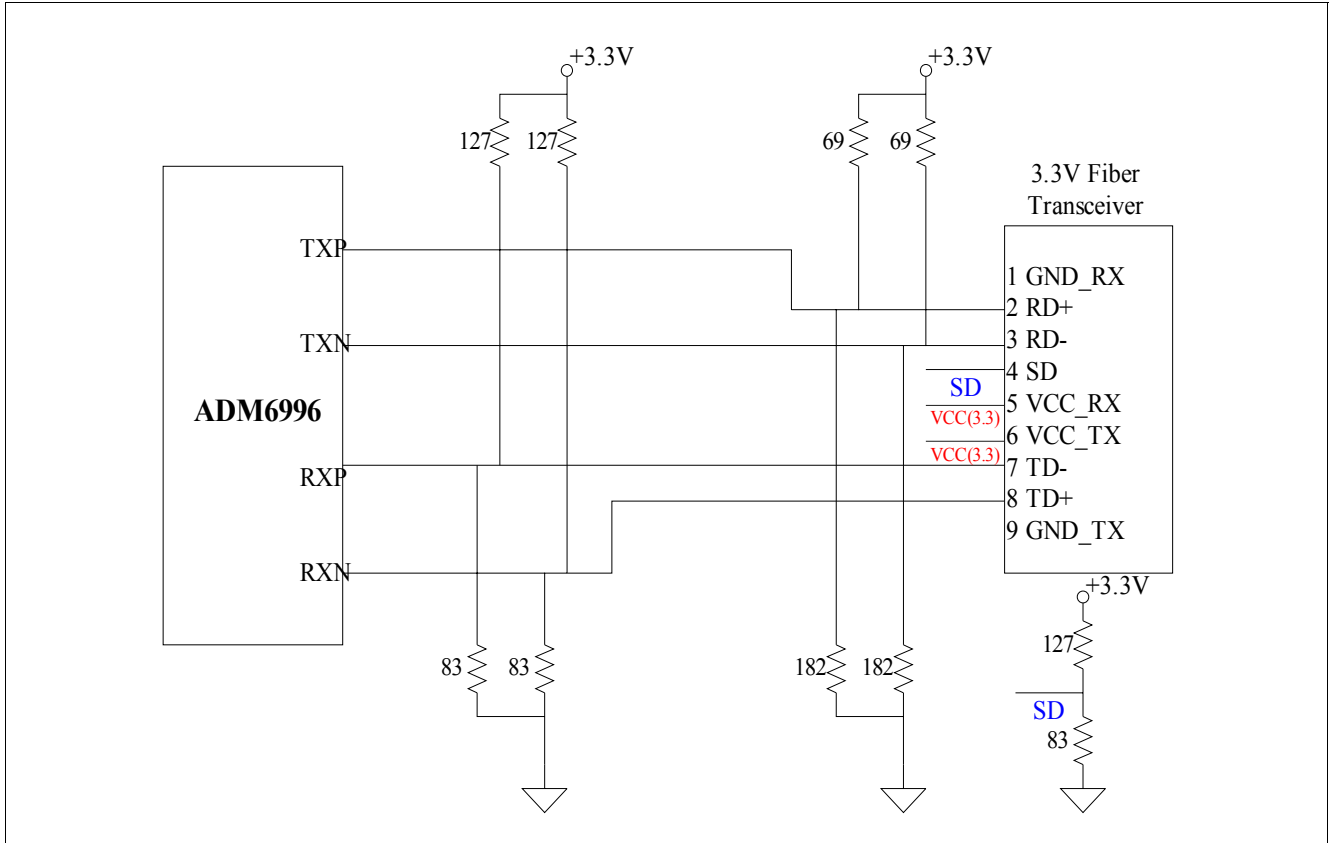


**Figure 16    FX Interface**

## 7.2    DC Characterization

**Table 58    Power Consumption**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| Power consumption when all twisted pair ports are linked at 100 Mbit/s. | $P_{100M\_5TP}$ | – | 980 | – | mW | Under EEPROM Register $29_H = C000_H$, and $30_H = 985_H$ |
| Power consumption when all twisted pair ports are linked at 10 Mbit/s (include transformer). | $P_{10M\_5TP}$ | – | 1450 | – | mW | Under EEPROM Register $29_H = C000_H$, and $30_H = 985_H$ |
| Power consumption when all twisted pair ports are disconnected. | $P_{DIS\_5TP}$ | – | 500 | – | mW | Under EEPROM Register $29_H = C000_H$, and $30_H = 985_H$ |

**Table 59    Absolute Maximum Ratings**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| 3.3 V Power Supply for I/O pad | $V_{CC3O}$ | 2.97 | 3.3 | 3.63 | V | – |
| 3.3 V Power Supply for bias circuit | $V_{CCBS}$ | 2.97 | 3.3 | 3.63 | V | – |
| 3.3 V Power Supply for A/D converter | $V_{CCAD}$ | 2.97 | 3.3 | 3.63 | V | – |
| 1.8 V Power Supply for line driver | $V_{CCA2}$ | 1.62 | 1.8 | 1.98 | V | – |
| 1.8 V Power Supply for PLL | $V_{CCPLL}$ | 1.62 | 1.8 | 1.98 | V | – |
| 1.8 V Power Supply for Digital core | $V_{CCIK}$ | 1.62 | 1.8 | 1.98 | V | – |
| Input Voltage | $V_{IN}$ | -0.3 | – | $V_{CC3O}$ + 0.3 | V | – |
| Output Voltage | $V_{out}$ | -0.3 | – | $V_{CC3O}$ + 0.3 | V | – |
| Maximum current for 3.3 V power supply | $I_{3.3VMAX}$ | – | – | 100 | mA | – |
| Maximum current for 1.8 V power supply (include transformer) | $I_{1.8VMAX}$ | – | – | 800 | mA | – |
| Storage Temperature | $T_{STG}$ | -55 | – | 155 | °C | – |
| ESD Rating | $ESD$ | 1.0 | – | – | kV | – |

*Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.*

**Table 60    Recommended Operating Conditions**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| 3.3 V Power Supply for I/O pad | $V_{CC3O}$ | 3.135 | 3.3 | 3.465 | V | – |
| 3.3 V Power Supply for bias circuit | $V_{CCBS}$ | 3.135 | 3.3 | 3.465 | V | – |
| 3.3 V Power Supply for A/D converter | $V_{CCAD}$ | 3.135 | 3.3 | 3.465 | V | – |
| 1.8 V Power Supply for line driver | $V_{CCA2}$ | 1.71 | 1.8 | 1.89 | V | – |
| 1.8 V Power Supply for PLL | $V_{CCPLL}$ | 1.71 | 1.8 | 1.89 | V | – |
| 1.8 V Power Supply for Digital core | $V_{CCIK}$ | 1.71 | 1.8 | 1.89 | V | – |
| Input Voltage | $V_{in}$ | 0 | – | $V_{CC}$ | V | – |
| Junction Operating Temperature | $T_j$ | 0 | 25 | 115 | °C | – |

**Table 61    DC Electrical Characteristics for 3.3 V Operation[1]**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input Low Voltage | $V_{IL}$ | – | – | 0.8 | V | TTL |
| Input High Voltage | $V_{IH}$ | 2.0 | – | – | V | TTL |
| Output Low Voltage | $V_{OL}$ | – | – | 0.4 | V | TTL |
| Output High Voltage | $V_{OH}$ | 2.4 | – | – | V | TTL |
| Input Pull-up/down Resistance | $R_I$ | – | 50 | – | kΩ | $V_{IL}$ = 0 V or $V_{IH}$ = $V_{cc3o}$ |

1)  Under $V_{CC3O}$ = 2.97V ~ 3.63 V, $T_j$ = 0 °C ~ 115 °C

## 7.3    AC Characterization

### 7.3.1    XTAL/OSC Timing
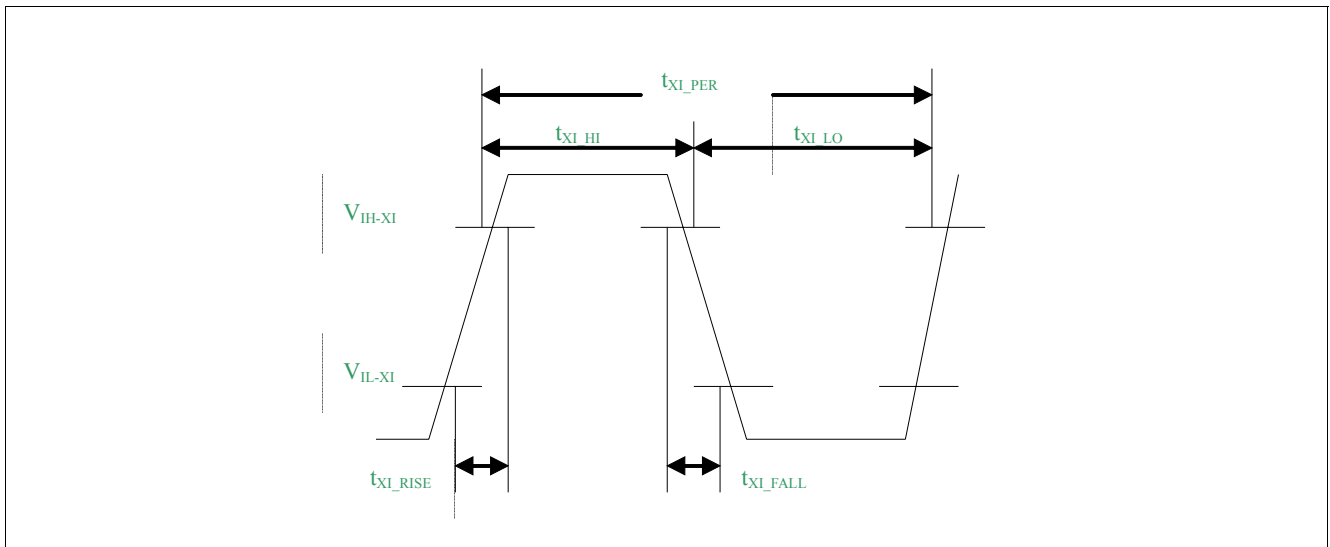


**Figure 17    XTAL/OSC Timing**

**Table 62    XTAL/OSC Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| XI/OSCI Clock Period | $t_{\_XI\_PER}$ | 40.0 - 50ppm | 40.0 | 40.0 + 50ppm | ns | – |
| XI/OSCI Clock High | $t_{\_XI\_HI}$ | 14 | 20.0 | – | ns | – |
| XI/OSCI Clock Low | $t_{\_XI\_LO}$ | 14 | 20.0 | – | ns | – |
| XI/OSCI Clock Rise Time, $V_{IL}$ (max) to $V_{IH}$ (min.) | $t_{\_XI\_RISE}$ | – | – | 4 | ns | – |
| XI/OSCI Clock Fall Time, $V_{IH}$ (min.) to $V_{IL}$ (max) | $t_{\_XI\_FALL}$ | – | – | 4 | ns | – |

## 7.3.2 Power On Reset
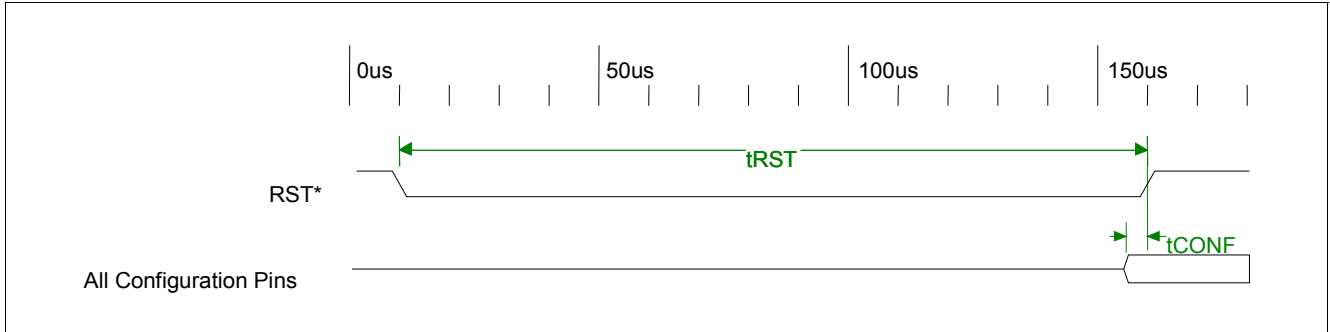


**Figure 18 Power On Reset Timing**

**Table 63 Power On Reset Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| RST Low Period | $t_{RST}$ | 100 | – | – | ms | – |
| Start of Idle Pulse Width | $t_{CONF}$ | 100 | – | – | ns | – |

## 7.3.3 EEPROM Interface Timing
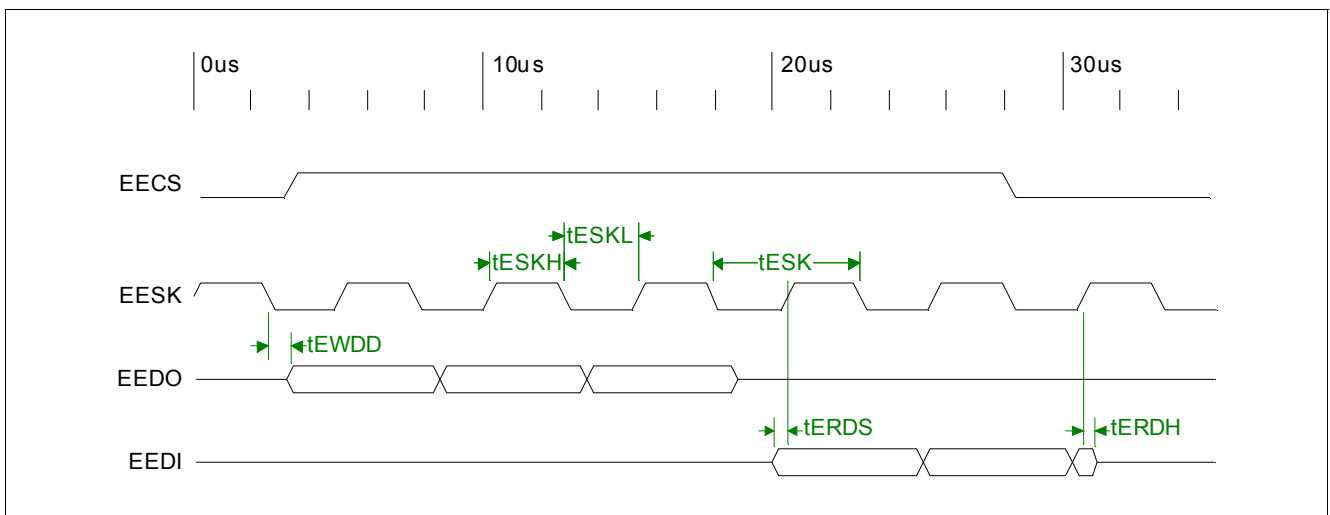


**Figure 19 EEPROM Interface Timing**

**Table 64 EEPROM Interface Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| EESK Period | $t_{ESK}$ | – | 5120 | – | ns | – |
| EESK Low Period | $t_{ESKL}$ | 2550 | – | 2570 | ns | – |
| EESK High Period | $t_{ESKH}$ | 2550 | – | 2570 | ns | – |

**Table 64    EEPROM Interface Timing** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| EEDI to EESK Rising Setup Time | $t_{ERDS}$ | 10 | – | – | ns | – |
| EEDI to EESK Rising Hold Time | $t_{ERDH}$ | 10 | – | – | ns | – |
| EESK Falling to EEDO Output Delay Time | $t_{EWDD}$ | – | – | 20 | ns | – |

## 7.3.4    10Base-TX MII Input Timing
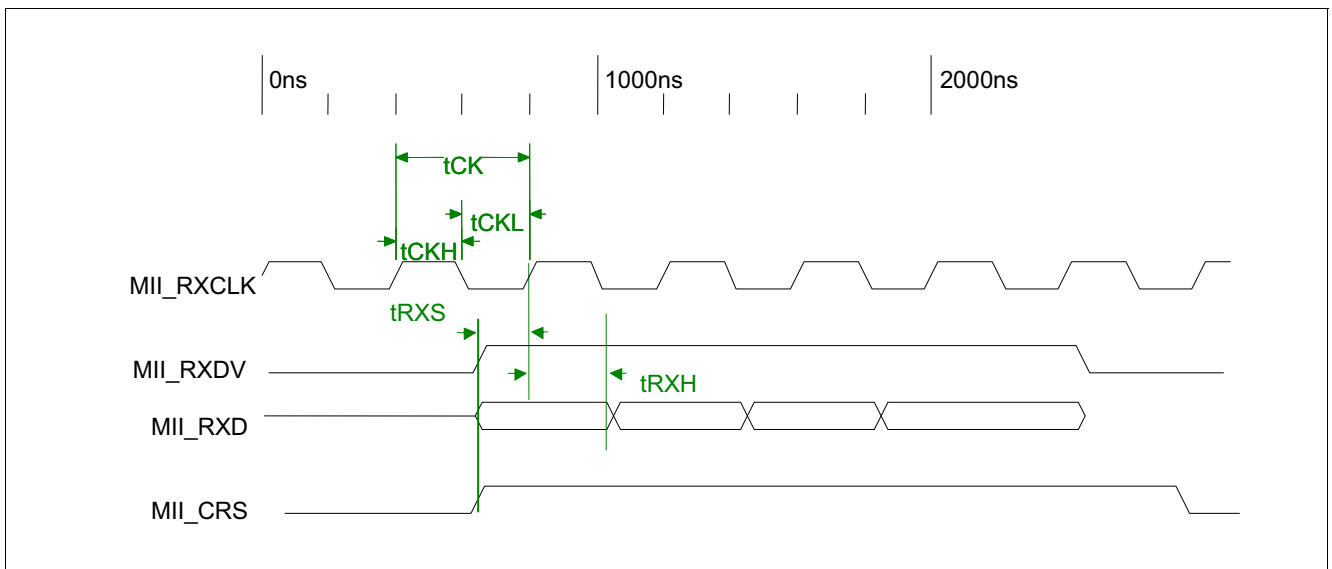


**Figure 20    10Base-TX MII Input Timing**

**Table 65    10Base-TX MII Input Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| MII_RXCLK Period | $t_{CK}$ | – | 400 | – | ns | – |
| MII_RXCLK Low Period | $t_{CKL}$ | 180 | – | 220 | ns | – |
| MII_RXCLK High Period | $t_{CKH}$ | 180 | – | 220 | ns | – |
| MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising setup | $t_{RXS}$ | 10 | – | – | ns | – |
| MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising hold | $t_{RXH}$ | 10 | – | – | ns | – |

## 7.3.5     10Base-TX MII Output Timing
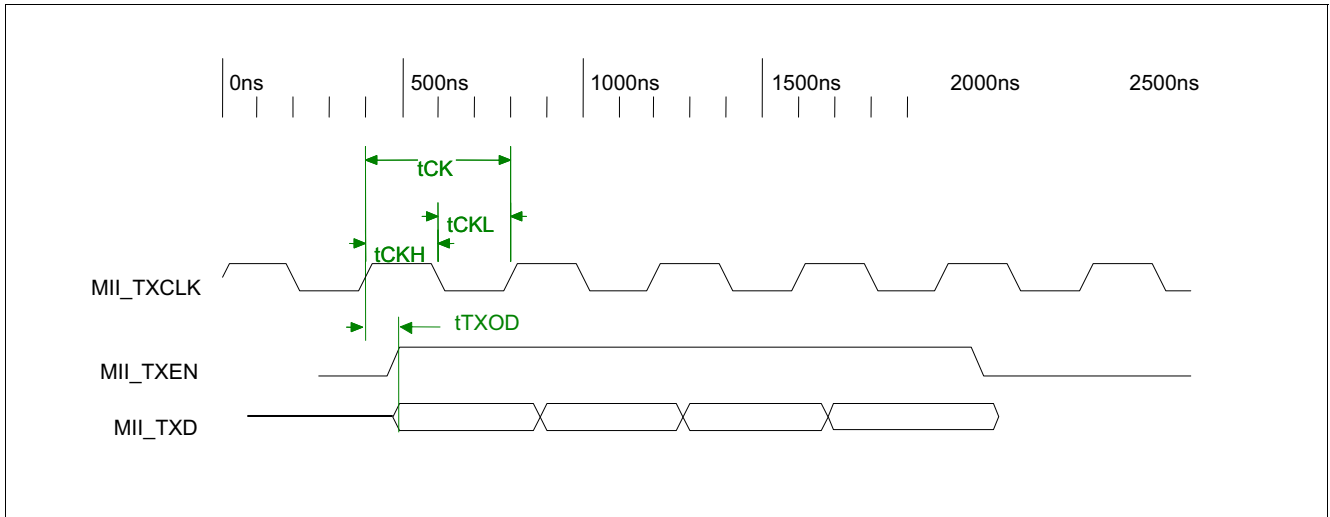


**Figure 21     10Base-TX MII Output Timing**

**Table 66     10-Base-TX MII Output Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| MII_TXCLK Period | $t_{CK}$ | – | 400 | – | ns | – |
| MII_TXCLK Low Period | $t_{CKL}$ | 180 | – | 220 | ns | – |
| MII_TXCLK High Period | $t_{CKH}$ | 180 | – | 220 | ns | – |
| MII_TXD, MII_TXEN toMII_TXCLK Rising Output Delay | $t_{TXOD}$ | 0 | – | 25 | ns | – |

## 7.3.6 100Base-TX MII Input Timing
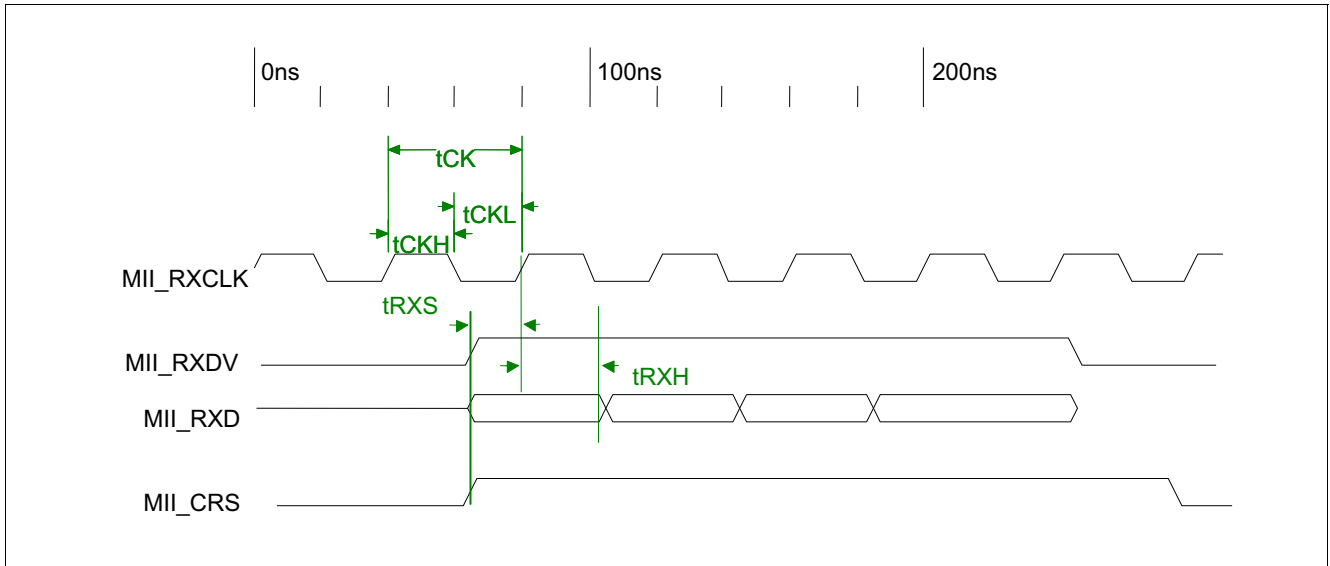


**Figure 22    100Base-TX MII Input Timing**

**Table 67     100Base-TX MII Input Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| MII_RXCLK Period | $t_{CK}$ | – | 40 | – | ns | – |
| MII_RXCLK Low Period | $t_{CKL}$ | 18 | – | 22 | ns | – |
| MII_RXCLK High Period | $t_{CKH}$ | 18 | – | 22 | ns | – |
| MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising setup | $t_{RXS}$ | 10 | – | – | ns | – |
| MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising hold | $t_{RXH}$ | 10 | – | – | ns | – |

## 7.3.7    100Base-TX MII Output Timing
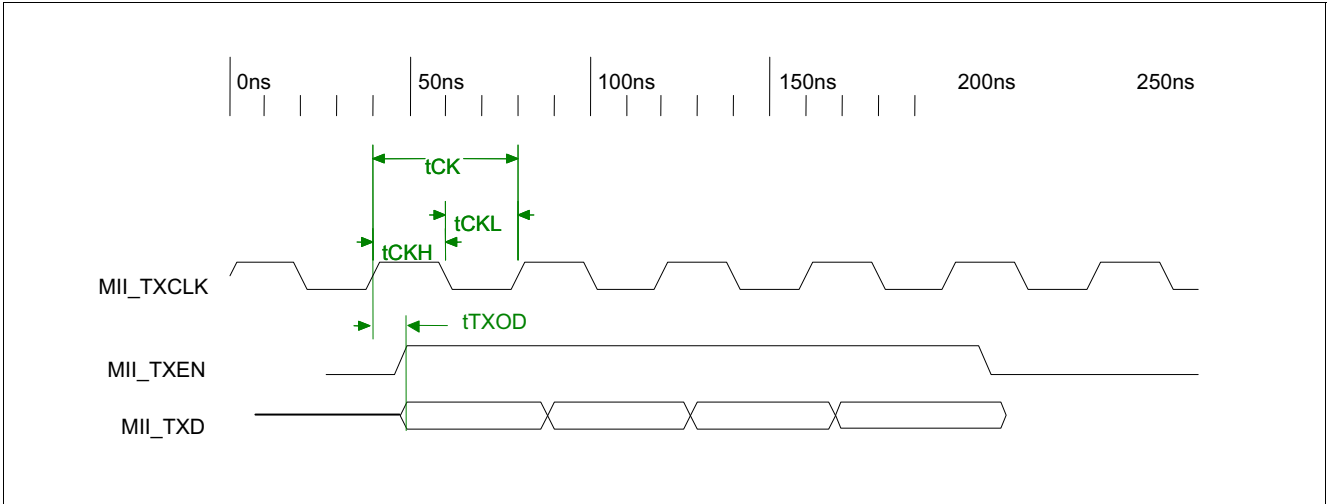


**Figure 23    100Base-TX MII Output Timing**

**Table 68    100Base-TX MII Output Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| MII_TXCLK Period | $t_{CK}$ | – | 40 | – | ns | – |
| MII_TXCLK Low Period | $t_{CKL}$ | 18 | – | 22 | ns | – |
| MII_TXCLK High Period | $t_{CKH}$ | 18 | – | 22 | ns | – |
| MII_TXD, MII_TXEN toMII_TXCLK Rising Output Delay | $t_{TXOD}$ | 0 | – | 25 | ns | – |

## 7.3.8    RMII REFCLK Input Timing
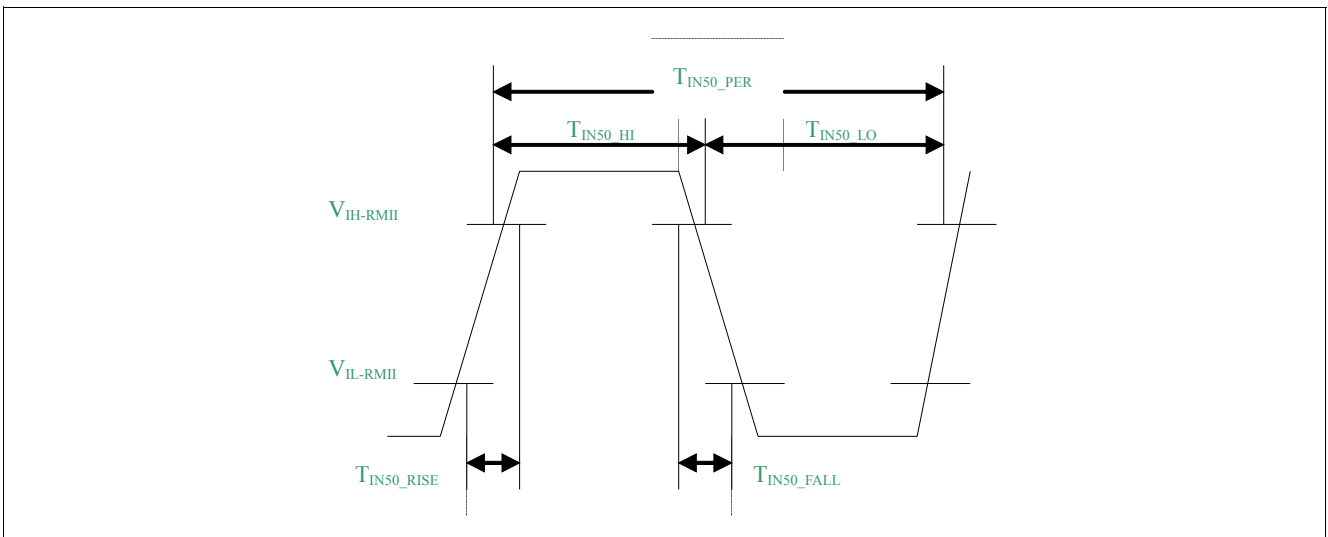


**Figure 24    RMII REFCLK Input Timing**

**Table 69    RMII REFCLK Input Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| REFCLK Clock Period | $t_{IN50\_PER}$ | 40.0 - 50ppm | 40.0 | 40.0 + 50ppm | ns | – |
| REFCLK Clock High | $t_{IN50\_HI}$ | 14 | 20.0 | – | ns | – |
| REFCLK Clock Low | $t_{IN50\_LO}$ | 14 | 20.0 | – | ns | – |
| REFCLK Clock Rise Time, $V_{IL}$ (max) to $V_{IH}$ (min.) | $t_{IN50\_RISE}$ | – | – | 2 | ns | – |
| REFCLK Clock Fall Time, $V_{IH}$ (min.) to $V_{IL}$ (max) | $t_{IN50\_FALL}$ | – | – | 2 | ns | – |

## 7.3.9    RMII REFCLK Output Timing
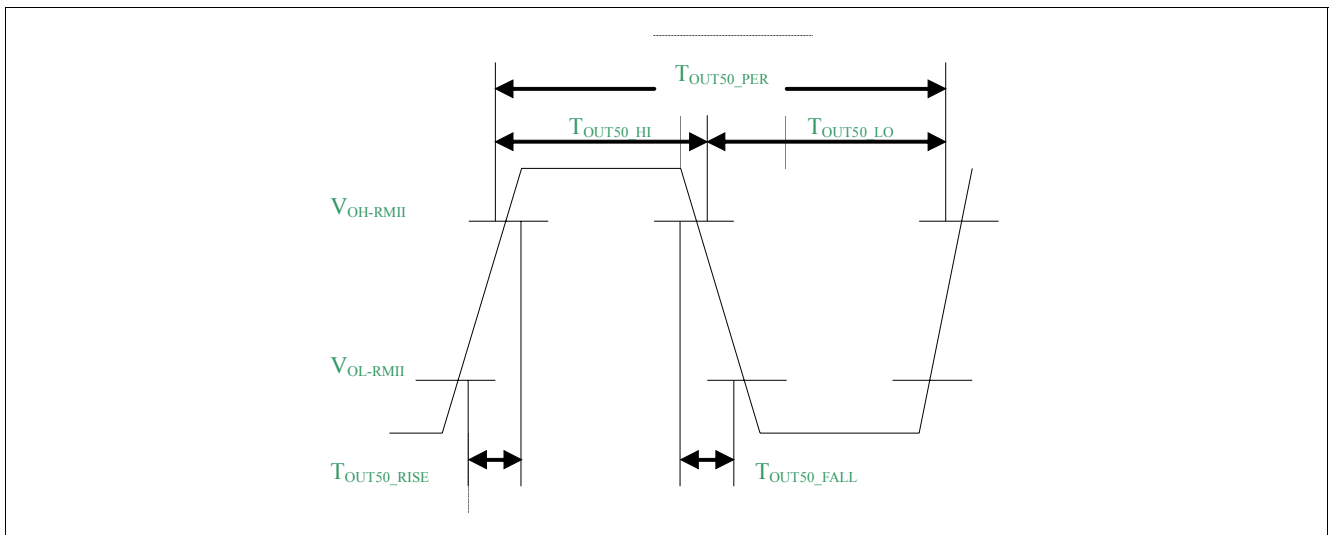


**Figure 25    RMII REFCLK Output Timing**

**Table 70    RMII REFCLK Output Timing**

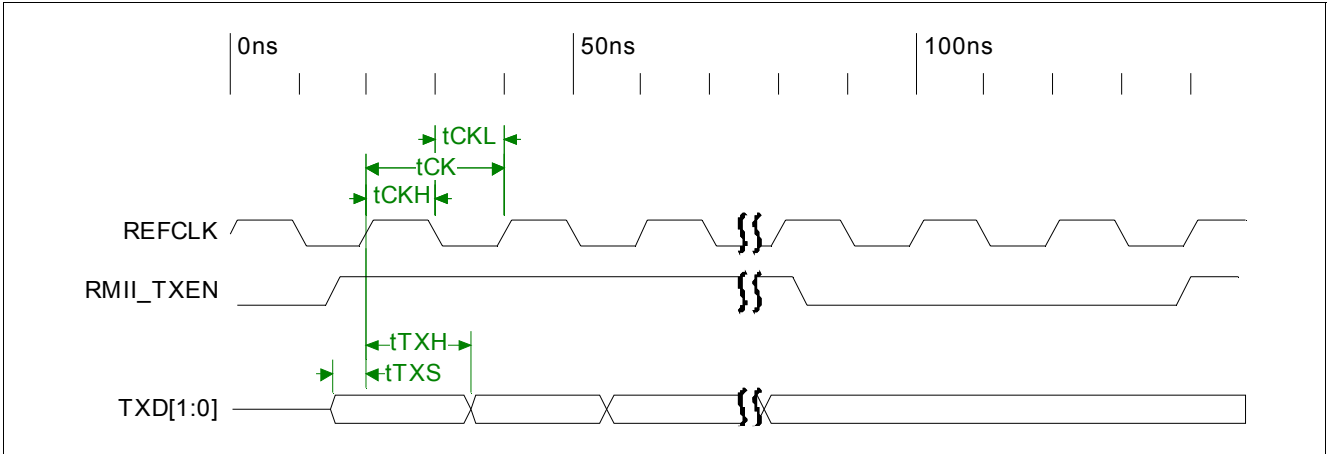| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| REFCLK Clock Period | $t_{OUT50\_PER}$ | 40.0 - 50ppm | 40.0 | 40.0 + 50ppm | ns | – |
| REFCLK Clock High | $t_{OUT50\_HI}$ | 14 | 20.0 | 26 | ns | – |
| REFCLK Clock Low | $t_{OUT50\_LO}$ | 14 | 20.0 | 26 | ns | – |
| REFCLK Clock Rise Time, $V_{OL}$ (max) to $V_{OH}$ (min.) | $t_{OUT50\_RISE}$ | – | – | 2 | ns | – |
| REFCLK Clock Fall Time, $V_{OH}$ (min.) to $V_{OL}$ (max) | $t_{OUT50\_FALL}$ | – | – | 2 | ns | – |
| REFCLK Clock Jittering (p-p) | $t_{OUT50\_JIT}$ | – | 0.15 | – | ns | – |

## 7.3.10 Reduce MII Timing



**Figure 26** Reduce MII Timing (1 of 2)
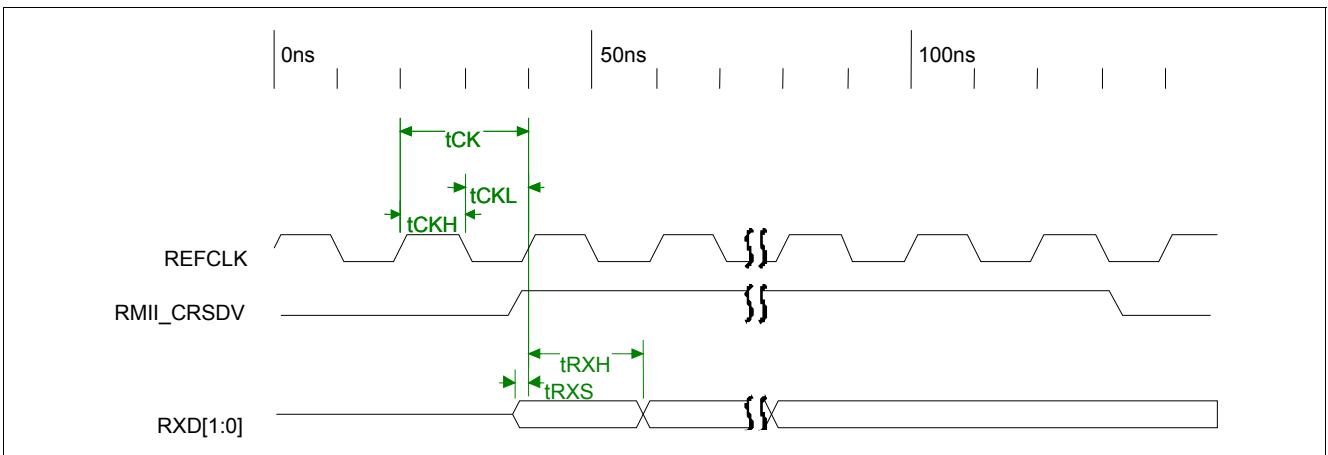


**Figure 27** Reduce MII Timing (2 of 2)

**Table 71** Reduce MII Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| RMII_REFCLK Period | $t_{CK}$ | – | 20 | – | ns | – |
| RMII_REFCLK Low Period | $t_{CKL}$ | – | 10 | – | ns | – |
| RMII_REFCLK High Period | $t_{CKH}$ | – | 10 | – | ns | – |
| TXEN, TXD to REFCLK rising setup time | $t_{TXS}$ | 4 | – | – | ns | – |
| TXE, TXD to REFCLK rising hold time | $t_{TXH}$ | 2 | – | – | ns | – |
| CSRDV, RXD to REFCLK rising setup time | $t_{RXS}$ | 4 | – | – | | – |
| CRSDV, RXD to REFCLK rising hold time | $t_{RXH}$ | 2 | – | – | | – |

## 7.3.11 GPSI (7-wire) Input Timing
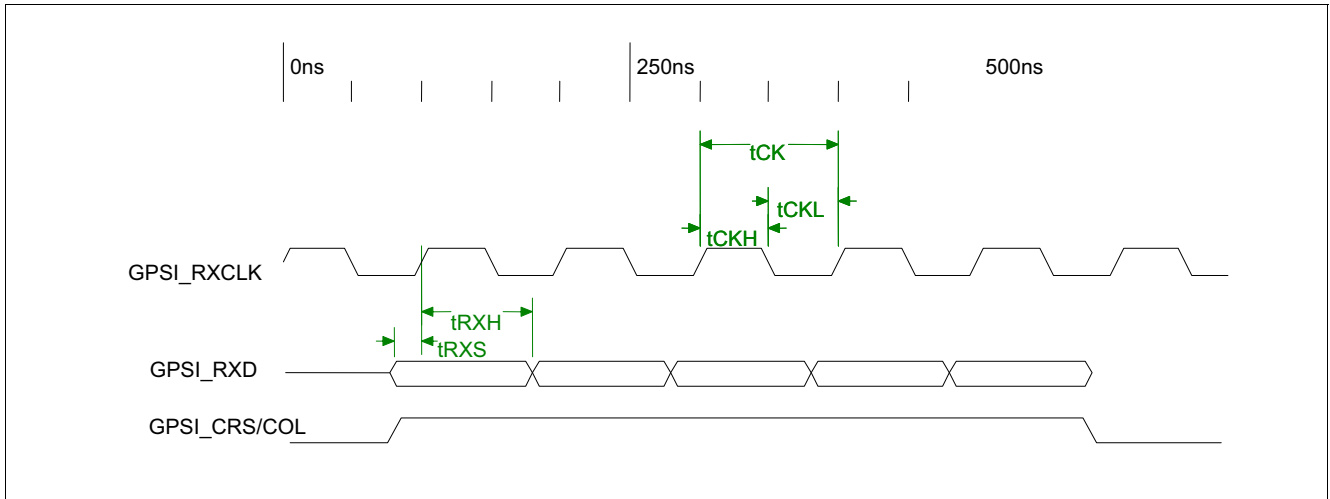


**Figure 28   GPSI (7-wire) Input Timing**

**Table 72   GPSI (7-wire) Input Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| GPSI_RXCLK Period | $t_{CK}$ | – | 100 | – | ns | – |
| GPSI_RXCLK Low Period | $t_{CKL}$ | 40 | – | 60 | ns | – |
| GPSI_RXCLK High Period | $t_{CKH}$ | 40 | – | 60 | ns | – |
| GPSI_RXD, GPSI_CRS/COL to GPSI_RXCLK Rising Setup Time | $t_{RXS}$ | 10 | – | – | ns | – |
| GPSI_RXD, GPSI_CRS/COL to GPSI_RXCLK Rising HoldTime | $t_{RXH}$ | 10 | – | – | ns | – |

## 7.3.12 GPSI (7-wire) Output Timing
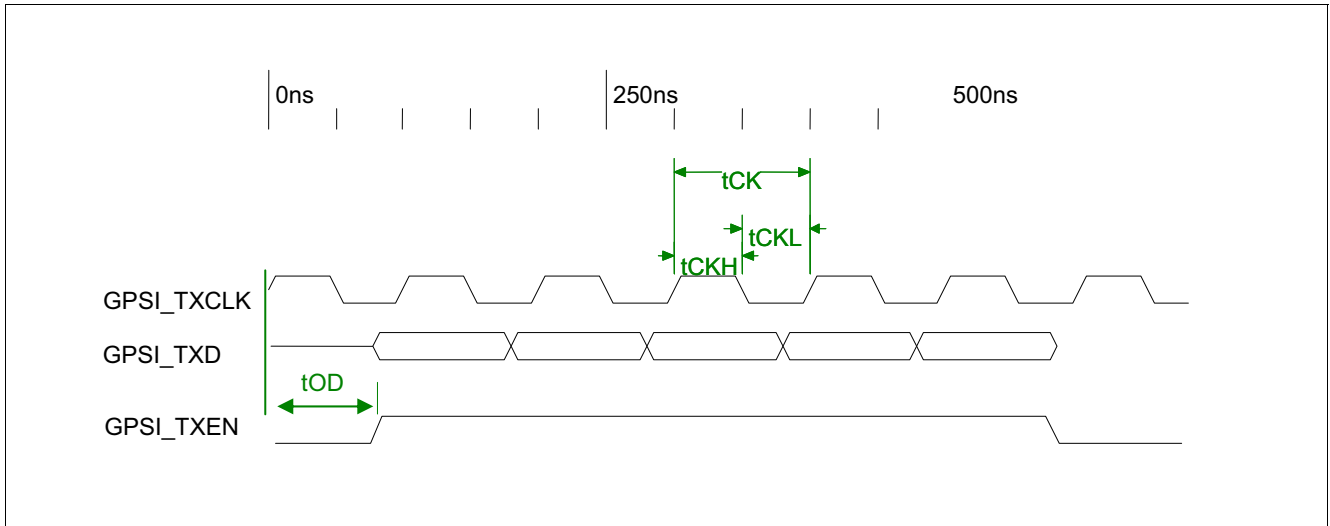


**Figure 29 GPSI (7-wire) Output Timing**

**Table 73 GPSI (7-wire) Output Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| GPSI_TXCLK Period | $t_{CK}$ | – | 100 | – | ns | – |
| GPSI_TXCLK Low Period | $t_{CKL}$ | 40 | – | 60 | ns | – |
| GPSI_TXCLK High Period | $t_{CKH}$ | 40 | – | 60 | ns | – |
| GPSI_TXCLK Rising toGPSI_TXEN/GPSI_TXD Output Delay | $t_{OD}$ | 50 | – | 70 | ns | – |

## 7.3.13 SDC/SDIO Timing
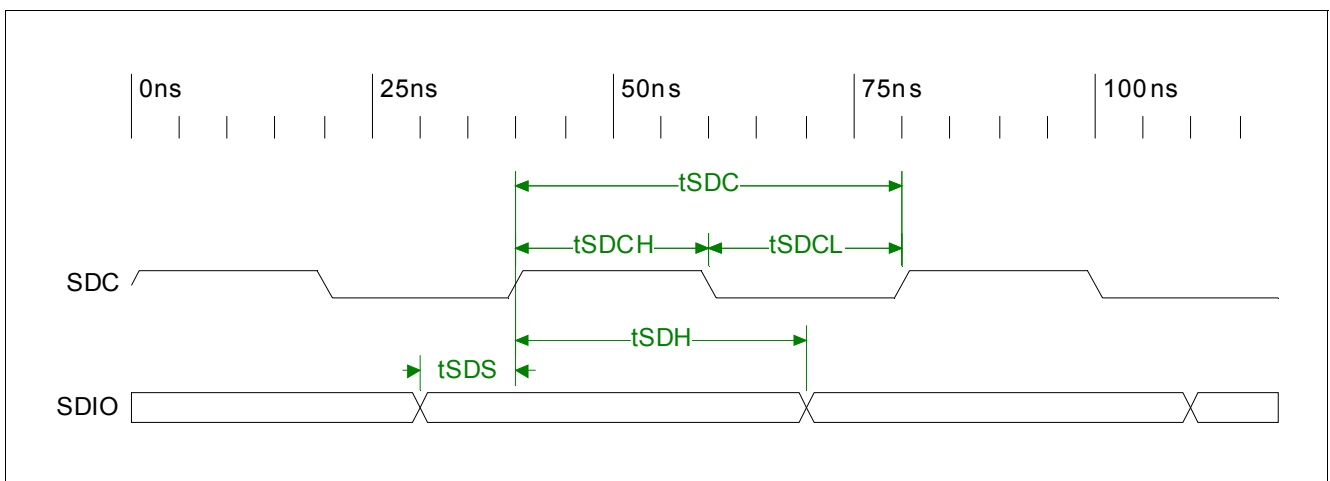


**Figure 30 SDC/SDIO Timing**

**Table 74    SDC/SDIO Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SDC Period | $t_{CK}$ | 20 | – | – | ns | – |
| SDC Low Period | $t_{CKL}$ | 10 | – | – | ns | – |
| SDC High Period | $t_{CKH}$ | 10 | – | – | ns | – |
| SDIO to SDC rising setup time on read/write cycle | $t_{SDS}$ | 4 | – | – | ns | – |
| SDIO to SDC rising hold time on read/write cycle | $t_{SDH}$ | 2 | – | – | ns | – |

# 8 Package Outlines
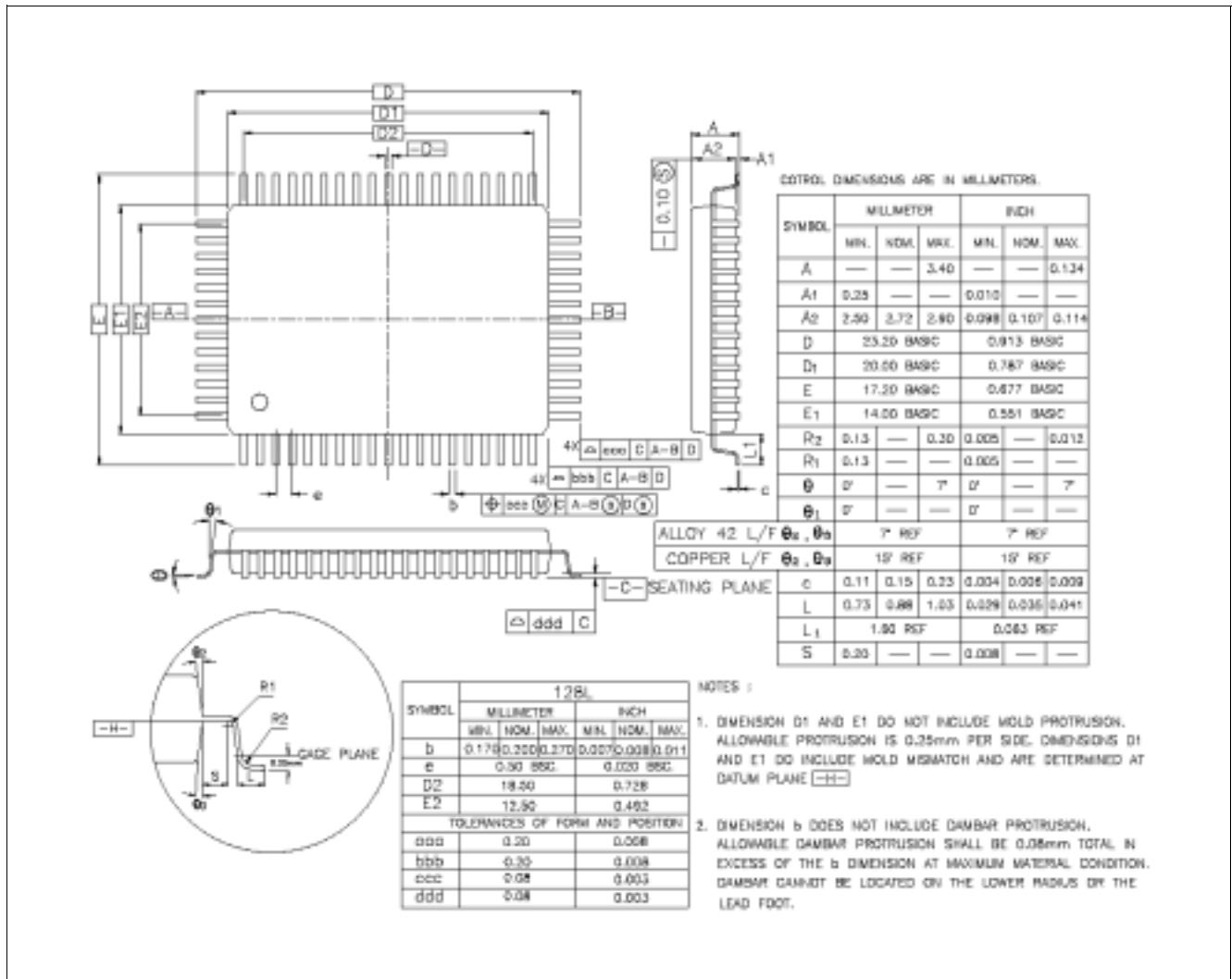


**Figure 31  P-PQFP-128 Outside Dimension**

## 8.1 Package Information

| Product Name | Product Type | Package |
|---|---|---|
| 6-Port 10/100 Mbit/s Single Chip Ethernet Switch Controller | Samurai, ADM6996LC/LCX/LHX-AC-T-1), Version AC | P-PQFP-128 |

# Terminology

**B**

| | |
|---|---|
| BER | Bit Error Rate |

**C**

| | |
|---|---|
| CFI | Canonical Format Indicator |
| COL | Collision |
| CRC | Cyclic Redundancy Check |
| CRS | Carrier Sense |
| CS | Chip Select |

**D**

| | |
|---|---|
| DA | Destination Address |
| DI | Data Input |
| DO | Data Output |

**E**

| | |
|---|---|
| EDI | EEPROM Data Input |
| EDO | EEPROM Data Output |
| EECS | EEPROM Chip Select |
| EESK | EEPROM Clock |
| ESD | End of Stream Delimiter |

**F**

| | |
|---|---|
| FEFI | Far End Fault Indication |
| FET | Field Effect Transistor |
| FLP | Fast Link Pulse |

**G**

| | |
|---|---|
| GND | Ground |
| GPSI | General Purpose Serial Interface |

**I**

| | |
|---|---|
| IPG | Inter-Packet Gap |

**L**

| | |
|---|---|
| LFSR | Linear Feedback Shift Register |

**M**

| | |
|---|---|
| MAC | Media Access Controller |
| MDIX | MDI Crossover |
| MII | Media Independent Interface |

**N**

| | |
|---|---|
| NRZI | Non Return to Zero Inverter |
| NRZ | Non Return to Zero |

**P**

| | |
|---|---|
| PCS | Physical Coding Sub-layer |
| PHY | Physical Layer |
| PLL | Phase Lock Loop |
| PMA | Physical Medium Attachment |

| PMD | Physical Medium Dependent |
|---|---|
| **Q** | |
| QoS | Quality of Service |
| QFP | Quad Flat Package |
| **R** | |
| RST | Reset |
| RXCLK | Receive Clock |
| RXD | Receive Data |
| RXDV | Receive Data Valid |
| RXER | Receive Data Errors |
| RXN | Receive Negative (Analog receive differential signal) |
| RXP | Receive Positive (Analog receive differential signal) |
| **S** | |
| SA | Source Address |
| SOHO | Small Office Home Office |
| SSD | Start of Stream Delimiter |
| SQE | Signal Quality Error |
| **T** | |
| TOS | Type of Service |
| TP | Twisted Pair |
| TTL | Transistor Logic |
| TXCLK | Transmission Clock |
| TXD | Transmission Data |
| TXEN | Transmission Enable |
| TXN | Transmission Negative |
| TXP | Transmission Positive |