

# SN54LS490, SN74LS490 DUAL 4-BIT DECADE COUNTERS

SDLS125A – OCTOBER 1976 – REVISED JULY 1998

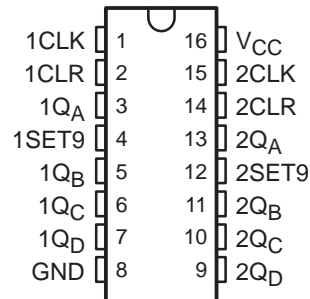
- Dual Versions of the SN54LS90 and SN74LS90 Counters
- Individual Clock, Direct Clear, and Set-to-9 Inputs for Each Decade Counter
- Dual Counters Can Significantly Improve System Densities as Package Count Can Be Reduced by 50%
- Maximum Count Frequency of 25 MHz . . . 35 MHz Typical
- Buffered Outputs Reduce Possibility of Collector Commutation
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

## description

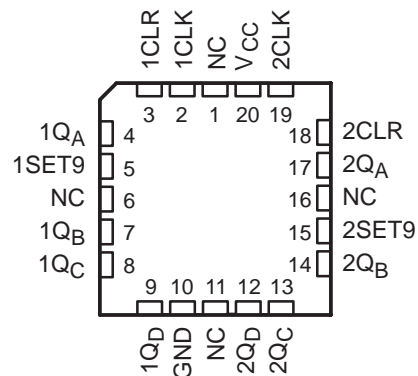
Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual 4-bit decade counters in a single package. Each decade counter has individual clock (1CLK, 2CLK), clear (1CLR, 2CLR), and set-to-9 (1SET9, 2SET9) inputs. BCD count sequences of any length up to divide-by-100 can be implemented with a single 'LS490 device. Buffering on each output is provided to significantly reduce susceptibility to collector commutation. All inputs are diode clamped to reduce the effects of line ringing. The counters have parallel outputs from each counter stage so that submultiples of the input count frequency are available for system timing signals.

The SN54LS490 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS490 is characterized for use in industrial systems operating from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54LS490 . . . J OR W PACKAGE  
SN74LS490 . . . D OR N PACKAGE  
(TOP VIEW)



SN54LS490 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

CLEAR/SET-TO-9 FUNCTION TABLE  
(each counter)

INPUTS		OUTPUTS			
CLR	SET9	QA	QB	QC	QD
H	L	L	L	L	L
L	H	H	L	L	H
L	L	Count			



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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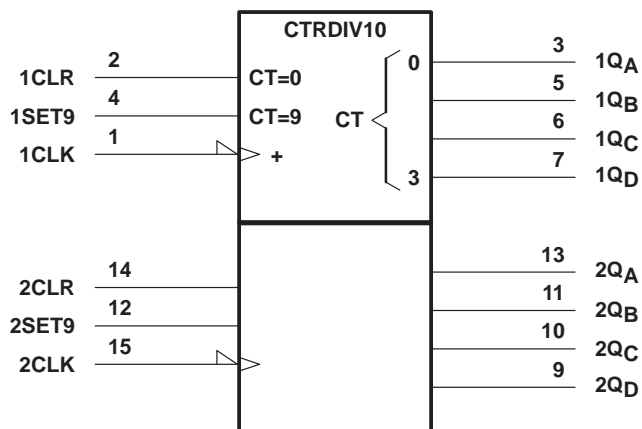
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BCD COUNT SEQUENCE  
(each counter)

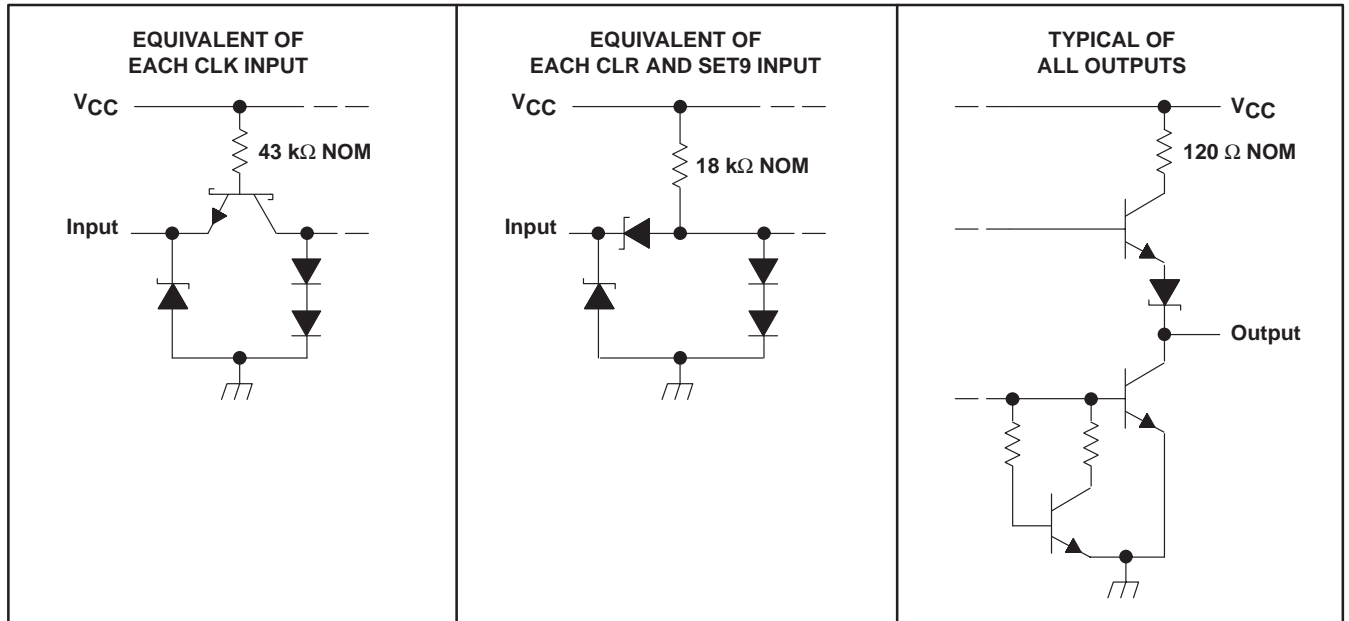
COUNT	OUTPUTS			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, N, and W packages.

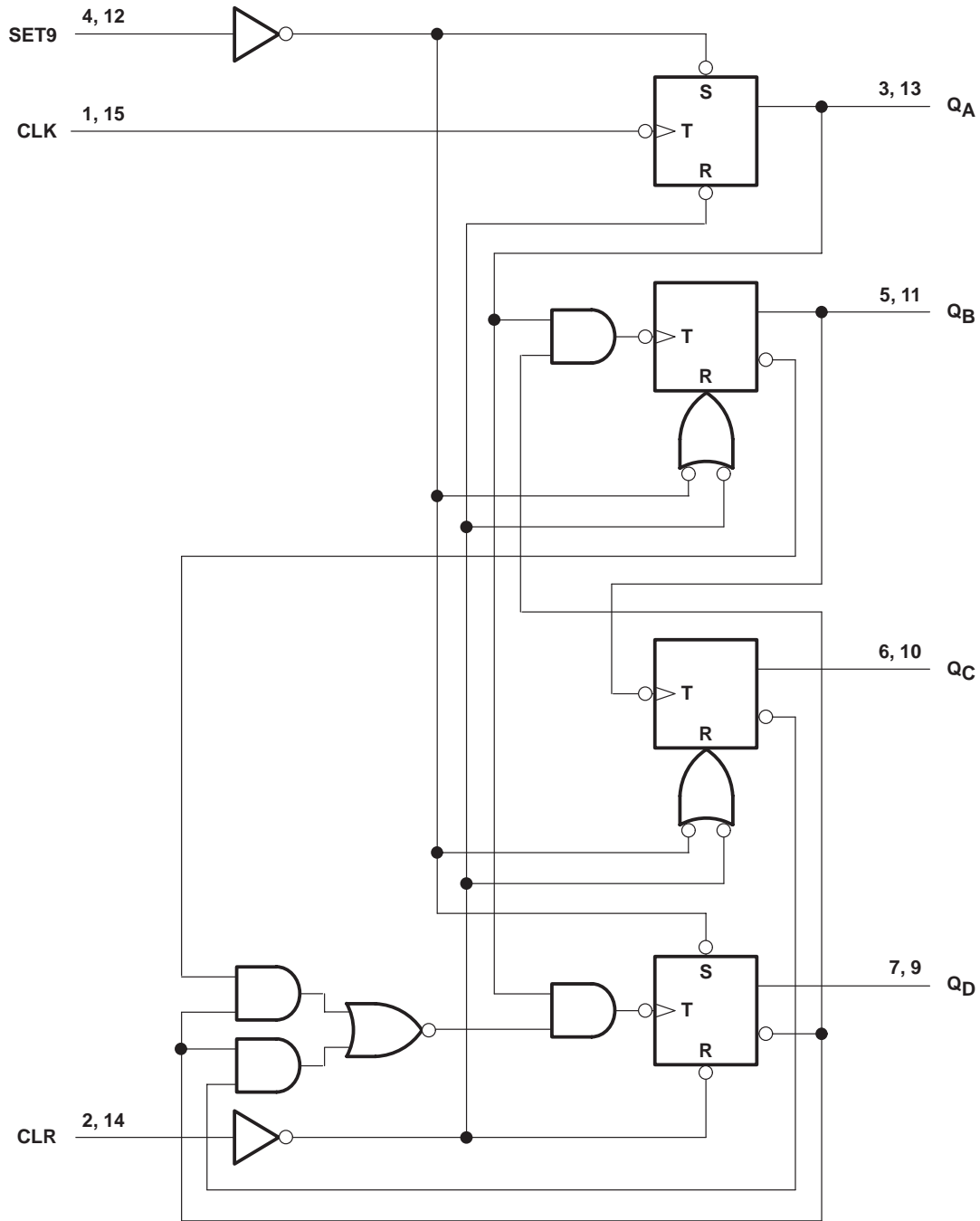
schematics of inputs and outputs



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## logic diagram (each counter)



Pin numbers shown are for the D, J, N, and W packages.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) .....	–0.5 V to 7 V
Clear and set-to-9 voltage .....	–0.5 V to 7 V
Clock input voltage .....	–0.5 V to 5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .....	113°C/W
N package .....	78°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.  
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions

	SN54LS490			SN74LS490			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$I_{OH}$ High-level output current			–400			–400	μA
$I_{OL}$ Low-level output current			4			8	mA
$f_{count}$ Count frequency	0		25	0		25	MHz
$t_w$ Pulse width (any input)	20			20			ns
$t_{su}$ Clear or set-to-9 inactive-state setup time	25↓‡			25↓‡			ns
$T_A$ Operating free-air temperature	–55		125	0		70	°C

‡ The arrow (↓) indicates that the falling edge of the clock pulse is used for reference.



# SN54LS490, SN74LS490 DUAL 4-BIT DECADE COUNTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN74LS490			SN74LS490			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage		0.7			0.8			V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA	-1.5			-1.5			V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>ILmax</sub>	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>ILmax</sub>	I <sub>OL</sub> = 4 mA		0.25	0.4	0.25	0.4	V
			I <sub>OL</sub> = 8 mA				0.35	0.5	
I <sub>I</sub>	Input current at maximum input voltage	CLR, SET9	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.1			0.1	mA
		CLK	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		0.2			0.2	
I <sub>IH</sub>	High-level input current	CLR, SET9	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		20			20	μA
		CLK			100			100	
I <sub>IL</sub>	Low-level input current	CLR, SET9	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-0.4			-0.4	mA
		CLK			-1.6			-1.6	
I <sub>OS</sub> §	Short-circuit output current	V <sub>CC</sub> = MAX	-20	-100	-20	-100			mA
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX, See Note 3	15	26	15	26			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

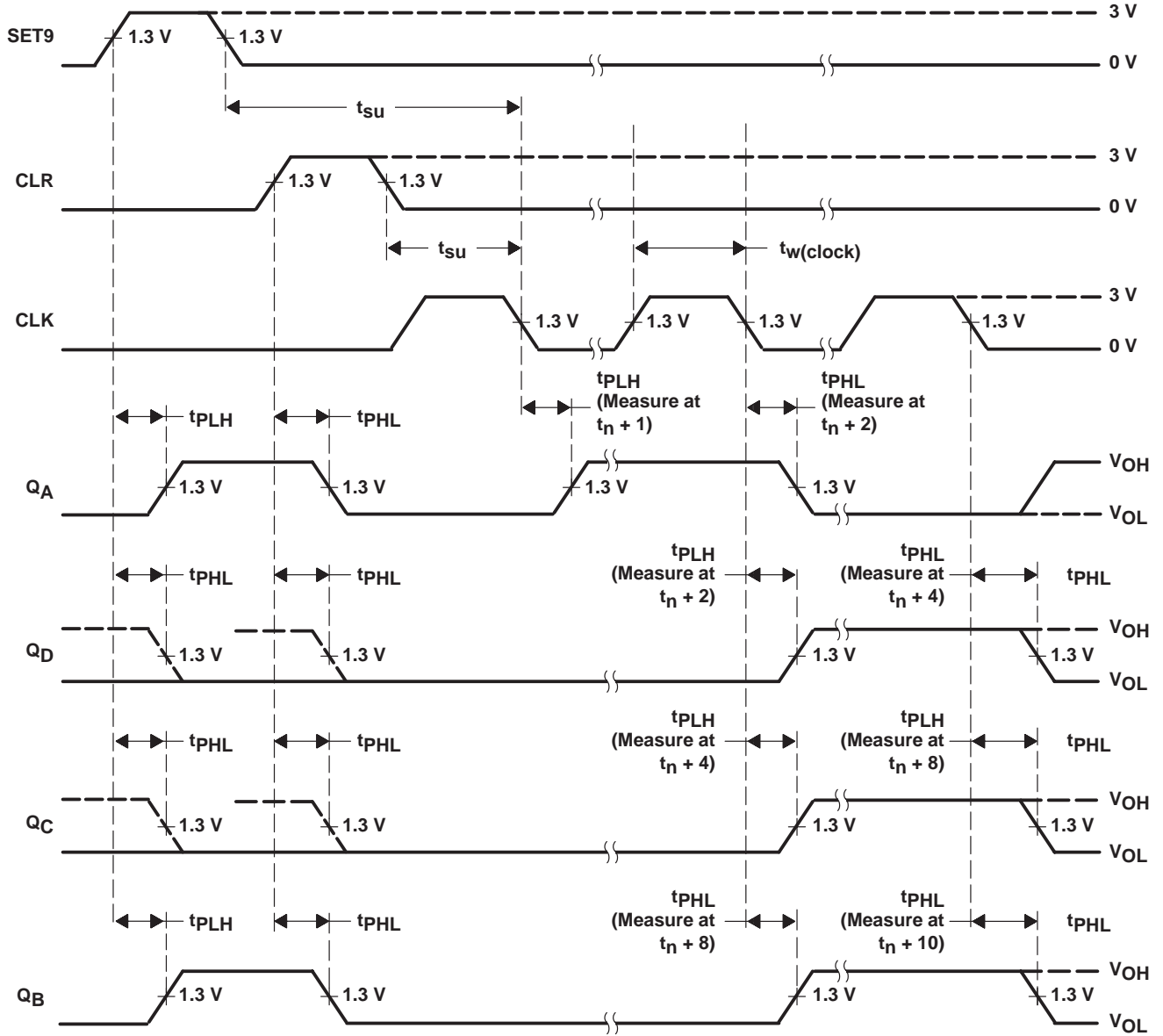
NOTE 3: I<sub>CC</sub> is measured with all outputs open, both CLR inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>	CLK	Q <sub>A</sub>	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ	25	35		MHz
t <sub>PLH</sub>	CLK	Q <sub>A</sub>	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ	12		20	ns
t <sub>PHL</sub>				13		20	
t <sub>PLH</sub>	CLK	Q <sub>B</sub> , Q <sub>D</sub>	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ	24		39	ns
t <sub>PHL</sub>				26		39	
t <sub>PLH</sub>	CLK	Q <sub>C</sub>	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ	32		54	ns
t <sub>PHL</sub>				36		54	
t <sub>PHL</sub>	CLR	Any	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ	24	39		ns
t <sub>PLH</sub>	SET9	Q <sub>A</sub> , Q <sub>D</sub>	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ	24	39		ns
t <sub>PHL</sub>		Q <sub>B</sub> , Q <sub>C</sub>		20	36		



PARAMETER MEASUREMENT INFORMATION



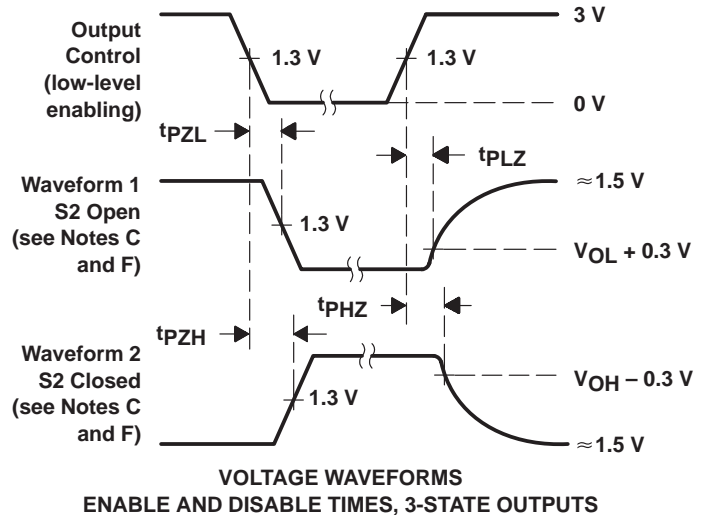
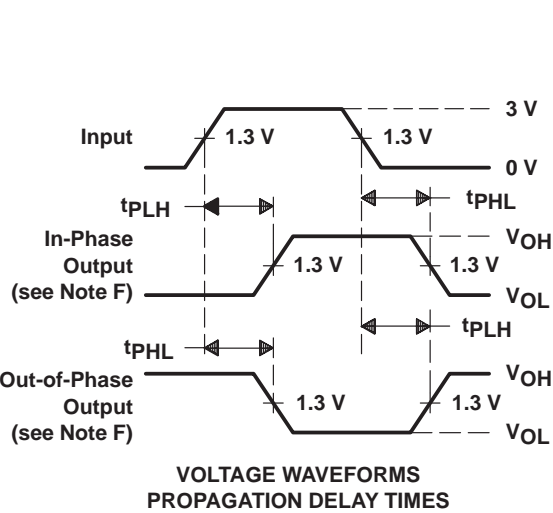
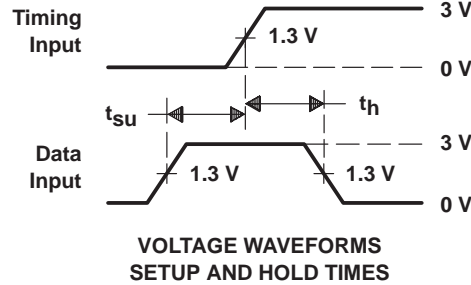
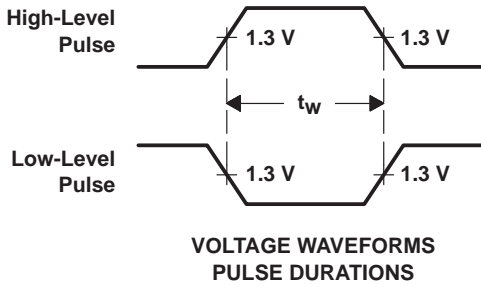
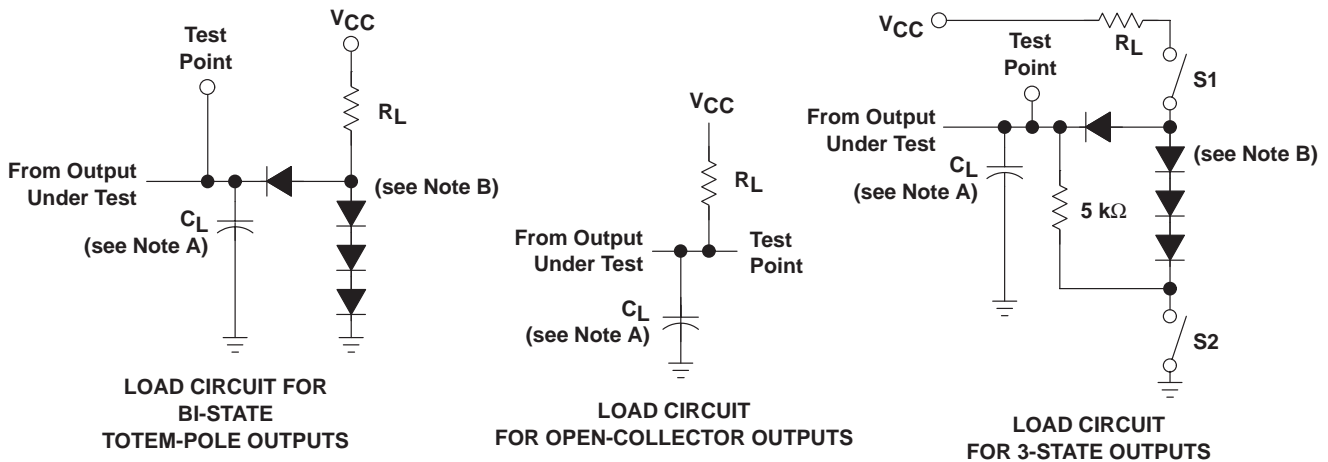
NOTE A: Input pulses are supplied by a generator having the following characteristics:  $t_r \leq 15$  ns,  $t_f \leq 6$  ns, PRR  $\leq 1$  MHz, duty cycle = 50%,  $Z_O \approx 50 \Omega$ .

Figure 1. Voltage Waveforms

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - All diodes are 1N3064 or equivalent.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O \approx 50 \Omega$ ,  $t_r \leq 15$  ns,  $t_f \leq 6$  ns.
  - S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ .
  - The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LS490N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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