

# SN74BCT533 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCBS055A – JULY 1990 – REVISED NOVEMBER 1993

- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$
- Full Parallel Access for Loading
- 3-State Inverting Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V Per MIL-Std-883C, Method 3015
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (N)

## description

The SN74BCT533 is an 8-bit transparent D-type latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

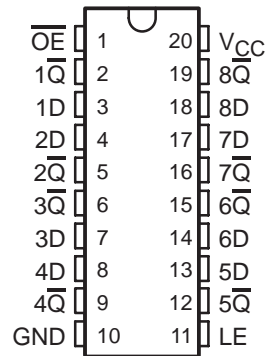
When the latch-enable (LE) input is high, the  $\bar{Q}$  outputs follow the complements of the data (D) inputs. When LE is taken low, the  $\bar{Q}$  outputs are latched at the inverse of the levels set up at the D inputs. The SN74BCT533 provides inverted data at its outputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ( $\overline{OE}$ ) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT533 is characterized for operation from 0°C to 70°C.

DW OR N PACKAGE  
(TOP VIEW)



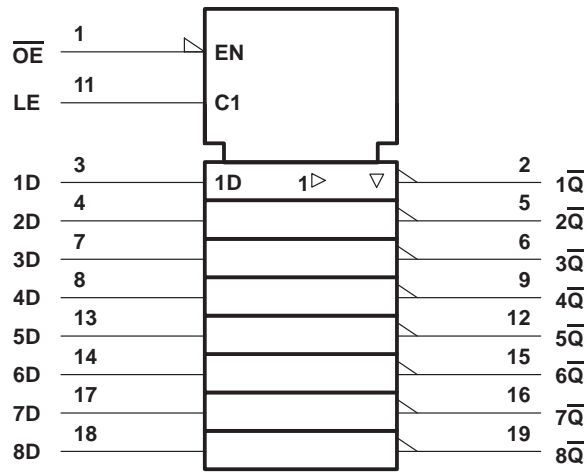
FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	$\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

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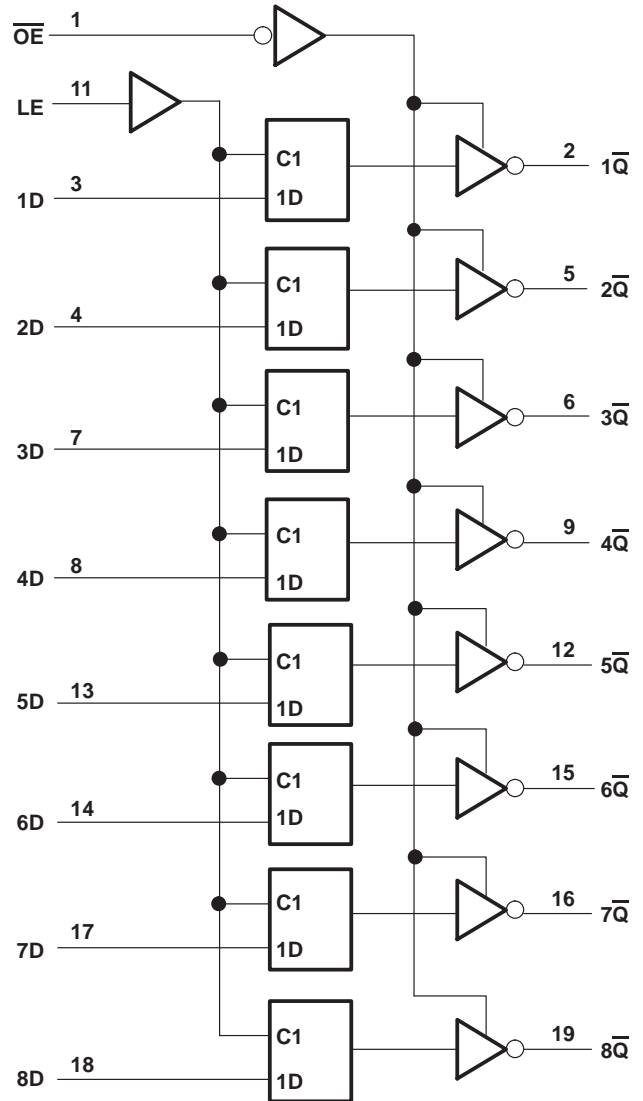
SCBS055A – JULY 1990 – REVISED NOVEMBER 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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SCBS055A – JULY 1990 – REVISED NOVEMBER 1993

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	– 0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	– 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ .....	– 0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ .....	– 0.5 V to $V_{CC}$
Input clamp current .....	–30 mA
Current into any output in the low state .....	128 mA
Operating free-air temperature range .....	0°C to 70°C
Storage temperature range .....	– 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			–18	mA
$I_{OH}$	High-level output current			–15	mA
$I_{OL}$	Low-level output current			64	mA
$T_A$	Operating free-air temperature	0		70	°C



# SN74BCT533

## OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCBS055A – JULY 1990 – REVISED NOVEMBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.3		V
		$I_{OH} = -15\text{ mA}$	2	3.1		
	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -3\text{ mA}$	2.7			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ ,	$I_{OL} = 64\text{ mA}$		0.42	0.55	V
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 5.5\text{ V}$			0.4	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.5\text{ V}$			-0.6	mA
$I_{OS}^\ddagger$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$	-100		-225	mA
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$			50	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.5\text{ V}$			-50	$\mu\text{A}$
$I_{CCL}$	$V_{CC} = 5.5\text{ V}$			40	63	mA
$I_{CCH}$	$V_{CC} = 5.5\text{ V}$			5	8	mA
$I_{CCZ}$	$V_{CC} = 5.5\text{ V}$			5	8	mA
$C_i$	$V_{CC} = 5\text{ V}$ ,	$V_I = 2.5\text{ V}$ or $0.5\text{ V}$		6		pF
$C_o$	$V_{CC} = 5\text{ V}$ ,	$V_O = 2.5\text{ V}$ or $0.5\text{ V}$		11		pF

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
$t_w$	Pulse duration, LE high	4		4		ns
$t_{su}$	Setup time, data before LE↓		High or low	2.5		ns
$t_h$	Hold time, data after LE↓		High or low	3		ns



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**WITH 3-STATE OUTPUTS**

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**switching characteristics (see Note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V},$ $C_L = 50\text{ pF},$ $R_1 = 500\ \Omega,$ $R_2 = 500\ \Omega,$ $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5\text{ V to }5.5\text{ V},$ $C_L = 50\text{ pF},$ $R_1 = 500\ \Omega,$ $R_2 = 500\ \Omega,$ $T_A = \text{MIN to MAX}^\dagger$		UNIT
			MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$	D	$\bar{Q}$	2.8	6.1	9.1	2.8	11.2	ns
$t_{PHL}$			2.7	5.3	8.2	2.7	9.3	
$t_{PLH}$	LE	$\bar{Q}$	2.3	5	7.7	2.3	8.6	ns
$t_{PHL}$			2.5	4.9	7.6	2.5	8.1	
$t_{PZH}$	$\overline{OE}$	$\bar{Q}$	3.1	6.1	8.8	3.1	10.8	ns
$t_{PZL}$			3.7	6.9	10	3.7	12	
$t_{PHZ}$	$\overline{OE}$	$\bar{Q}$	1.8	3.9	5.9	1.8	6.9	ns
$t_{PLZ}$			1.3	3.5	6.1	1.3	7.2	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74BCT533DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74BCT533DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74BCT533N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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