Section 15. Electrical Specifications

15.1 Absolute Maximum Ratings

Table 15-1 lists the absolute maximum ratings.

Table 15-1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.3 to +7.0	V
Programming voltage	V_{PP}	–0.3 to +13.5	V
Input voltage	V_{in}	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note: The input pins have protection circuits that guard against high static voltages and electric fields, but these high input-impedance circuits should never receive overvoltages exceeding the absolute maximum ratings shown in table 15-1.

15.2 Electrical Characteristics

15.2.1 DC Characteristics

Tables 15-2 and 15-3 list the DC characteristics of the H8/325 series.

Table 15-2. DC Characteristics (5V Version)

Conditions: V_{CC} = 5.0V ±10%, V_{SS} = 0V, Ta = –20 to 75°C (regular specifications)
Ta = –40 to 85°C (wide-range specifications)

Item		Symbol	min	typ	max	Unit	Measurement conditions
Schmitt trigger input voltage (1)	P66 to P63, P60, P70	V_T^-	1.0	–	–	V	
		V_T^+	–	–	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	0.4	–	–	V	
Input high voltage (2)	$\overline{RES}$, $\overline{STBY}$ MD1, MD0 EXTAL, $\overline{NMI}$	V_{IH}	$V_{CC} - 0.7$	–	$V_{CC} + 0.3$	V	
Input high voltage	Input pins other than (1) and (2)	V_{IH}	2.0	–	$V_{CC} + 0.3$	V	
Input low voltage (3)	$\overline{RES}$, $\overline{STBY}$ MD1, MD0, EXTAL	V_{IL}	–0.3	–	0.5	V	
Input low voltage	Input pins other than (1) and (3)	V_{IL}	–0.3	–	0.8	V	
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	–	–	V	I_{OH} = –200 µA
			3.5	–	–	V	I_{OH} = –1.0 mA
Output low voltage	All output pins	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
	P17 to P10, P27 to P20		–	–	1.0	V	I_{OL} = 10.0 mA
Input leakage current	$\overline{RES}$	$\|I_{in}\|$	–	–	10.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
	$\overline{STBY}$, $\overline{NMI}$, MD1, MD0		–	–	1.0	µA	
Leakage current in 3-state (off state)	Ports 1 to 7	$\|I_{TSI}\|$	–	–	1.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
Input pull-up MOS current	Ports 1 to 7	-Ip	30	–	250	µA	V_{in} = 0 V

Table 15-2. DC Characteristics (5V Version) (cont.)

Conditions: V_{CC} = AV_{CC} = 5.0V ±10%, V_{SS} = 0V, Ta = –20 to 75°C (regular specifications)
Ta = –40 to 85°C (wide-range specifications)

Item		Symbol	min	typ	max	Unit	Measurement conditions
Input capacitance	$\overline{RES}$	C_{in}	–	–	60	pF	V_{in} = 0 V
	$\overline{NMI}$		–	–	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and $\overline{NMI}$		–	–	15	pF	Ta = 25°C
Current dissipation*1	Normal operation	I_{CC}	–	12	25	mA	f = 6 MHz
			–	16	30	mA	f = 8 MHz
			–	20	40	mA	f = 10 MHz
	Sleep mode		–	8	15	mA	f = 6 MHz
			–	10	20	mA	f = 8 MHz
			–	12	25	mA	f = 10 MHz
	Standby modes*2		–	0.01	5.0	μA	
RAM standby voltage		V_{RAM}	2.0	–	–	V	

Notes: 1. Current dissipation values assume that $V_{IH\ min.}$ = V_{CC} – 0.5V, $V_{IL\ max.}$ = 0.5V, all output pins are in the no-load state, and all MOS input pull-ups are off.

2. For these values it is assumed that $V_{RAM} \leq V_{CC} < 4.5$ V and V_{IH} min = $V_{CC} \times 0.9$, V_{IL} max = 0.3 V.

Table 15-3. DC Characteristics (3V Version for only H8/3257 and H8/3256)

Conditions: V_{CC} = 2.7 to 3.6V, V_{SS} = 0V, Ta = –20 to 75°C

Item		Symbol	min	typ	max	Unit	Measurement conditions
Schmitt trigger input voltage (1)	P66 to P63, P60, P70	V_T^-	$V_{CC} \times 0.15$	–	–	V	
		V_T^+	–	–	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	0.2	–	–	V	
Input high voltage (2)	$\overline{RES}$, $\overline{STBY}$ MD1, MD0 EXTAL, $\overline{NMI}$	V_{IH}	$V_{CC} \times 0.9$	–	$V_{CC} + 0.3$	V	
Input high voltage	Input pins other than (1) and (2)	V_{IH}	$V_{CC} \times 0.7$	–	$V_{CC} + 0.3$	V	
Input low voltage (3)	$\overline{RES}$, $\overline{STBY}$ MD1, MD0, EXTAL	V_{IL}	–0.3	–	$V_{CC} \times 0.1$	V	
Input low voltage	Input pins other than (1) and (3)	V_{IL}	–0.3	–	$V_{CC} \times 0.15$	V	
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.4$	–	–	V	I_{OH} = –200 µA
			$V_{CC} - 0.9$	–	–	V	I_{OH} = –1.0 mA
Output low voltage	P17 to P10, P27 to P20	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
	All output pins		–	–	0.4	V	I_{OL} = 0.8 mA
Input leakage current	$\overline{RES}$	$\|I_{in}\|$	–	–	10.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
	$\overline{STBY}$, $\overline{NMI}$, MD1, MD0		–	–	1.0	µA	
Leakage current in 3-state (off state)	Ports 1 to 7	$\|I_{TSI}\|$	–	–	1.0	µA	V_{in} = 0.5 V to V_{CC} – 0.5 V
Input pull-up MOS current	Ports 1 to 7	-Ip	3	–	120	µA	V_{CC} = 3.3 V V_{in} = 0 V

Table 15-3. DC Characteristics (3V Version for only H8/3257 and H8/3256) (cont.)

Conditions: V_{CC} = 2.7 to 3.6V, V_{SS} = 0V, Ta = –20 to 75°C

Item		Symbol	min	typ	max	Unit	Measurement conditions
Input capacitance	$\overline{RES}$	C_{in}	–	–	60	pF	V_{in} = 0 V
	$\overline{NMI}$		–	–	30	pF	f = 1 MHz
	All input pins except $\overline{RES}$ and $\overline{NMI}$		–	–	15	pF	Ta = 25°C
Current dissipation*	Normal operation	I_{CC}	–	4	–	mA	f = 3 MHz
	Sleep mode		–	3	–	mA	
	Normal operation		–	6	12	mA	f = 5 MHz
	Sleep mode		–	4	8	mA	
	Standby modes		–	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	–	–	V	

Note: Current dissipation values assume that $V_{IH\ min.} = V_{CC} - 0.5V$, $V_{IL\ max.} = 0.5V$, all output pins are in the no-load state, and all MOS input pull-ups are off.

Table 15-4. Allowable Output Current Sink Values

Conditions: V_{CC} = 5.0V ±10%, V_{SS} = 0V, Ta = –20 to 75°C (regular specifications)
Ta = –40 to 85°C (wide-range specifications)

Item		Symbol	min	typ	max	Unit
Allowable output low current sink (per pin)	Ports 1 and 2	I_{OL}	–	–	10	mA
	Other output pins		–	–	2.0	mA
Allowable output low current sink (total)	Ports 1 and 2, total	ΣI_{OL}	–	–	80	mA
	All output pins		–	–	120	mA
Allowable output high current sink (per pin)	All output pins	$-I_{OH}$	–	–	2.0	mA
Allowable output high current sink (total)	Total of all output	$\Sigma-I_{OH}$	–	–	40	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 15-4. In particular, when driving a Darlington pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 17-1 and 17-2.

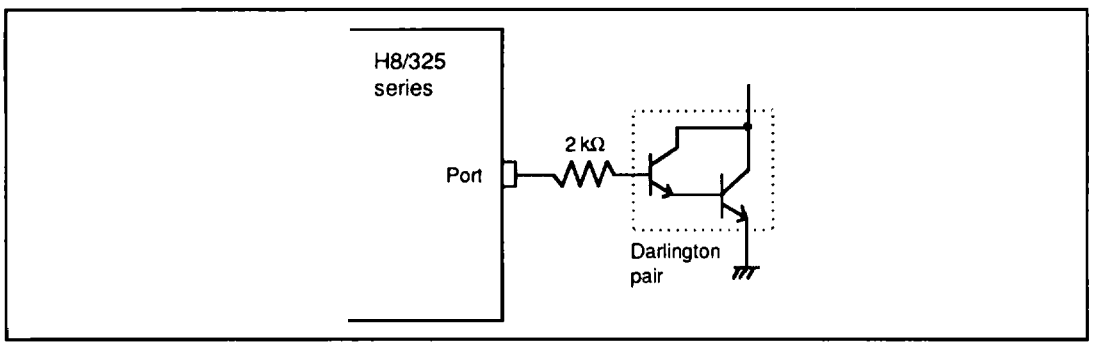

Figure 15-1. Example of Circuit for Driving a Darlington Pair

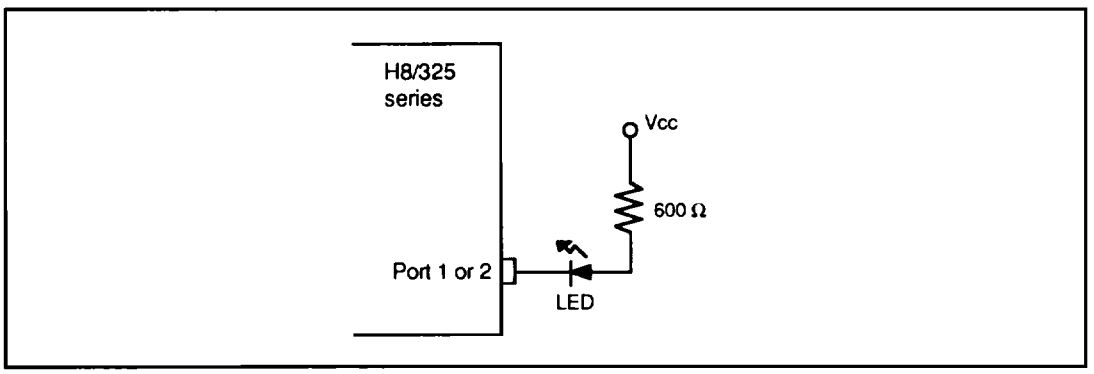

Figure 15-2. Example of Circuit for Driving a LED

Table 15-5. Allowable Output Current Sink Values (3V Version for only H8/3257 and H8/3256)
Conditions: V_{CC} = 2.7 to 3.6V, V_{SS} = 0V, Ta = –20 to 75°C

Item		Symbol	min	typ	max	Unit
Allowable output low current sink (per pin)	Ports 1 and 2	I_{OL}	–	–	2	mA
	Other output pins		–	–	1.0	mA
Allowable output low current sink (total)	Ports 1 and 2, total of 16 pins	ΣI_{OL}	–	–	40	mA
	Total of all other output pins		–	–	60	mA
Allowable output high current sink (per pin)	All output pins	$-I_{OH}$	–	–	2.0	mA
Allowable output high current sink (total)	Total of all output pins	$\Sigma-I_{OH}$	–	–	30	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 15-5.

15.2.2 AC Characteristics

The AC characteristics of the H8/325 series are listed in three tables. Bus timing parameters are given in table 15-6, control signal timing parameters in table 15-7, and timing parameters of the on-chip supporting modules in table 15-8.

Table 15-6. Bus Timing

Condition A: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10MHz, V_{SS} = 0V,
Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)
Condition B: V_{CC} = 2.7 to 3.6V, V_{SS} = 0V, Ta = –20 to 75°C, for only H8/3257 and H8/3256

		Condition B		Condition A							
		5MHz		6MHz		8MHz		10MHz			Measurement
Item	Symbol	min	max	min	max	min	max	min	max	Unit	conditions
Clock cycle time	t_{cyc}	200	2000	166.7	2000	125	2000	100	2000	ns	Fig. 15-4
Clock pulse width Low	t_{CL}	65	–	65	–	45	–	35	–	ns	Fig. 15-4
Clock pulse width High	t_{CH}	65	–	65	–	45	–	35	–	1ns	Fig. 15-4
Clock rise time	t_{Cr}	–	25	–	15	–	15	–	15	ns	Fig. 15-4
Clock fall time	t_{Cf}	–	25	–	15	–	15	–	15	ns	Fig. 15-4
Address delay time	t_{AD}	–	90	–	70	–	60	–	55	ns	Fig. 15-4
Address hold time	t_{AH}	30	–	30	–	25	–	20	–	ns	Fig. 15-4
Address strobe delay time	t_{ASD}	–	80	–	70	–	60	–	40	ns	Fig. 15-4
Write strobe delay time	t_{WSD}	–	80	–	70	–	60	–	50	ns	Fig. 15-4
Strobe delay time	t_{SD}	–	90	–	70	–	60	–	50	ns	Fig. 15-4
Write strobe pulse width	t_{WSW}	200	–	200	–	150	–	120	–	ns	Fig. 15-4
Address setup time 1	t_{AS1}	25	–	25	–	20	–	15	–	ns	Fig. 15-4
Address setup time 2	t_{AS2}	105	–	105	–	80	–	65	–	ns	Fig. 15-4
Read data setup time	t_{RDS}	90	–	60	–	50	–	35	–	ns	Fig. 15-4
Read data hold time	t_{RDH}	0	–	0	–	0	–	0	–	ns	Fig. 15-4
Write data delay time	t_{WDD}	–	125	–	85	–	75	–	75	ns	Fig. 15-4
Read data access time	t_{ACC}	–	300	–	280	–	210	–	170	ns	Fig. 15-4
Write data setup time	t_{WDS}	10	–	30	–	15	–	10	–	ns	Fig. 15-4
Write data hold time	t_{WDH}	30	–	30	–	25	–	20	–	ns	Fig. 15-4
Wait setup time	t_{WTS}	60	–	45	–	45	–	45	–	ns	Fig. 15-5
Wait hold time	t_{WTH}	20	–	10	–	10	–	10	–	ns	Fig. 15-5
E clock delay time	t_{ED}	–	30	–	25	–	25	–	25	ns	Fig. 15-6
E clock rise time	t_{Er}	–	25	–	15	–	15	–	15	ns	Fig. 15-6
E clock fall time	t_{Ef}	–	25	–	15	–	15	–	15	ns	Fig. 15-6
Read data hold time (for E clock)	t_{RDHE}	0	–	0	–	0	–	0	–	ns	Fig. 15-6
Write data hold time (for E clock)	t_{WDHE}	60	–	50	–	40	–	30	–	ns	Fig. 15-6

Table 15-7. Control Signal Timing

Condition A: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10MHz, V_{SS} = 0V,
Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Condition B: V_{CC} = 2.7 to 3.6V, V_{SS} = 0V, Ta = –20 to 75°C, for only H8/3257 and H8/3256

		Condition B		Condition A							
		5MHz		6MHz		8MHz		10MHz			Measurement
Item	Symbol	min	max	min	max	min	max	min	max	Unit	conditions
$\overline{RES}$ setup time	t_{RESS}	300	–	200	–	200	–	200	–	ns	Fig. 15-7
$\overline{RES}$ pulse width	t_{RESW}	10	–	10	–	10	–	10	–	t_{cyc}	Fig. 15-7
Mode programming setup time	t_{MDS}	4	–	4	–	4	–	4	–	t_{cyc}	Fig. 15-7
$\overline{NMI}$ setup time ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_2}$)	t_{NMIS}	300	–	150	–	150	–	150	–	ns	Fig. 15-8
$\overline{NMI}$ hold time ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_2}$)	t_{NMIH}	10	–	10	–	10	–	10	–	ns	Fig. 15-8
Interrupt pulse width for recovery from software standby mode ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_2}$)	t_{NMIW}	300	–	200	–	200	–	200	–	ns	Fig. 15-8
Crystal oscillator settling time (reset)	t_{OSC1}	20	–	20	–	20	–	20	–	ms	Fig. 15-9
Crystal oscillator settling time (software standby)	t_{OSC2}	10	–	10	–	10	–	10	–	ms	Fig. 15-10

Table 15-8. Timing Conditions of On-Chip Supporting Modules

Condition A: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10MHz, V_{SS} = 0V,
Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Condition B: V_{CC} = 2.7 to 3.6V, V_{SS} = 0V, Ta = –20 to 75°C, for only H8/3257 and H8/3256

			Condition B		Condition A							
			5MHz		6MHz		8MHz		10MHz			Measurement
Item		Symbol	min	max	min	max	min	max	min	max	Unit	conditions
FRT	Timer output delay time	t_{FTOD}	–	150	–	100	–	100	–	100	ns	Fig. 15-11
	Timer input setup time	t_{FTIS}	80	–	50	–	50	–	50	–	ns	Fig. 15-11
	Timer clock input setup time	t_{FTCS}	80	–	50	–	50	–	50	–	ns	Fig. 15-12
	Timer clock pulse width	t_{FTCWH} t_{FTCWL}	1.5	–	1.5	–	1.5	–	1.5	–	t_{cyc}	Fig. 15-12

Table 15-8. Timing Conditions of On-Chip Supporting Modules (cont.)

Condition A: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10MHz, V_{SS} = 0V,
Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Condition B: V_{CC} = 2.7 to 3.6V, V_{SS} = 0V, Ta = –20 to 75°C, for only H8/3257 and H8/3256

			Condition B		Condition A							
			5MHz		6MHz		8MHz		10MHz			Measurement
Item		Symbol	min	max	min	max	min	max	min	max	Unit	conditions
TMR	Timer output delay time	t_{TMOD}	–	150	–	100	–	100	–	100	ns	Fig. 15-13
	Timer reset input setup time	t_{TMRS}	80	–	50	–	50	–	50	–	ns	Fig. 15-15
	Timer clock input setup time	t_{TMCS}	80	–	50	–	50	–	50	–	ns	Fig. 15-14
	Timer clock pulse width (single edge)	t_{TMCWH}	1.5	–	1.5	–	1.5	–	1.5	–	t_{cyc}	Fig. 15-14
	Timer clock pulse width (both edges)	t_{TMCWL}	2.5	–	2.5	–	2.5	–	2.5	–	t_{cyc}	Fig. 15-14
SCI	Input clock cycle (Async)	t_{Scyc}	2	–	2	–	2	–	2	–	t_{cyc}	Fig. 15-16
	(Sync)	t_{Scyc}	4	–	4	–	4	–	4	–	t_{cyc}	Fig. 15-16
	Transmit data delay time (Sync)	t_{TXD}	–	200	–	100	–	100	–	100	ns	Fig. 15-16
	Receive data setup time (Sync)	t_{RXS}	150	–	100	–	100	–	100	–	ns	Fig. 15-16
	Receive data hold time (Sync)	t_{RXH}	150	–	100	–	100	–	100	–	ns	Fig. 15-16
	Input clock pulse width	t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}	Fig. 15-17
Ports	Output data delay time	t_{PWD}	–	150	–	100	–	100	–	100	ns	Fig. 15-18
	Input data setup time	t_{PRS}	80	–	50	–	50	–	50	–	ns	Fig. 15-18
	Input data hold time	t_{PRH}	80	–	50	–	50	–	50	–	ns	Fig. 15-18

Table 15-8. Timing Conditions of On-Chip Supporting Modules (cont.)

Condition A: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10MHz, V_{SS} = 0V,
Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Condition B: V_{CC} = 2.7 to 3.6V, V_{SS} = 0V, Ta = –20 to 75°C, for only H8/3257 and H8/3256

			Condition B		Condition A							
			5MHz		6MHz		8MHz		10MHz			Measurement
Item		Symbol	min	max	min	max	min	max	min	max	Unit	conditions
Parallel handshake interface	Handshake input strobe pulse width	t_{HSW}	1.5	–	1.5	–	1.5	–	1.5	–	t_{cyc}	Fig. 15-19
	Handshake input data setup time	t_{HS}	10	–	10	–	10	–	10	–	ns	Fig. 15-19
	Handshake input data hold time	t_{HH}	120	–	120	–	120	–	120	–	ns	Fig. 15-19
	Handshake output strobe delay time	t_{HOSD1}	–	100	–	80	–	80	–	80	ns	Fig. 15-20
		t_{HOSD2}	–	100	–	80	–	80	–	80	ns	Fig. 15-20
	Busy output delay time	t_{HBSOD1}	–	150	–	150	–	150	–	150	ns	Fig. 15-21
		t_{HBSOD2}	–	150	–	150	–	150	–	150	ns	Fig. 15-21

- **Measurement Conditions for AC Characteristics**

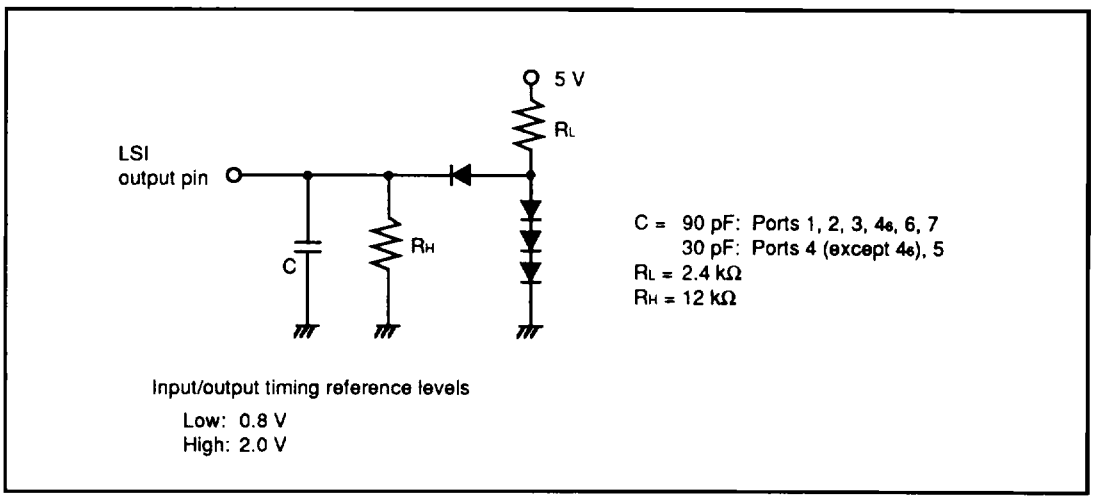

Figure 15-3. Output Load Circuit

15.3 MCU Operational Timing

This section provides the following timing charts:

15.3.1 Bus Timing	Figures 15-4 to 15-6
15.3.2 Control Signal Timing	Figures 15-7 to 15-10
15.3.3 16-Bit Free-Running Timer Timing	Figures 15-11 to 15-12
15.3.4 8-Bit Timer Timing	Figures 15-13 to 15-15
15.3.6 SCI Timing	Figures 15-15 to 15-17
15.3.7 I/O Port Timing	Figure 15-18
15.3.8 Parallel Handshaking Interface Timing	Figures 15-19 to 15-21

15.3.1 Bus Timing

(1) Basic Bus Cycle (without Wait States) in Expanded Modes

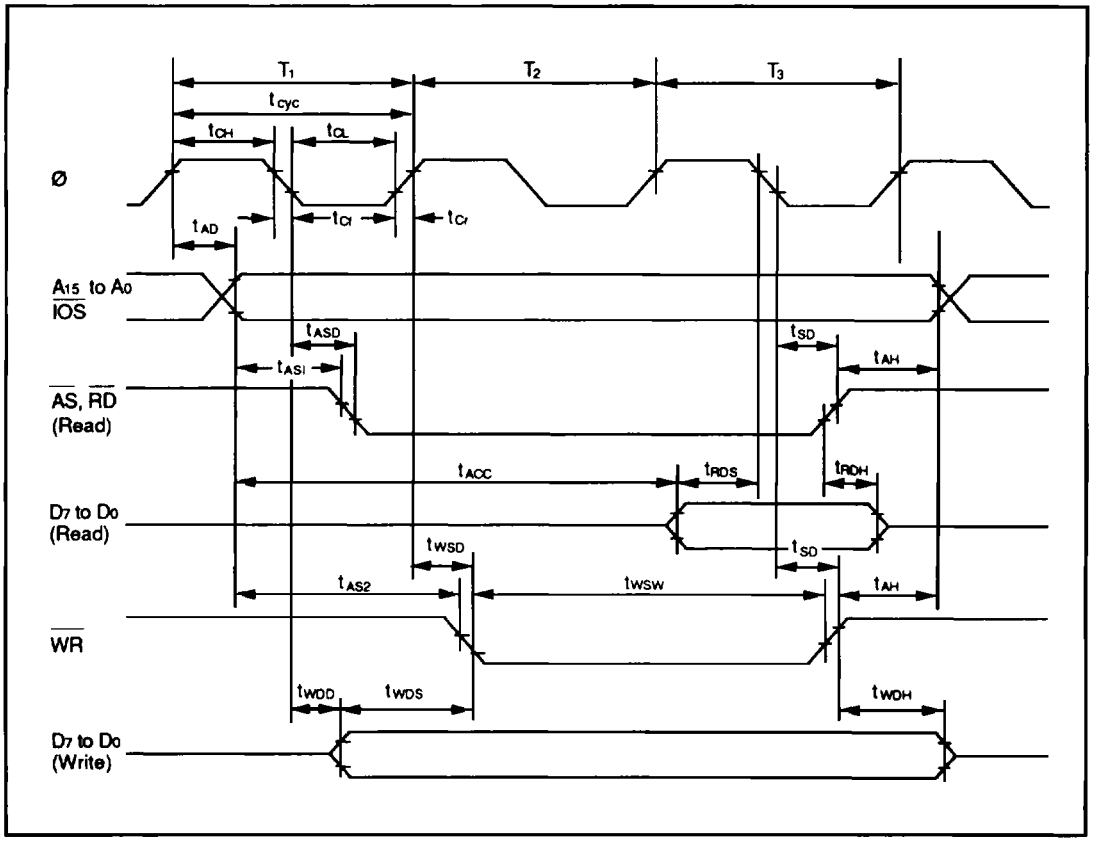

Figure 15-4. Basic Bus Cycle (without Wait States) in Expanded Modes

(2) Basic Bus Cycle (with 1 Wait State) in Expanded Modes

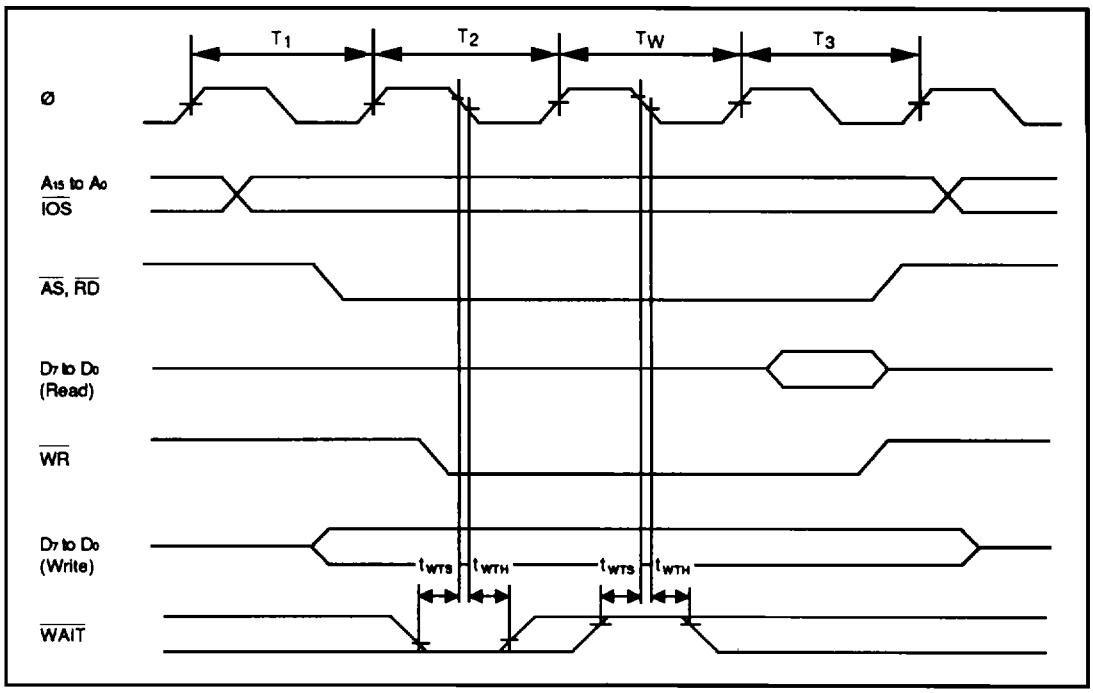

Figure 15-5. Basic Bus Cycle (with 1 Wait State) in Expanded Modes

(3) E Clock Bus Cycle

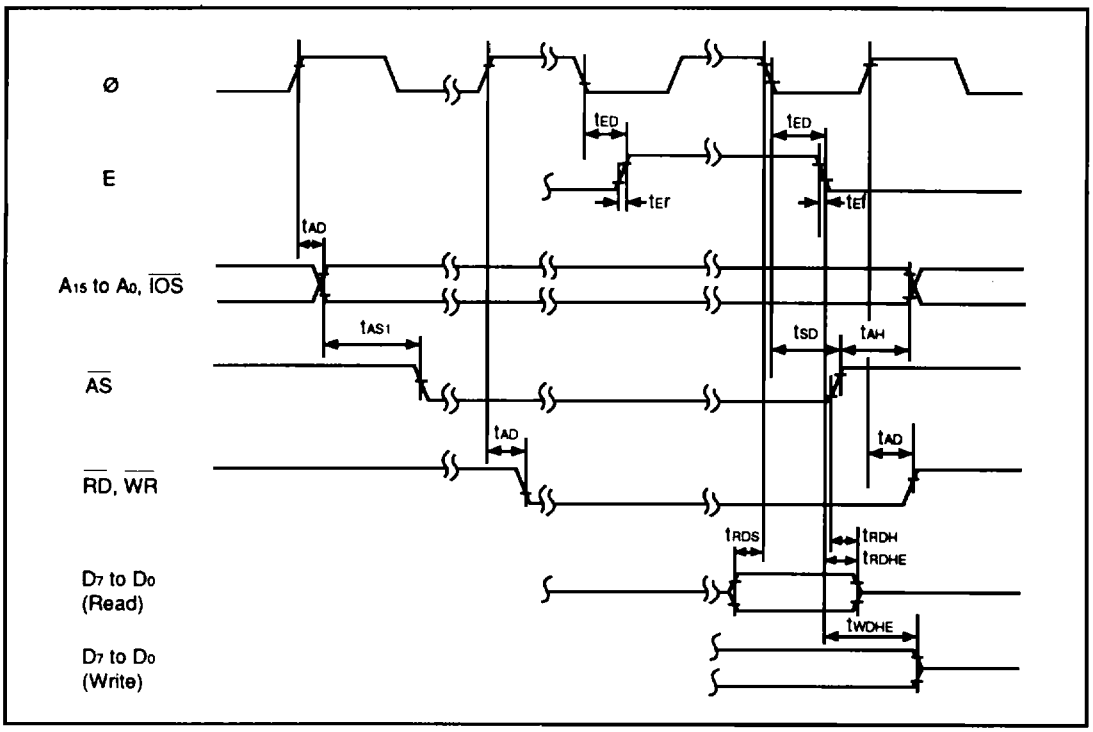

Figure 15-6. E Clock Bus Cycle

15.3.2 Control Signal Timing

(1) Reset Input Timing

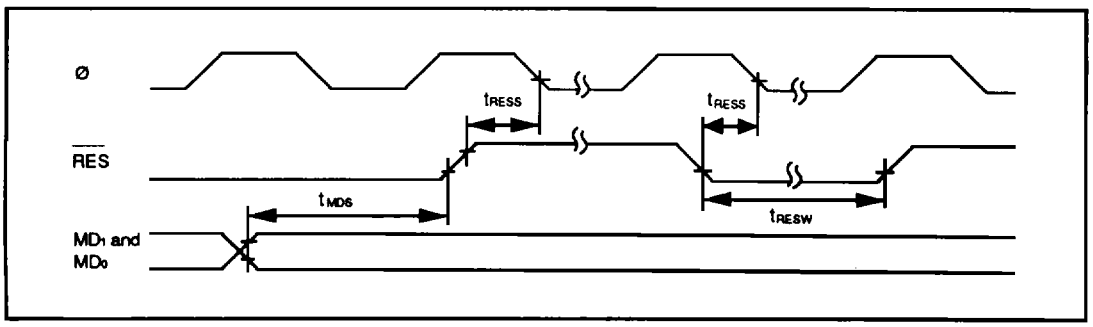

Figure 15-7. Reset Input Timing

(2) Interrupt Input Timing

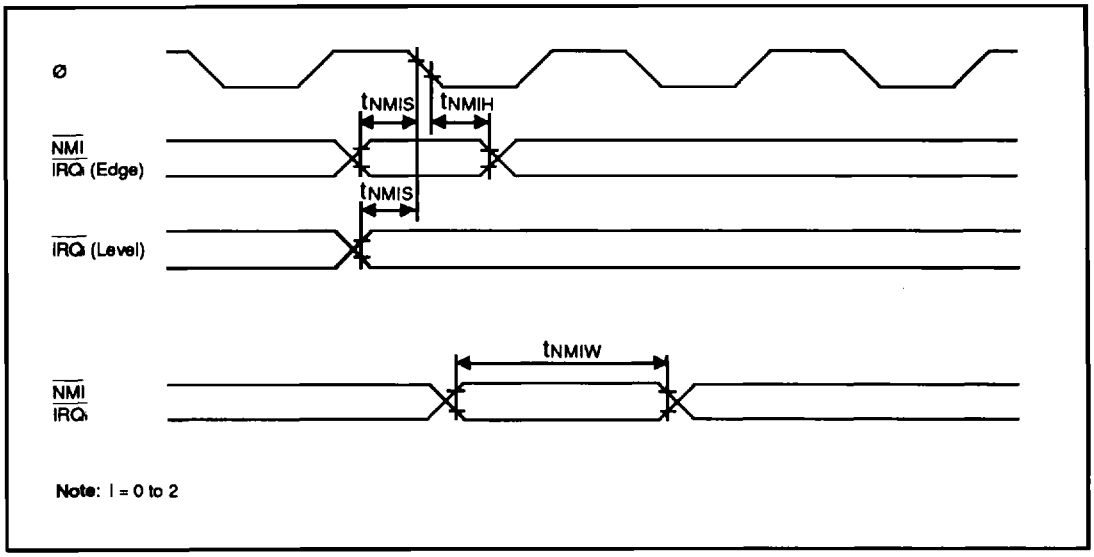

Figure 15-8. Interrupt Input Timing

(3) Clock Settling Timing

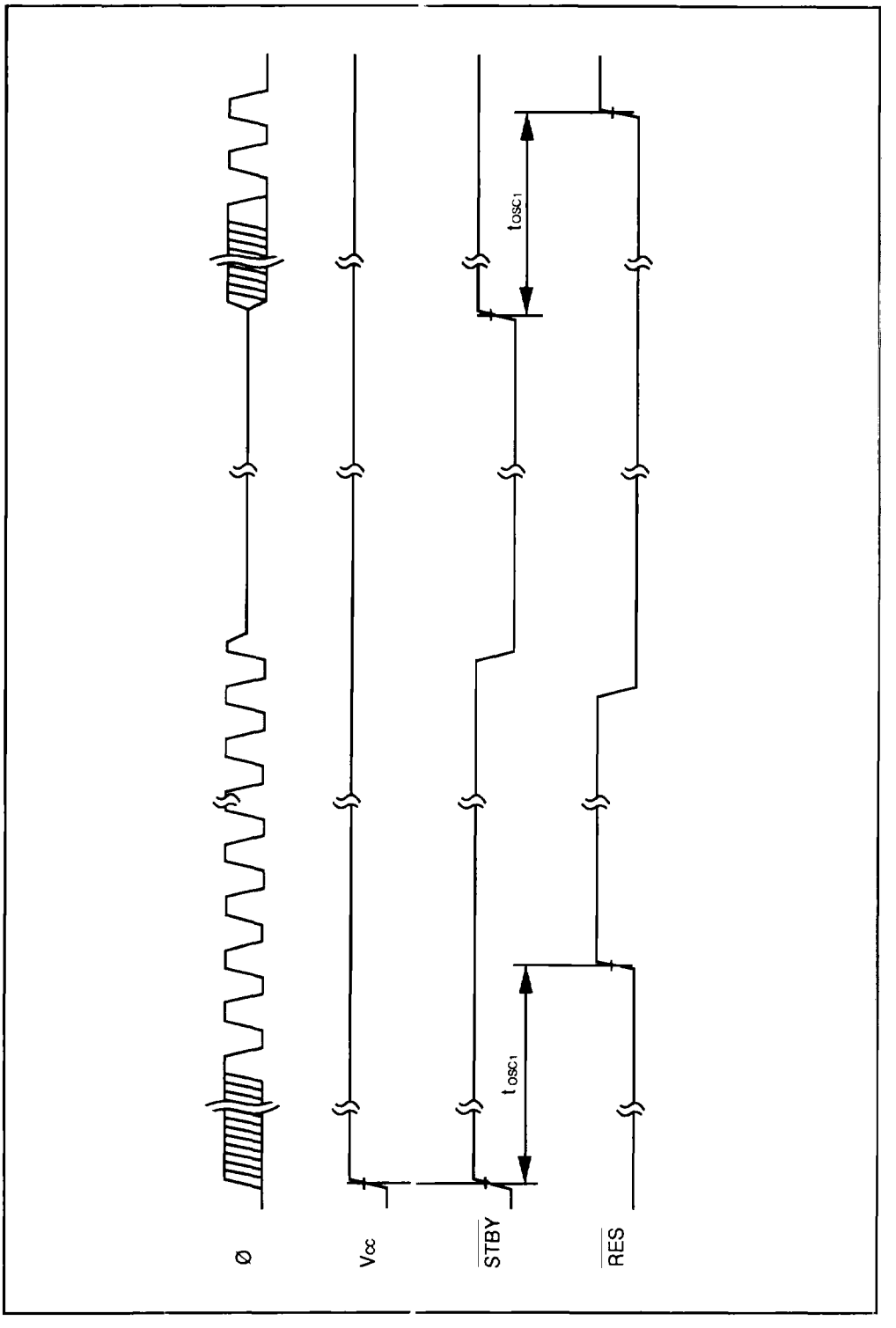

Figure 15-9. Clock Settling Timing

(4) Clock Settling Timing for Recovery from Software Standby Mode

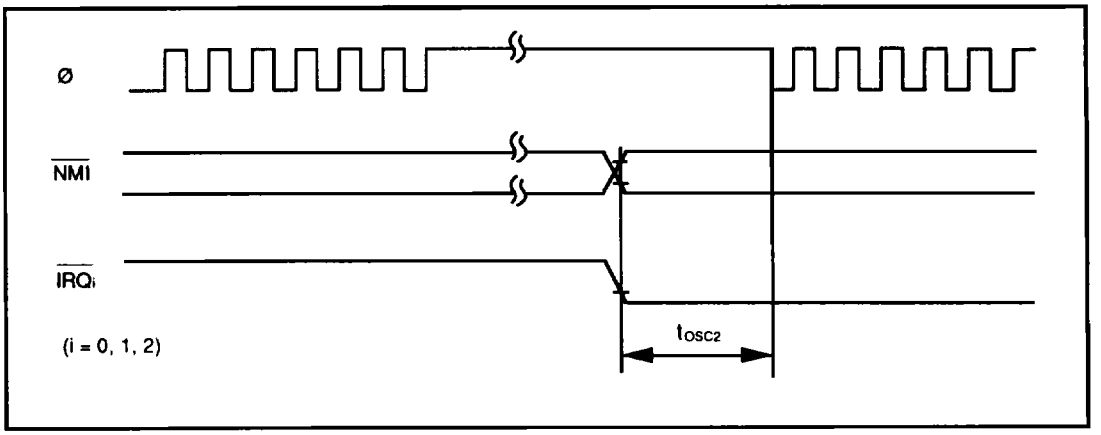

Figure 15-10. Clock Settling Timing for Recovery from Software Standby Mode

15.3.3 16-Bit Free-Running Timer Timing

(1) Free-Running Timer Input/Output Timing

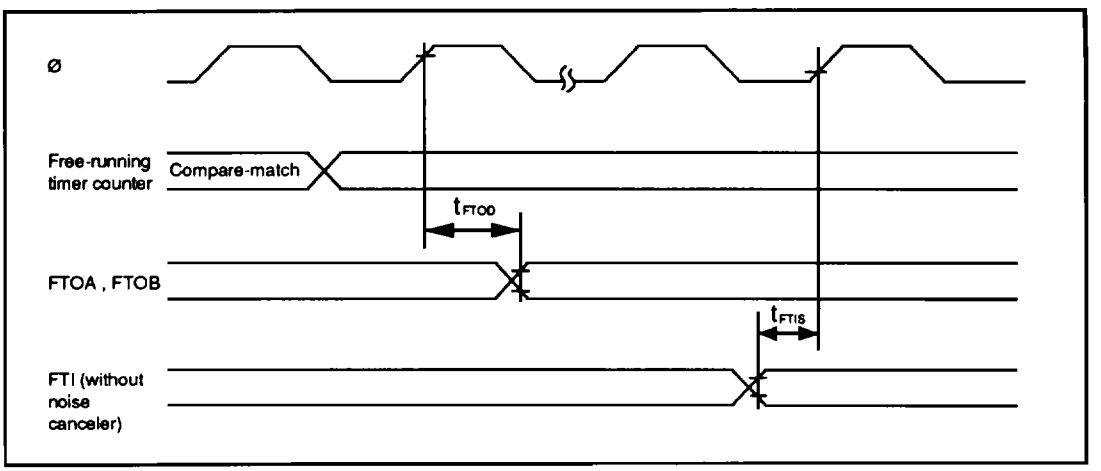

Figure 15-11. Free-Running Timer Input/Output Timing

(2) External Clock Input Timing for Free-Running Timer

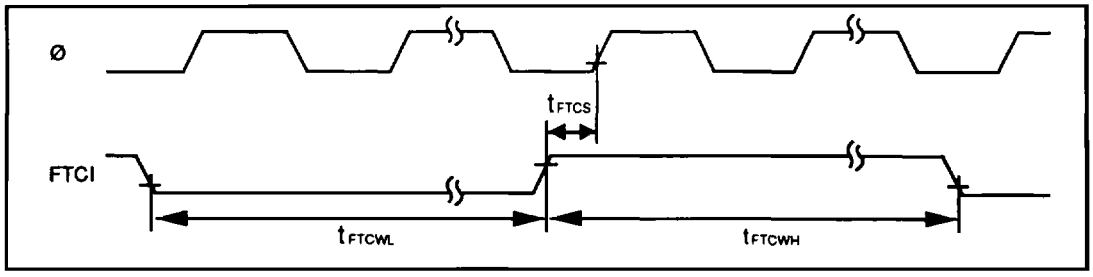

Figure 15-12. External Clock Input Timing for Free-Running Timer

15.3.4 8-Bit Timer Timing

(1) 8-Bit Timer Output Timing

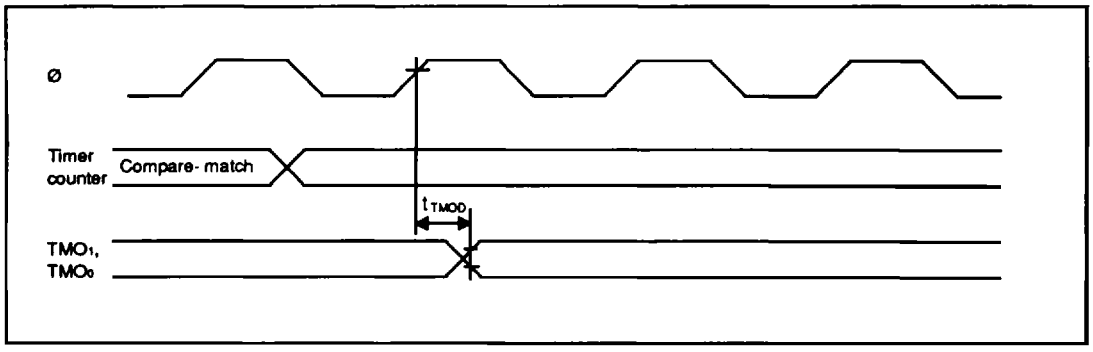

Figure 15-13. 8-Bit Timer Output Timing

(2) 8-Bit Timer Clock Input Timing

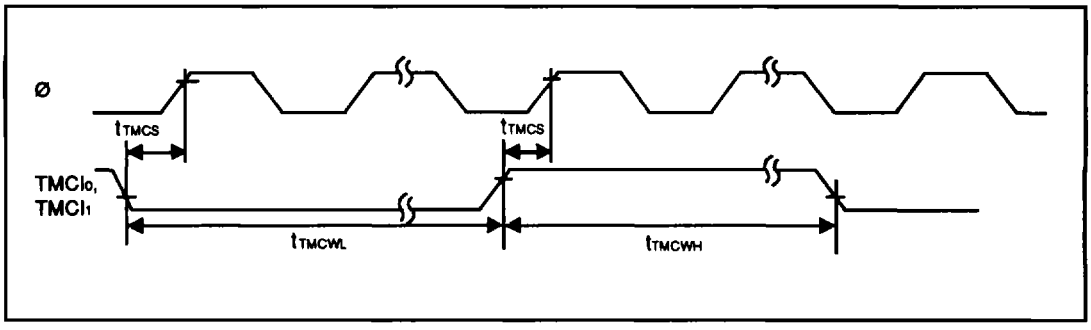

Figure 15-14. 8-Bit Timer Clock Input Timing

(3) 8-Bit Timer Reset Input Timing

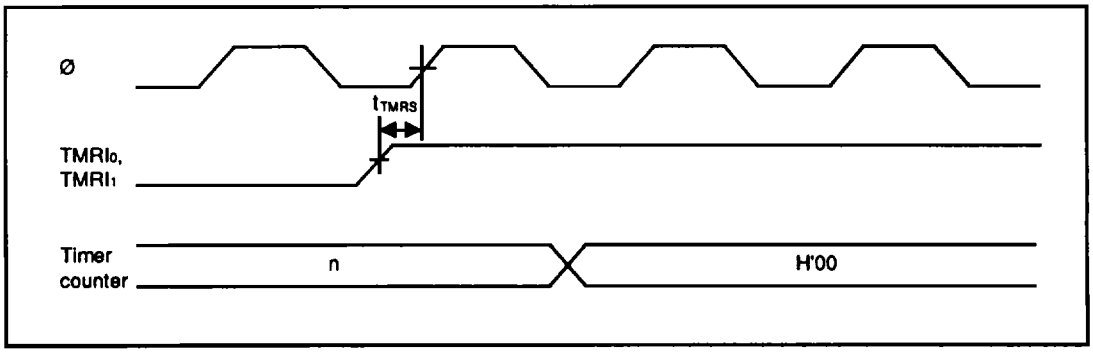

Figure 15-15. 8-Bit Timer Reset Input Timing

15.3.5 Serial Communication Interface Timing

(1) SCI Input/Output Timing

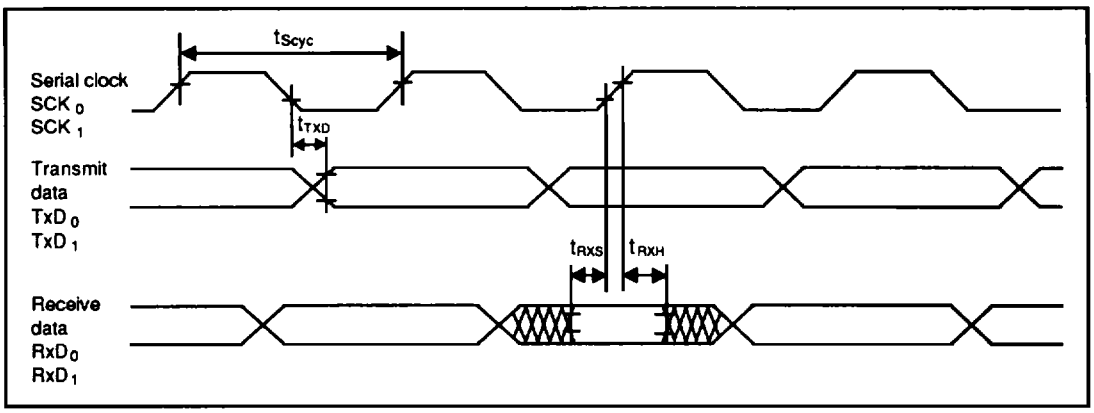

Figure 15-16. SCI Input/Output Timing (Synchronous Mode)

(2) SCI Input Clock Timing

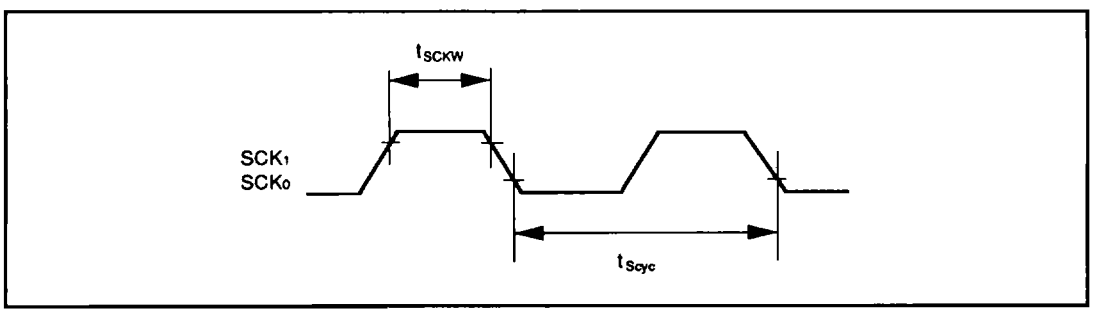

Figure 15-17. SCI Input Clock Timing

15.3.6 I/O Port Timing

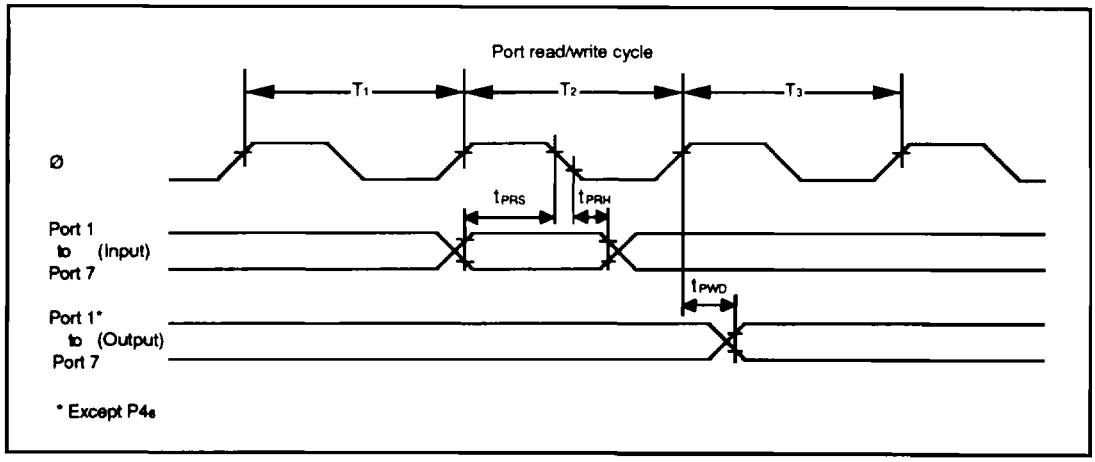

Figure 15-18. I/O Port Input/Output Timing

15.3.7 Parallel Handshake Interface Timing

(1) Input Strobe Input Timing

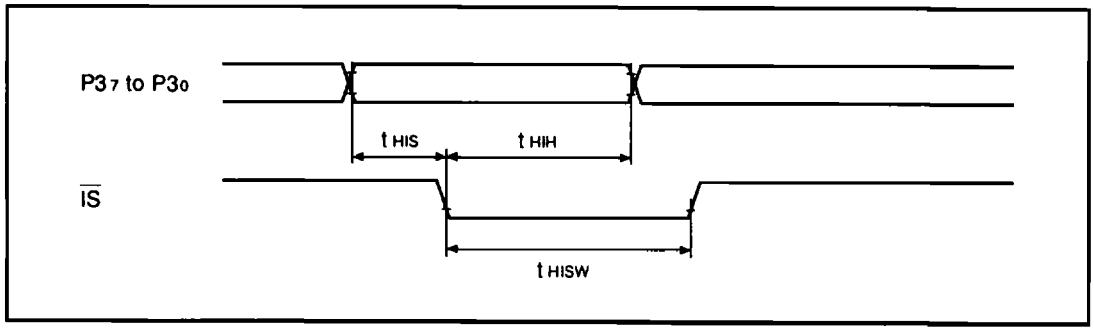

Figure 15-19. Input Strobe Input Timing

(2) Output Strobe Output Timing

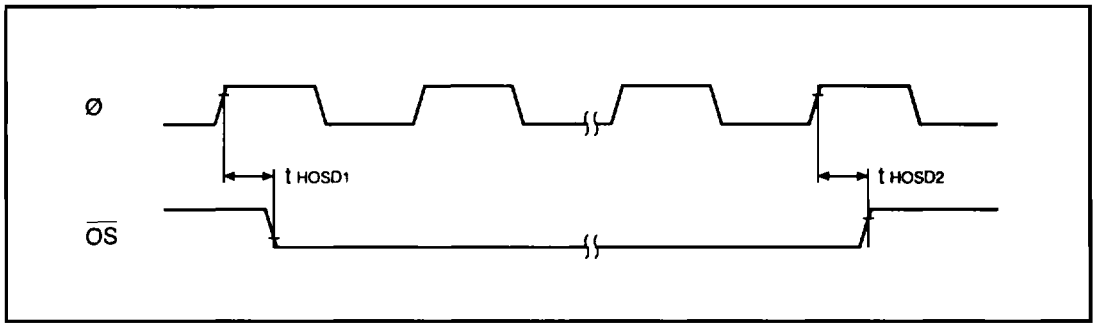

Figure 15-20. Output Strobe Output Timing

(3) Busy Output Timing

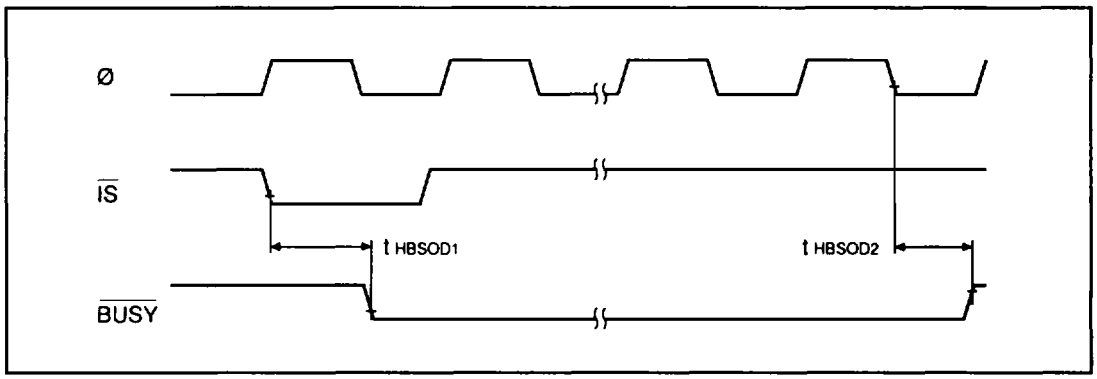

Figure 15-21. Busy Output Timing