M28F008
8 MBIT (1 MBIT x 8) FLASH MEMORY

- **High-Density Symmetrically Blocked Architecture**
  - **Sixteen 64 Kbyte Blocks**
- **Extended Cycling Capability**
  - **10K Block Erase Cycles Minimum**
  - **160K Block Erase Cycles per Chip**
- **Automated Byte Write and Block Erase**
  - **Command User Interface**
  - **Status Register**
- **System Performance Enhancements**
  - **RY/$\overline{BY}$ Status Output**
  - **Erase Suspend Capability**
- **SRAM-Compatible Write Interface**
- **Very High-Performance Read**
  - **100 ns Maximum Access Time**
- **Hardware Data Protection Feature**
  - **Erase/Write Lockout during Power Transitions**
- **Industry Standard Packaging**
  - **40-Lead Sidebrazed DIP**
  - **42-Lead Flatpack**
- **ETOX™ Nonvolatile Flash Technology**
  - **12V Byte Write/Block Erase**
- **Independent Software Vendor Support**
  - **Microsoft* Flash File System (FFS)**

The M28F008 8-Mbit FlashFile Memory is the highest density nonvolatile read/write solution for solid state storage. The M28F008's extended cycling, symmetrically blocked architecture, fast access time, write automation and low power consumption provide a more reliable, lower power, lighter weight and higher performance alternative to traditional rotating disk technology. The M28F008 brings new capabilities to portable computing. Application and operating system software stored in resident flash memory arrays provide instant-on, rapid execute-in-place and protection from obsolescence through in-system software updates. Resident software also extends system battery life and increases reliability by reducing disk drive accesses.

For high-density data acquisition applications, the M28F008 offers a more cost-effective and reliable alternative to SRAM and battery. Traditional high density embedded applications, such as telecommunications, can take advantage of the M28F008's nonvolatility, blocking and minimal system code requirements for flexible firmware and modular software designs.

The M28F008 is offered in 40-lead sidebrazed DIP and 42-lead Flatpack packages. This device uses an integrated Command User Interface and state machine for simplified block erasure and byte write. The M28F008 memory map consists of 16 separately erasable 64 Kbyte blocks.

The M28F008 employs advanced CMOS circuitry for systems requiring low power consumption and noise immunity. Its 100 ns access time provides superior performance when compared with magnetic storage media. A deep powerdown mode lowers power consumption to 500 µW maximum thru V_{CC}. The RP power control input also provides absolute data protection during system powerup/down.

For complete Rochester ordering guide, please refer to page 2
Please contact factory for specific package availability and Military/Aerospace specifications/availability.

Rochester Ordering Guide

**Most products can also be offered as RoHS compliant, designated by a –G suffix. Please contact factory for more information.*

Rochester Part Number	Intel Part Number	Package	Temperature
MC28F008-10/B	MC28F008-10	CDIP-40	-55° to +125°C
MC28F008-12/B	MC28F008-12	CDIP-40	-55° to +125°C
MF28F008-10/B	MF28F008-10	FP-42, Ceramic	-55° to +125°C
MF28F008-12/B	MF28F008-12	FP-42, Ceramic	-55° to +125°C

PRODUCT OVERVIEW

The M28F008 is a high-performance **8 Mbit** (8,388,608 bit) memory organized as **1 Mbyte** (1,048,576 bytes) of 8 bits each. **Sixteen 64 Kbyte** (65,536 byte) **blocks** are included on the M28F008. A memory map is shown in Figure 4 of this specification. A block erase operation erases one of the sixteen blocks of memory in typically **1.6 seconds**, independent of the remaining blocks. Each block can be independently erased and written **10,000 cycles**. **Erase Suspend** mode allows system software to suspend block erase to read data or execute code from any other block of the M28F008.

The M28F008 is available in **40-lead sidebrazed DIP** and **42-lead Flatpack** packages. Pinouts are shown in Figures 2a and 2b of this specification.

The **Command User Interface** serves as the interface between the microprocessor or microcontroller and the internal operation of the M28F008.

Byte Write and Block Erase Automation allow byte write and block erase operations to be executed using a two-write command sequence to the Command User Interface. The internal **Write State Machine** (WSM) automatically executes the algorithms and timings necessary for byte write and block erase operations, including verifications, thereby unburdening the microprocessor or microcontroller. Writing of memory data is performed in byte increments typically within **9 µs**, an 80% improvement over current flash memory products. **I_{PP} byte write and block erase currents** are **30 mA maximum. V_{PP} byte write and block erase voltage** is **11.4V to 12.6V**.

The **Status Register** indicates the status of the WSM and when the WSM successfully completes the desired byte write or block erase operation.

The **RY/$\overline{BY}$** output gives an additional indicator of WSM activity, providing capability for both hardware signal of status (versus software polling) and status masking (interrupt masking for background erase, for example). Status polling using RY/$\overline{BY}$ minimizes both CPU overhead and system power consumption. When low, RY/$\overline{BY}$ indicates that the WSM is performing a block erase or byte write operation. RY/$\overline{BY}$ high indicates that the WSM is ready for new commands, block erase is suspended or the device is in deep powerdown mode.

Maximum access time is **100 ns (t_{ACC})** over the military temperature range (−55°C to +125°C) and over V_{CC} supply voltage range 4.5V to 5.5V. **I_{CC} active current** (CMOS Read) is **35 mA maximum at 8 MHz**.

When the $\overline{CE}$ and $\overline{RP}$ pins are at V_{CC}, the **I_{CC} CMOS Standby** mode is enabled.

A **Deep Powerdown** mode is enabled when the $\overline{RP}$ pin is at GND, minimizing power consumption and providing write protection. **I_{CC} current** in deep powerdown is **100 µA maximum**. Reset time of 400 ns is required from $\overline{RP}$ switching high until outputs are valid to read attempts. Equivalently, the device has a wake time of 1 µs from $\overline{RP}$ high until writes to the Command User Interface are recognized by the M28F008. With $\overline{RP}$ at GND, the WSM is reset and the Status Register is cleared.

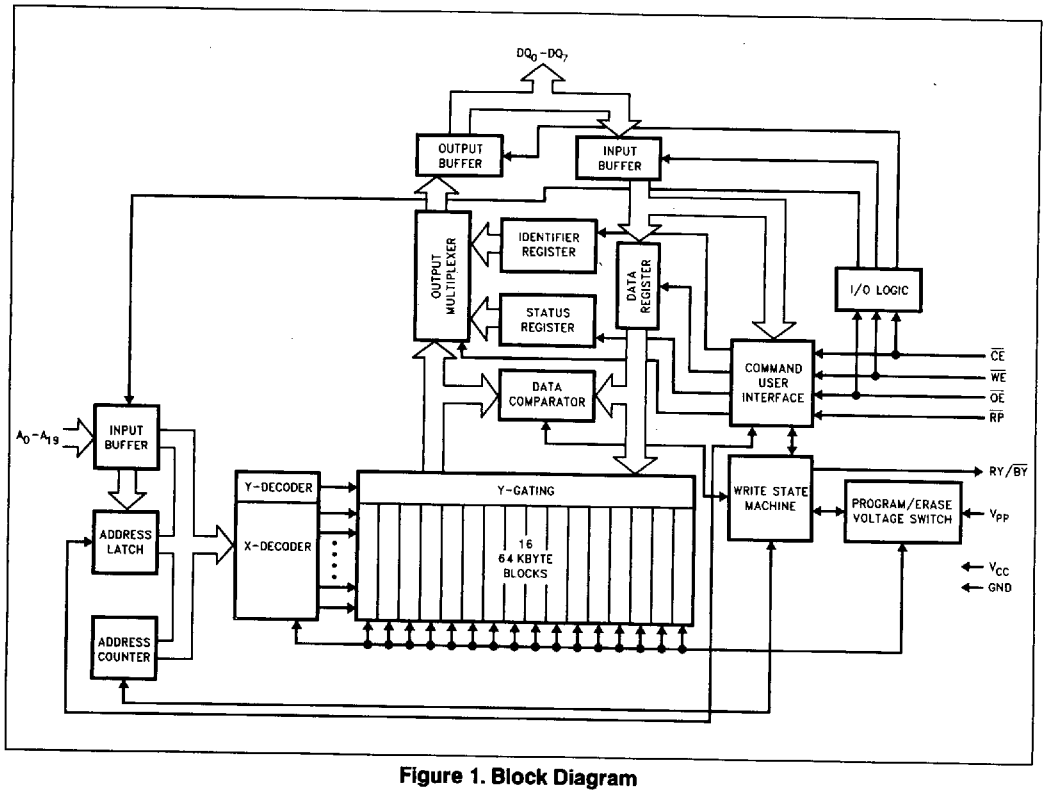


Figure 1. Block Diagram

Table 1. Pin Description

Symbol	Type	Name and Function
A_0–A_{19}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
DQ_0–DQ_7	INPUT/OUTPUT	**DATA INPUT/OUTPUTS:** Inputs data and commands during Command User Interface write cycles; outputs data during memory array, Status Register and Identifier read cycles. The data pins are active high and float to tri-state off when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders, and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels.
$\overline{RP}$	INPUT	**RESET/DEEP POWERDOWN:** Puts the device in deep powerdown mode. $\overline{RP}$ is active low; $\overline{RP}$ high gates normal operation. $\overline{RP}$ also locks out block erase or byte write operations when active low, providing data protection during power transitions. $\overline{RP}$ active resets internal automation. Exit from Deep Powerdown sets device to read-array mode.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Gates the device's outputs through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Controls writes to the Command User Interface and array blocks. $\overline{WE}$ is active low. Addresses and data are latched on the rising edge of the $\overline{WE}$ pulse.

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
RY/$\overline{BY}$	OUTPUT	**READY/$\overline{BUSY}$:** Indicates the status of the internal Write State Machine. When low, it indicates that the WSM is performing a block erase or byte write operation. RY/$\overline{BY}$ high indicates that the WSM is ready for new commands, block erase is suspended or the device is in deep powerdown mode. RY/$\overline{BY}$ is always active and does **NOT** float to tri-state off when the chip is deselected or data outputs are disabled.
V_{PP}		**BLOCK ERASE/BYTE WRITE POWER SUPPLY** for erasing blocks of the array or writing bytes of each block. **NOTE:** With $V_{PP} < V_{PPLMAX}$, memory contents cannot be altered.
V_{CC}		**DEVICE POWER SUPPLY (5V ±10%)**
GND		**GROUND**

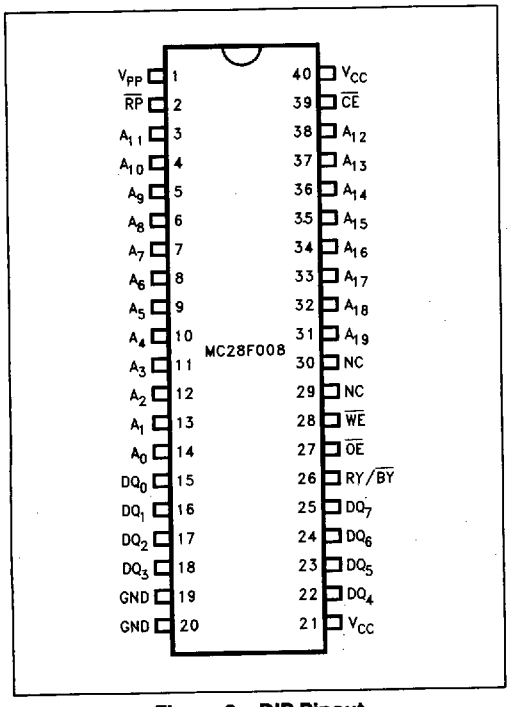


Figure 2a. DIP Pinout

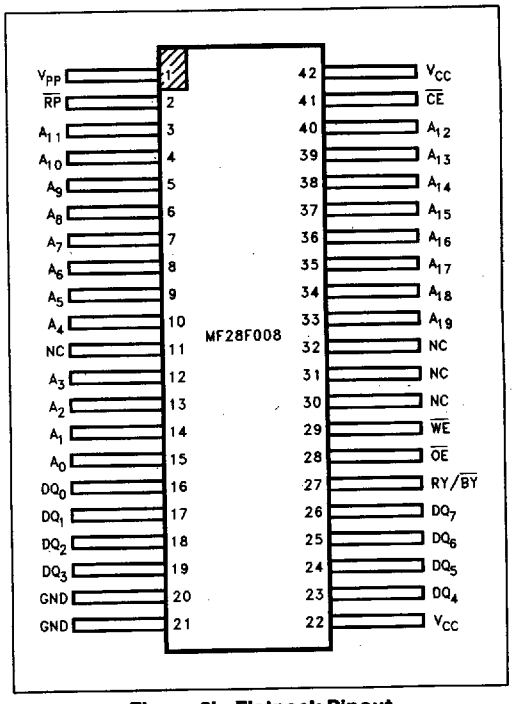


Figure 2b. Flatpack Pinout

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... −55°C to +125°C

Temperature Under Bias ..... −55°C to +125°C

Storage Temperature ..... −65°C to +125°C

Voltage on Any Pin (except V_{CC} and V_{PP}) with Respect to GND ..... −2.0V to +7.0V(1)

V_{PP} Program Voltage with Respect to GND during Block Erase/Byte Write ... −2.0V to +14.0V(1, 2)

V_{CC} Supply Voltage with Respect to GND ..... −2.0V to +7.0V(1)

Output Short Circuit Current ..... 100 mA(3)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20 ns.
2. Maximum DC voltage on V_{PP} may overshoot to +14.0V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_C	Operating Temperature	−55	+125	°C
V_{CC}	V_{CC} Supply Voltage (10%)	4.50	5.50	V

DC CHARACTERISTICS

Symbol	Parameter	Notes	MC28F008 and MF28F008		Unit	Test Conditions
			Min	Max		
I_{LI}	Input Load Current	1		±1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Load Current	1		±10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1, 3		2.0	mA	$V_{CC} = V_{CC}$ Max $\overline{CE} = \overline{RP} = V_{IH}$
				150	µA	$V_{CC} = V_{CC}$ Max $\overline{CE} = \overline{RP} = V_{CC} \pm 0.2V$
I_{CCD}	V_{CC} Deep Powerdown Current	1		100	µA	$\overline{RP}$ = GND ±0.2V I_{OUT} (RY/$\overline{BY}$) = 0 mA
I_{CCR}	V_{CC} Read Current	1		35	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE}$ = GND, F = 8 MHz, I_{OUT} = 0 mA, CMOS Inputs
				50	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, F = 8 MHz, I_{OUT} = 0 mA, TTL Inputs

DC CHARACTERISTICS (Continued)

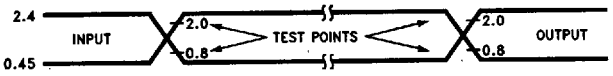
Symbol	Parameter	Notes	MC28F008 and MF28F008		Unit	Test Conditions
			Min	Max		
I_{CCW}	V_{CC} Byte Write Current	1		30	mA	Byte Write In Progress
I_{CCE}	V_{CC} Block Erase Current	1		30	mA	Block Erase In Progress
I_{CCES}	V_{CC} Erase Suspend Current	1, 2		10	mA	Block Erase Suspended $\overline{CE} = V_{IH}$
I_{PPS}	V_{PP} Standby Current	1		±15	µA	$V_{PP} \leq V_{CC}$
				200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep PowerDown Current	1		20	µA	$\overline{RP}$ = GND ±0.2V
I_{PPW}	V_{PP} Write Current	1		30	mA	$V_{PP} = V_{PPH}$ Byte Write in Progress
I_{PPE}	V_{PP} Block Erase Current	1		30	mA	$V_{PP} = V_{PPH}$ Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current	1		200	µA	$V_{PP} = V_{PPH}$ Block Erase Suspended
V_{IL}	Input Low Voltage		−0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	$V_{CC}+0.5$	V	
V_{OL}	Output Low Voltage	3		0.45	V	$V_{CC} = V_{CC}$ Min I_{OL} = 5.8 mA
V_{OH}	Output High Voltage	3	2.4		V	$V_{CC} = V_{CC}$ Min I_{OH} = −2.5 mA
V_{PPL}	V_{PP} during Normal Operations	4	0.0	6.5	V	
V_{PPH}	V_{PP} during Erase/Write Operations		11.4	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		1.8		V	

CAPACITANCE(5) T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

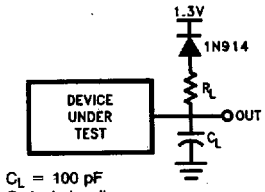
NOTES:
1. All currents are in RMS unless otherwise noted.
2. I_{CCES} is specified with the device deselected. If the M28F008 is read while in Erase Suspend Mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. Includes RY/$\overline{BY}$.
4. Block Erases/Byte Writes are inhibited when $V_{PP} = V_{PPL}$ and not guaranteed in the range between V_{PPH} and V_{PPL}.

AC INPUT/OUTPUT REFERENCE WAVEFORM



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a Logic "0". Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) < 10 ns.

AC TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance
R_L = 3.3 kΩ

AC CHARACTERISTICS—Read-Only Operations(1, 4)

Symbol		Parameter	Notes	M28F008-10(4)		M28F008-12(4)		Unit
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time		100		120		ns
t_{AVQV}	t_{ACC}	Address to Output Display			100		120	ns
t_{ELQV}	t_{CE}	$\overline{CE}$ to Output Delay	2		100		120	ns
t_{PHQV}	t_{PWH}	$\overline{RP}$ High to Output Delay			400		400	ns
t_{GLQV}	t_{OE}	$\overline{OE}$ to Output Delay	2		60		60	ns
t_{ELQX}	t_{LZ}	$\overline{CE}$ to Output Low Z	3	0		0		ns
t_{EHQZ}	t_{HZ}	$\overline{CE}$ High to Output High Z	3		55		55	ns
t_{GLQX}	t_{OLZ}	$\overline{OE}$ to Output Low Z	3	0		0		ns
t_{GHQZ}	t_{DF}	$\overline{OE}$ High to Output High Z	3		30		30	ns
	t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change, Whichever is First	3	0		0		ns

NOTES:
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. Sampled, not 100% tested.
4. See AC Input/Output Reference Waveforms and AC Testing Load Circuits for testing characteristics.

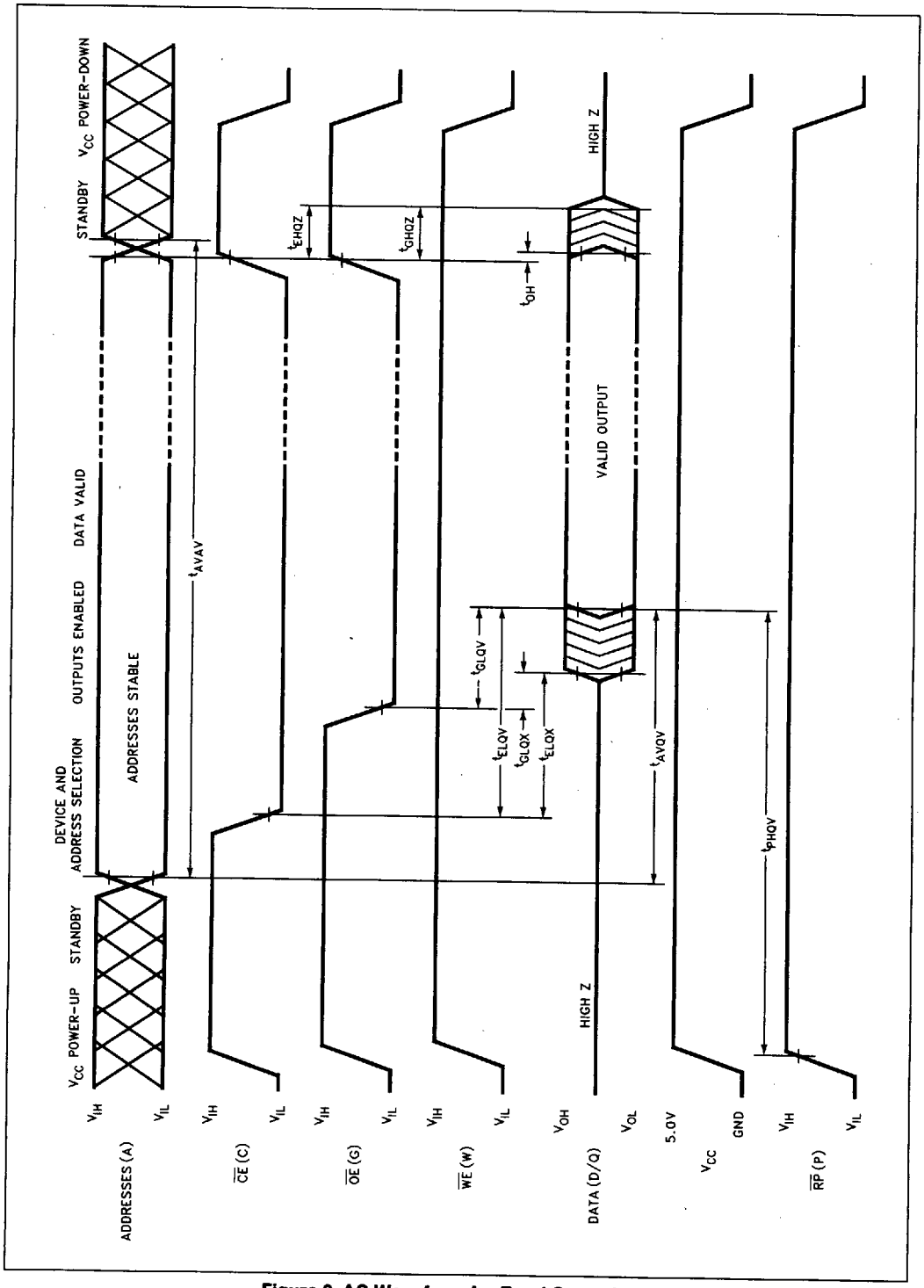


Figure 8. AC Waveform for Read Operations

AC CHARACTERISTICS—Write Operations[1, 7]

Symbol		Parameter	Notes	M28F008-10[7]		M28F008-12[7]		Unit
				Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time		100		120		ns
t_{PHWL}	t_{PS}	$\overline{RP}$ High Recovery to $\overline{WE}$ Going Low	2	1		1		µs
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low		10		10		ns
t_{WLWH}	t_{WP}	$\overline{WE}$ Pulse Width		40		40		ns
t_{VPWH}	t_{VPS}	V_{PP} Setup to $\overline{WE}$ Going High	2	100		100		ns
t_{AVWH}	t_{AS}	Address Setup to $\overline{WE}$ Going High	3	40		40		ns
t_{DVWH}	t_{DS}	Data Setup to $\overline{WE}$ Going High	4	40		40		ns
t_{WHDX}	t_{DH}	Data Hold from $\overline{WE}$ High		5		5		ns
t_{WHAX}	t_{AH}	Address Hold from $\overline{WE}$ High		5		5		ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold from $\overline{WE}$ High		10		10		ns
t_{WHWL}	t_{WPH}	$\overline{WE}$ Pulse Width High		30		30		ns
t_{WHRL}		$\overline{WE}$ High to RY/$\overline{BY}$ Going Low			100		100	ns
t_{WHQV1}		Duration of Byte Write Operation	5, 6	6		6		µs
t_{WHQV2}		Duration of Block Erase Operation	5, 6	0.3		0.3		sec
t_{WHGL}		Write Recovery before Read		0		0		µs
t_{QVVL}	t_{VPH}	V_{PP} Hold from Valid SRD, RY/$\overline{BY}$ High	2, 6	0		0		ns

NOTES:
1. Read timing characteristics during erase and byte write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Sampled, not 100% tested.
3. Refer to Table 3 for valid A_{IN} for byte write or block erasure.
4. Refer to Table 3 for valid D_{IN} for byte write or block erasure.
5. The on-chip Write State Machine incorporates all byte write and block erase system functions and overhead of standard Intel flash memory, including byte program and verify (byte write) and block precondition, precondition verify, erase and erase verify (block erase).
6. Byte write and block erase durations are measured to completion (SR.7 = 1, RY/$\overline{BY}$ = V_{OH}). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success (SR.3/4/5 = 0)
7. See AC Input/Output Reference Waveforms and AC Testing Load Circuits for testing characteristics.

BLOCK ERASE AND BYTE WRITE PERFORMANCE

Parameter	Notes	M28F008-10			M28F008-12			Unit
		Min	Typ	Max	Min	Typ	Max	
Block Erase Time	1, 2		1.6	10		1.6	10	sec
Block Write Time	1, 2		0.6	2.1		0.6	2.1	sec

NOTES:
1. 25°C, 12.0 V_{PP}.
2. Excludes System-Level Overhead.

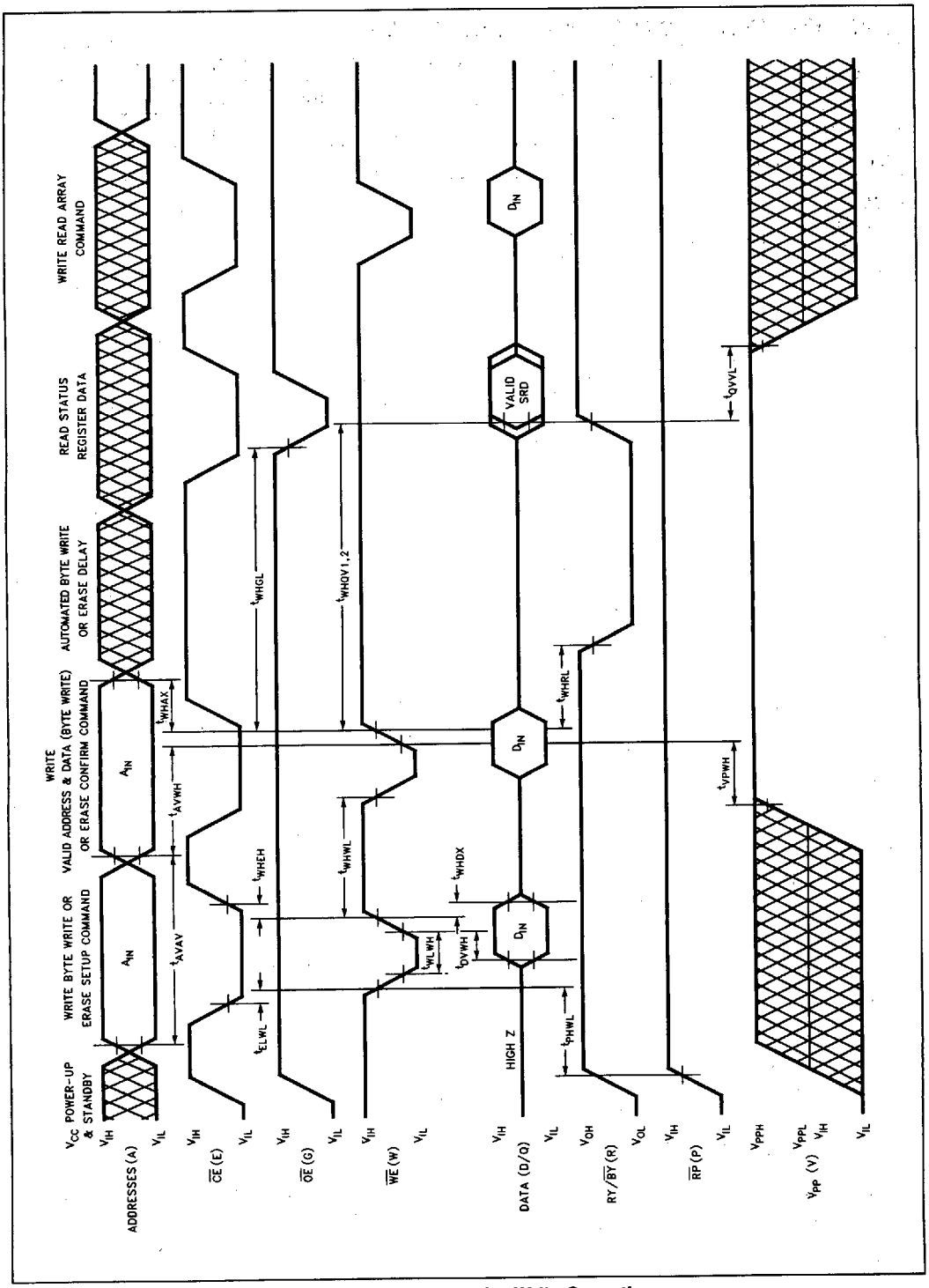


Figure 9. AC Waveform for Write Operations

ALTERNATIVE $\overline{CE}$-CONTROLLED WRITES(1)

Symbol		Parameter	Notes	M28F008-10(6)		M28F008-12(6)		Unit
				Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time		100		120		ns
t_{PHEL}	t_{PS}	$\overline{RP}$ High Recovery to $\overline{CE}$ Going Low	2	1		1		μs
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup to $\overline{CE}$ Going Low		0		0		ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		50		50		ns
t_{VPEH}	t_{VPS}	V_{PP} Setup to $\overline{CE}$ Going High	2	100		100		ns
t_{AVEH}	t_{AS}	Address Setup to $\overline{CE}$ Going High	3	40		40		ns
t_{DVEH}	t_{DS}	Data Setup to $\overline{CE}$ Going High	4	40		40		ns
t_{EHDX}	t_{DH}	Data Hold from $\overline{CE}$ High		5		5		ns
t_{EHAX}	t_{AH}	Address Hold from $\overline{CE}$ High		5		5		ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold from $\overline{CE}$ High		0		0		ns
t_{EHEL}	t_{EPH}	$\overline{CE}$ Pulse Width High		25		25		ns
t_{EHRL}		$\overline{CE}$ High to RY/$\overline{BY}$ Going Low			100		100	ns
t_{EHQV1}		Duration of Byte Write Operation	5	6		6		μs
t_{EHQV2}		Duration of Block Erase Operation	5	0.3		0.3		sec
t_{EHGL}		Write Recovery before Read		0		0		μs
t_{QVVL}	t_{VPH}	V_{PP} Hold from Valid SRD, RY/$\overline{BY}$ High	2, 5	0		0		ns

NOTES:
1. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of $\overline{CE}$ and $\overline{WE}$. In systems where $\overline{CE}$ defines the write pulsewidth (within a longer $\overline{WE}$ timing waveform), all setup, hold and inactive $\overline{WE}$ times should be measured relative to the $\overline{CE}$ waveform.
2. Sampled, not 100% tested.
3. Refer to Table 3 for valid A_{IN} for byte write or block erasure.
4. Refer to Table 3 for valid D_{IN} for byte write or block erasure.
5. Byte write and block erase durations are measured to completion (SR.7 = 1, RY/$\overline{BY}$ = V_{OH}). V_{PP} should be held at V_{PPH} until determination of byte write/block erase success (SR.3/4/5 = 0)
6. See AC Input/Output Reference Waveforms and AC Testing Load Circuits for testing characteristics.

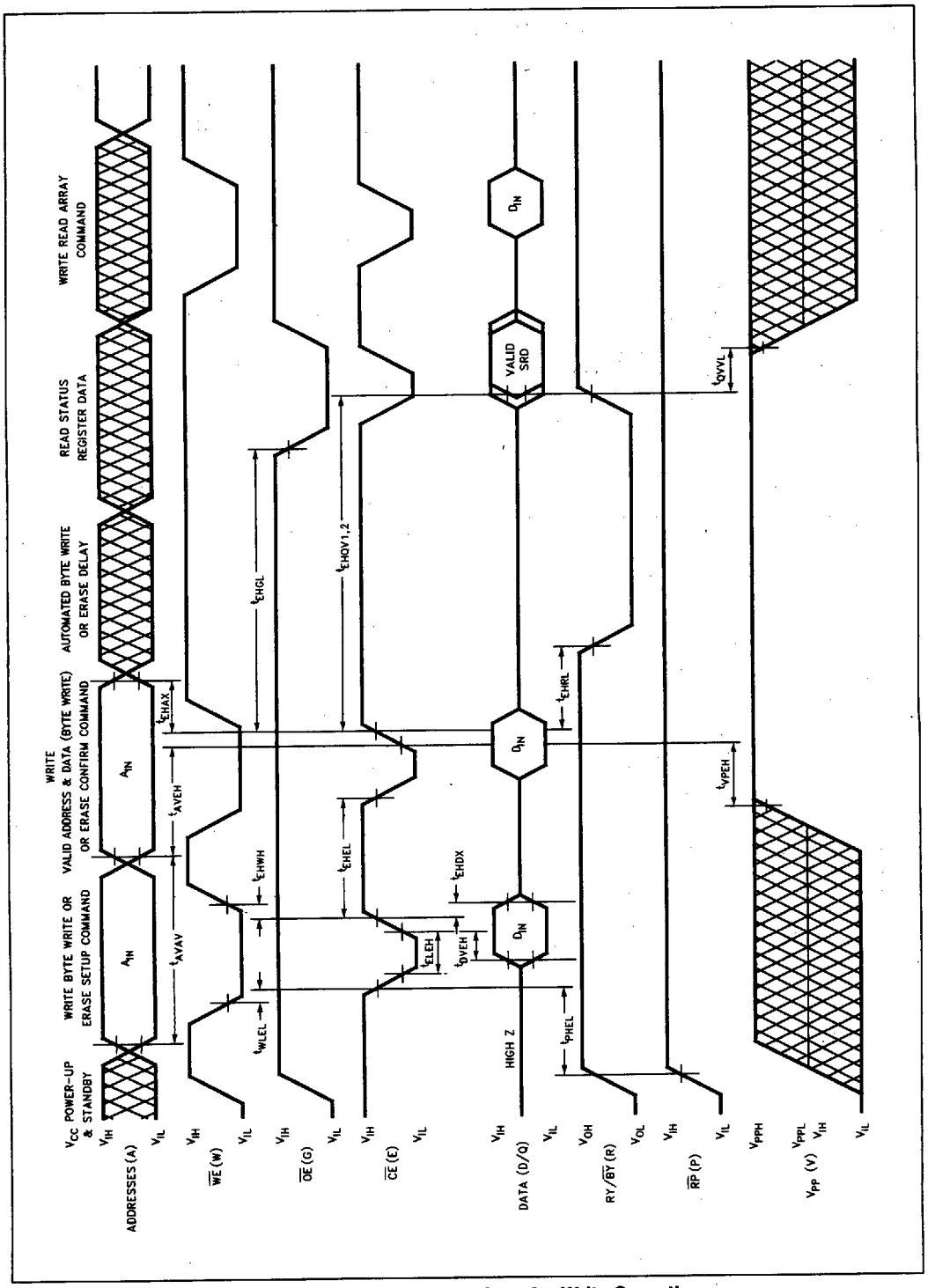


Figure 10. Alternate AC Waveform for Write Operations