HARRIS

CDP68HC68R1
CDP68HC68R2

CMOS 128 Word (CDP68HC68R1) and 256 Word (CDP68HC68R2) by 8-Bit Static RAMs

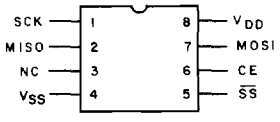
January 1991

Features

- Fully Static Operation
- Operating Voltge Range ..... 3V to 5.5V
- Typical Standby Current 1µA
- Directly Compatible with Harris/Motorola SPI Bus
- Separate Data Input and Three State Data Output Pins
- Input Data and clock buffers Gated Off with Chip Enable
- Automatic Sequencing for Fast Multiple Byte Accesses
- Low Minimum Data Retention Voltage 2V
- Wide Operating Temperature Range: -40°C to +85°C

Pinout

PACKAGE TYPE E
TOP VIEW



Description

The CDP68HC68R1 and CDP68HC68R2 are 128 word and 256 word by 8-bit static random access memories, respectively. The memories are intended for use in systems utilizing a synchronous serial three wire (clock, data in, and data out) interface where minimum package size, interconnect wiring, low power, and simplicity of use are desirable. These parts will interface directly with CDP68HC05D2, CDP68HC05C4, and CDP68HC05C8 microcomputers (providing the CPHA bit in the microcomputer's SPI Control Register is set equal to 1). The CDP68HC68R1 and CDP68HC68R2 are also compatible with general purpose microcomputers, including the CDP1804A and CDP6805 family, by utilizing I/O bits for the SPI (Serial Peripheral Interface) bus. Other industry microcomputers such as the 80C51 can also interface to these serial RAMs.

The CDP68HC68R1 and CDP68HC68R2 are supplied in 8 lead plastic Mini DIP packages. (E suffix).

TRUTH TABLE

MODE	SIGNAL				
	CE	$\overline{SS}$	SCK	MOSI	MISO
Disabled and Reset	L X	X H	Input Disabled	Input Disabled	High Z
Read or Write	H	L	CPOL = 0, ⌐¯ CPOL = 1, ¯⌐	Data Bit Latch	High Z During Write, Current Data Bit During Read
Shift	H	L	CPOL = 0, ¯⌐ CPOL = 1, ⌐¯	X	Next Data Bit

NOTE: MISO remains at a High Z until 8 bits of data are ready to be shifted out during a Read and it remains at a High Z during the entire Write cycle. The CPHA bit must be set = 1 in the Serial Peripheral control register of 6805 microcomputers in order to communicate with these devices.

File Number **1544.1**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(All voltage values referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A=-40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A=+60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A=FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E ..... -40° to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = -40° to +85°C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS ALL TYPES		UNITS
		MIN.	MAX.	
DC Operating Voltage Range		3	5.5	V
Input Voltage Range	V_{IH}	0.7 V_{DD}	V_{DD} +0.3	
	V_{IL}	-0.3	0.2 V_{DD}	
Serial Clock Frequency	f_{SCK}			MHz
V_{DD}=3 V		—	1.05	
V_{DD}=4.5 V		—	2.1	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} = 3.3 V ±10%, Except as Noted

CHARACTERISTIC	CONDITIONS	LIMITS CDP68HC68R1			CDP68HC68R2			UNITS
		MIN.	TYP.•	MAX.	MIN.	TYP.•	MAX.	
Standby Device Current I_{DDS}	—	—	1	15	—	1	50	μA
Output Voltage High Level V_{OH}	I_{OH}=-0.4 mA, V_{DD}=3 V	2.7	—	—	2.7	—	—	V
Output Voltage Low Level V_{OL}	I_{OL}=0.4 mA, V_{DD}=3 V	—	—	0.3	—	—	0.3	
Input Leakage Current, I_{IN}	—	—	*	±1	—	*	±1	μA
3-State Output Leakage Current, I_{OUT}	—	—	—	±10	—	—	±10	
Operating Device Current I_{OPER}#	V_{IN}=V_{IL},V_{IH}	—	5	10	—	5	10	mA
Input Capacitance, C_{IN}	V_{IN}=0 V, f=1 MHz, T_A=25°C	—	4	6	—	4	6	pF

•Typical values are for T_A = 25°C and nominal V_{DD}.
#Outputs open circuited; cycle time = Min. t_{cycle}, duty = 100%.
*Typical input current values (high and low) for pins 1, 5, 6, 7, approximately 100 nA due to presence of feedback transistor. Pin 6 is an exception - I_{in}(high) typically 1 nA.

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} = 5 V ±10%, Except as Noted

CHARACTERISTIC	CONDITIONS	LIMITS						UNITS
		CDP68HC68R1			CDP68HC68R2			
		MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
Standby Device Current I_{DDS}	—	—	1	15	—	1	50	μA
Output Voltage High Level V_{OH}	I_{OH}=-1.6 mA, V_{DD}=4.5 V	3.7	—	—	3.7	—	—	V
Output Voltage Low Level V_{OL}	I_{OL}=1.6 mA, V_{DD}=4.5 V	—	—	0.4	—	—	0.4	V
Output Voltage High Level V_{OH}	I_{OH}≤10 μA, V_{DD}=4.5 V	4.4	—	—	4.4	—	—	V
Output Voltage Low Level V_{OL}	I_{OL}≤10 μA, V_{DD}=4.5 V	—	—	0.1	—	—	0.1	V
Input Leakage Current, I_{IN}	—	—	*	±1	—	*	±1	μA
3-State Output Leakage Current, I_{OUT}	—	—	—	±10	—	—	±10	μA
Operating Device Current I_{OPER}#	V_{IN}=V_{IL},V_{IH}	—	5	10	—	5	10	mA
Input Capacitance, C_{IN}	V_{IN}=0 V, f=1 MHz, T_A=25°C	—	4	6	—	4	6	pF

•Typical values are for T_A = 25°C and nominal V_{DD}.

#Outputs open circuited; cycle time = Min. t_{cycle}, duty = 100%.

*Typical input current values (high and low) for pins 1, 5, 6, 7, approximately 100 nA due to presence of feedback transistor. Pin 6 is an exception - I_{in}(high) typically 1 nA.

PIN SIGNAL DESCRIPTION

SCK (Serial Clock Input)* - This input causes serial data to be latched from the MOSI input and shifted out on the MISO output.

MOSI (Master Out/Slave In)* - Data bytes are shifted in at this pin most significant bit (MSB) first.

MISO (Master In/Slave Out)* - Data bytes are shifted out at this pin most significant bit (MSB) first.

$\overline{SS}$ (Slave Select)* - A negative chip select input. A high level at this input holds the serial interface logic in a reset state.

CE (Chip Enable)** - A positive chip enable input. A low level at this input holds the serial interface logic in a reset state.

CE · SS - This is a logical function of CE and $\overline{SS}$ used throughout this data sheet to simplify diagrams. CE · SS = 1 when pin 5 is low and pin 6 is high. CE · SS = 0 at all other times.

*These inputs will retain their previous state if the line driving them goes into a HIGH-Z state.

**The CE input has an internal pull-down device—if the input is driven to a low state before going to a HIGH Z.

FUNCTIONAL DESCRIPTION

The Serial Peripheral Interface (SPI) utilized by the CDP68HC68R1 and CDP68HC68R2, is a serial synchronous bus for address and data transfers. The clock, which is generated by the microcomputer, is active only during address and data transfers. In systems using the CDP68HC05C4, CDP68HC05C8 or CDP68HC05D2, the inactive clock polarity is determined by the CPOL bit in the microcomputer's control register. A unique feature of the CDP68HC68R1 and CDP68HC68R2 is that they automatically determine the level of the inactive clock by sampling SCK when CE • SS becomes active (see Fig. 1). Input data (MOSI) is latched internally on the Internal Strobe edge and output data (MISO) is shifted out on the Shift edge, as defined by Fig. 1. There is one clock for each data bit transferred (address as well as data bits are transferred in groups of 8).

ADDRESS AND DATA FORMAT

The address and data bytes are shifted MSB first into the serial data input (MOSI) and out of the serial data output (MISO). The Address/Control byte (see Fig. 2b) contains a Write/$\overline{Read}$ bit and a 7-bit address. Any transfer of data requires an Address/Control byte to specify a RAM location, followed by one or more bytes of data. Data is transferred out of MISO for a Read and into MOSI for a Write. Address/Control bytes are recognizable because they are the first byte transferred following a valid CE · SS (except for Page select bytes, see PAGE SELECTION). To transmit a new address, CE · SS must first go false and then true again.

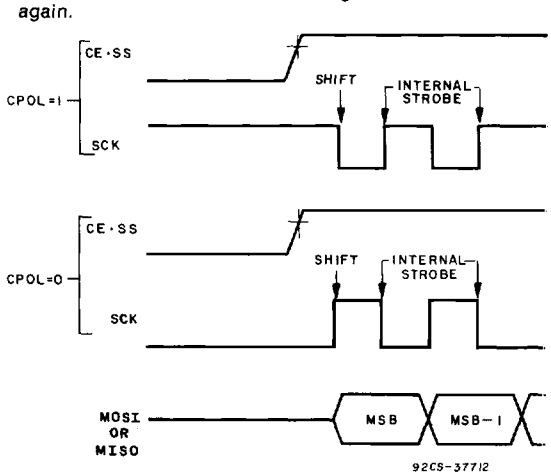


Fig. 1 - Serial RAM clock (SCK) as a function of MCU clock polarity (CPOL).

a. Page/Device Byte (CDP68HC68R2 Only)

BIT	7	6	5	4	3	2	1	0
	X	X	X	X	X	X	X	A7

b. Address/Control Byte

BIT	7	6	5	4	3	2	1	0
	W/$\overline{R}$	A6	A5	A4	A3	A2	A1	A0

A0-A6 The seven least significant RAM address bits, sufficient to address 128 bytes.

W/$\overline{R}$ Read or Write data transfer control bit. W/$\overline{R}$ = 0 initiates one or more memory read cycles. W/$\overline{R}$ = 1 initiates one or more memory write cycles.

c. Data Byte

BIT	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

Fig. 2 - Serial byte format.

PAGE SELECTION (CDP68HC68R2 Only)

For the CDP68HC68R2, a Page/Device byte is sent from the microcomputer before the Address/Control byte. Because the Address/Control byte is limited to 128 addresses, the CDP68HC68R2 is divided into two 128-byte pages. A page select is accomplished by enabling the CDP68HC68R2, transmitting the Page/Device Select byte (see Fig. 2a), and finally disabling the device prior to any more data transfers. The Page/Device byte is recognizable because it is the only time that a single byte is transferred to the RAM before CE · SS is disabled (see Fig. 3). The page select is latched and remains until changed or is incremented during a burst transfer (see next section).

ADDRESS AND DATA

Data transfers can occur one byte at a time (Fig. 4) or in a multi-byte burst mode (Fig. 5). After the chip is enabled, an address word is sent to select one of the 128 bytes (on the selected page) and specify the type of operation (i.e., Read or Write). For a single byte Read or Write (Fig. 4), one byte is transferred to or from the location specified in the Address/Control byte; the device is then disabled. Additional reading or writing requires re-enabling the RAM and providing a new Address/Control byte. If the RAM is not disabled, additional bytes can be read or written in a burst mode (Fig. 5). Each Read or Write cycle causes the latched

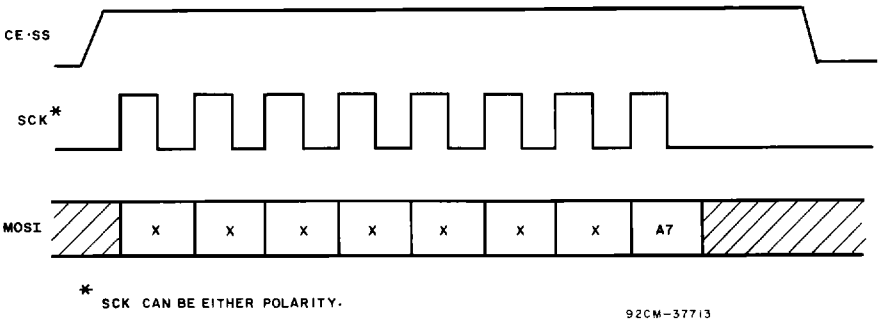


Fig. 3 - Page/Device Select byte transfer waveforms.

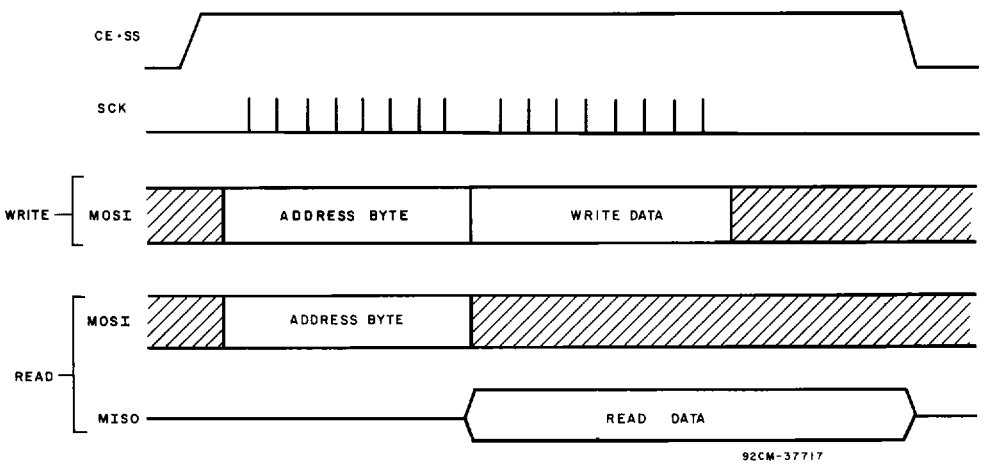


Fig. 4 - Single-byte transfer.

RAM address to automatically increment. Incrementing continues after each transfer until the device is disabled. After incrementing to 7FH on the CDP68HC68R1 or to FFH on the CDP68HC68R2, the address will recycle to 00H and continue. Note that incrementing past 7FH on the CDP-68HC68R2 causes the address to go to location 80H (i.e., location 00H of page 1). The programmer must take care to keep track when crossing page boundaries.

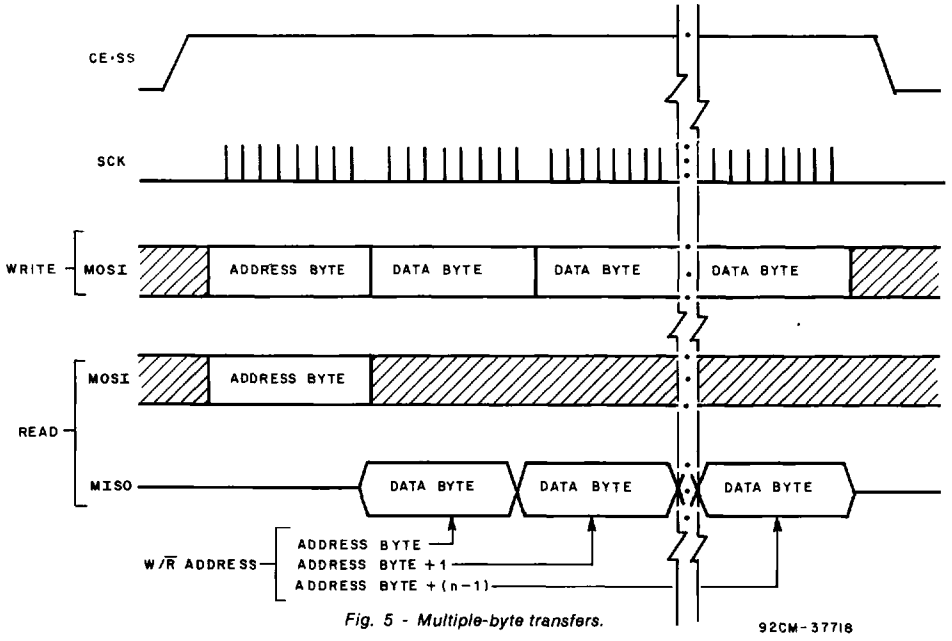


Fig. 5 - Multiple-byte transfers.

DYNAMIC ELECTRICAL CHARACTERISTICS - BUS TIMING V_{DD} ±10%, V_{SS} = 0 V dc, T_A = -40° to +85°C, C_L = 200 pF. See Figs. 6, 7 and 8.

IDENT. NUMBER	CHARACTERISTIC		LIMITS (ALL TYPES)				UNITS
			V_{DD}=3.3 V		V_{DD}=5 V		
			Min.	Max.	Min.	Max.	
(1)	Chip Enable Set-Up Time	t_{EVCV}	200	—	100	—	ns
(2)	Chip Enable after Clock Hold Time	t_{CVEX}	250	—	125	—	
(3)	Clock Width High	t_{WH}	400	—	200	—	
(4)	Clock Width Low	t_{WL}	400	—	200	—	
(5)	Data In to Clock Set-Up Time	t_{DVCV}	200	—	100	—	
(6)	Data In after Clock Hold Time	t_{CVDX}	200	—	100	—	
(7)	Clock to Data Propagation Delay	t_{CVDV}	—	200	—	100	
(8)	Chip Disable to Output High Z	t_{EXQZ}	—	200	—	100	
(11)	Output Rise Time	t_r	—	200	—	100	
(12)	Output Fall Time	t_f	—	200	—	100	
(A)	Clock to Data Out Active	t_{CVQX}	—	200	—	100	
(B)	Clock Recovery Time	t_{REC}	200	—	200	—	

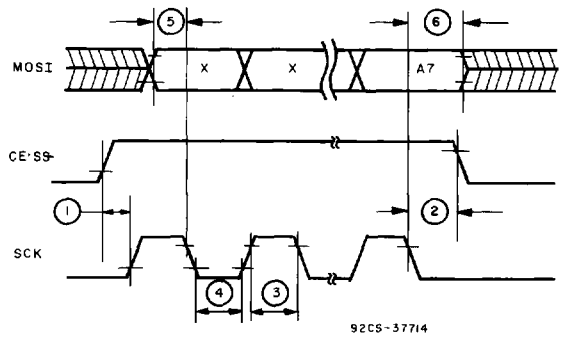


Fig. 6 - Page/Device byte timing waveforms.

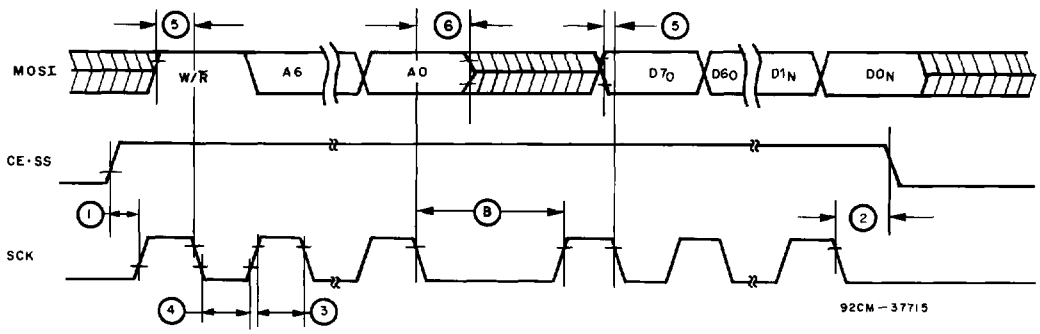


Fig. 7 - WRITE cycle timing waveforms.

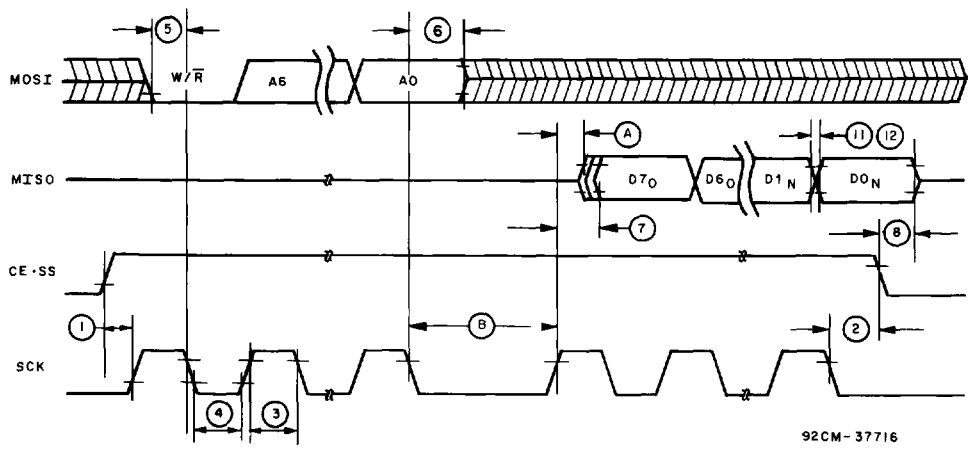


Fig. 8 - READ cycle timing waveforms.

DATA RETENTION CHARACTERISTICS at T_A = -40° to +85°C

CHARACTERISTIC		TEST CONDITIONS	LIMITS ALL TYPES MIN.	LIMITS ALL TYPES MAX.	UNITS
Minimum Data Retention Voltage	V_{DR}	$\overline{CS} \geq V_{DD}$ -0.2 V	2	—	V
Data Retention Quiescent Current	$I_{DD}DR$	V_{DD} = 2 V, CE = V_{SS}	—	1	μA