KEY FEATURES

- **SMPTE 292M compliant**
- **NRZ(I) encoding**
- **SMPTE 292M scrambler with BYPASS option**
- **selectable TRS insertion**
- **selectable line number insertion**
- **selectable line based CRC insertion**
- **selectable active picture illegal code re-mapping**
- **20 bit 3.3V CMOS compatible input data bus**
- **optimized output interface to GS1522**
- **Pb-free and Green**
- **single +3.3V power supply**
- **5V tolerant I/O**

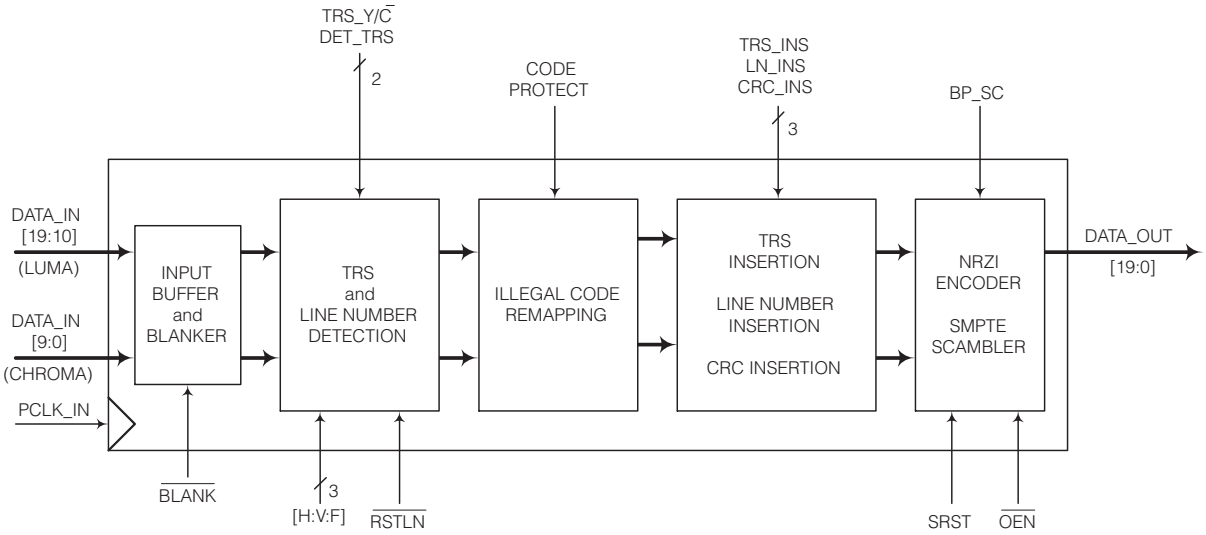
APPLICATIONS

- SMPTE 292M Serial Digital Interfaces

DESCRIPTION

The GS1511 HDTV Serial Digital Formatter formats the HDTV Luma and Chroma data according to SMPTE 292M prior to serialization by the GS1522 HDTV Serializer. The GS1511 optionally inserts TRS and line number signals based on externally supplied H, V and F signals. The device also allows the insertion of CRCs based on TRS signals embedded in the input data streams, should the user choose not to supply external HVF signals.

Following the insertion of TRS, Line Number, and CRC, protected words of 000-003 and 3FC to 3FF occurring during the active video period are optionally re-mapped to 004 and 3FB respectively. Prior to exiting the device SMPTE 292M compliant NRZ(I) encoding and scrambling may be performed on the data stream.



GS1511 FUNCTIONAL BLOCK DIAGRAM

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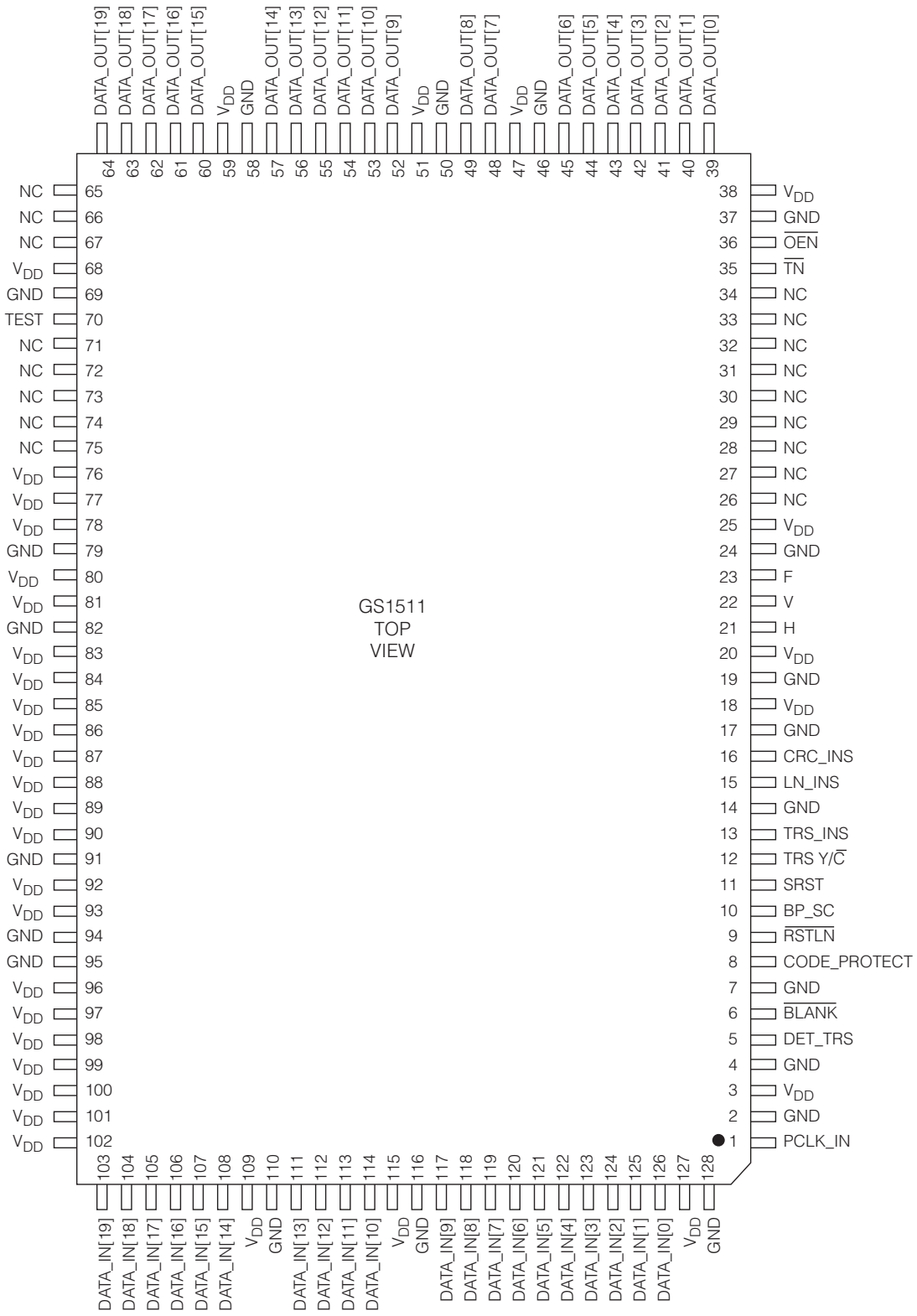
1. PIN OUT

1.1 PIN ASSIGNMENT



1.2 PIN DESCRIPTIONS

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
1	PCLK_IN	Synchronous	Input	**Parallel Data Clock input.** 74.25MHz or 74.25/1.001MHz.
2, 4, 14, 19, 24, 37, 46, 50, 58, 69, 79, 82, 91, 94, 110, 116, 128	GND	N/A	Ground	**Ground.** Ground power supply connections.
3, 20, 25, 38, 47, 51, 59, 68, 78, 81, 90, 93, 99, 102, 109, 115, 127	V_{DD}	N/A	Power	**Power.** Positive power supply connections.
5	DET_TRS	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable the detection of the TRS signals embedded in the video stream. When DET _TRS is high, the device detects the TRS signals embedded in the input video stream and uses the detected HVF signals instead of the external HVF signals. When DET _TRS is low, TRS detection is disabled. The device uses the external supplied HVF signals.
6	$\overline{\text{BLANK}}$	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** When $\overline{\text{BLANK}}$ is low, the device sets the accompanying LUMA and CHROMA data to their appropriate blanking levels. When $\overline{\text{BLANK}}$ is high, the LUMA and CHROMA data streams pass through this stage of the device unaltered. See timing diagram Figure 3.
7, 17, 95	GND	N/A		**Ground.** This pin must be connected to GND for normal operation.
8	CODE_PROTECT	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable re-mapping of out-of-range words contained in the active portion of the video signal. When this signal is high, the device re-maps out-of-range words contained within the active portion of the video signal into CCIR-601 compliant words. Values between 000-003 are re-mapped to 004. Values between 3FC and 3FF are re-mapped to 3FB. When this signal is low, out-of-range words in the active video region pass through the device unaltered.
9	$\overline{\text{RSTLN}}$	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** Line number reset signal which must be asserted once per frame at the beginning of the frame (for example, on the falling edge of the F signal). A high to low transition will reset the line number counter of the device to one (1). See Figure 2 for timing.
10	BP_SC	Non-synchronous	Input	**Control Signal Input.** Used to enable or bypass the SMPTE292M scrambler and NRZ(I) encoder. When BP_SC is low, the video stream is scrambled according to SMPTE 292M and NRZ(I) encoded. When BP_SC is high, the scrambler and NRZ(I) encoder are by-passed.
11	SRST	Non-synchronous	Input	**Control Signal Input.** Used to reset the SMPTE292M scrambler and NRZI encoder. When SRST is low, the scrambler and encoder operate normally. A low to high transition on SRST causes the scrambler and encoder to reset.
12	TRS_Y/$\overline{\text{C}}$	Non-synchronous	Input	**Control Signal Input.** Only used when DET_TRS is high. When TRS_Y/$\overline{\text{C}}$ is high, the device detects and uses TRS signals embedded in the LUMA (DATA_IN[19:10]) channel. When TRS_Y/$\overline{\text{C}}$ is low, the device detects and uses TRS signals embedded in the CHROMA (DATA_IN[9:0]) channel.

1.2 PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
13	TRS_INS	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable insertion of TRS into the video streams. When TRS_INS is high, the device inserts SMPTE 292M compliant TRS signals into the input LUMA and CHROMA data streams based on the supplied HVF signals. When TRS_INS is low, the device does not insert TRS signals.
15	LN_INS	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable insertion of line numbers into the video stream. When LN_INS is high, the device inserts SMPTE 292M compliant line number information into the LUMA and CHROMA channels. When LN_INS is low, the device does not insert the line number information into the LUMA and CHROMA channels. Line number insertion is only available when user supplied external FVH data is used (DET_TRS set LOW).
16	CRC_INS	Non-synchronous	Input	**Control Signal Input.** Used to enable or disable insertion of CRCs into the video stream. When CRC_INS is high, the device calculates and inserts line based CRCs. When CRC_INS is low, this feature is disabled.
18, 99, 102, 76, 77, 80, 83-89, 92, 96-98, 100, 101	V_{DD}	N/A		This pin must be connected to V_{DD} for normal operation.
21	H	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** This signal indicates the Horizontal blanking period of the input video data stream. The device inserts HDTV TRS based on the supplied HVF signals. Refer to Figure 4 for required timing of H relative to LUMA (DATA_IN[19:10]) and CHROMA (DATA_IN[9:0]).
22	V	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** This signal indicates the Vertical blanking period of the input video data streams. Refer to Figure 4 for required timing of V relative to LUMA (DATA_IN[19:10]) and CHROMA (DATA_IN[9:0]).

1.2 PIN DESCRIPTIONS (Continued)

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
23	F	Synchronous wrt PCLK_IN	Input	**Control Signal Input.** This signal indicates the ODD/EVEN field of the input video data streams. Refer to Figure 4 for required timing of F relative to LUMA (DATA_IN[19:10]) and CHROMA (DATA_IN[9:0]). When the input video format is progressive scan, F should remain low at all times.
26, 27, 28, 29, 30-34, 65, 66, 67, 71-75,	NC	N/A		**No Connect.** Do not connect these pins.
35	$\overline{TN}$	N/A	TEST	**Test pin.** Used for test purposes only. This pin must be connected to V_{DD} for normal operation.
36	$\overline{OEN}$	Non-synchronous	Input	**Control Signal Input.** Used to enable the DATA_OUT[19:0] output bus or set it to a high Z state. When $\overline{OEN}$ is low, the DATA_OUT[19:0] bus is enabled. When $\overline{OEN}$ is high, the DATA_OUT[19:0] bus is disabled and in a high Z state.
64, 63, 62, 61, 60, 57 56, 55, 54, 53, 52, 49, 48, 45, 44, 43, 42, 41, 40, 39	DATA_OUT[19:0]	Synchronous wrt PCLK_IN	Outputs	**Output Data Bus.** The device generates a 20 bit wide data stream running at 74.25 (or 74.25/1.001) MHz. DATA_OUT[19] is the MSB and DATA_OUT[0] is the LSB.
70	TEST	N/A	TEST	**Test Pin.** Used for test purposes only. This pin must be connected to GND for normal operation.
103,104,105, 106, 107, 108, 111, 112, 113, 114	DATA_IN [19:10] (LUMA channel)	Synchronous wrt PCLK_IN	Input	**Input Data Bus.** LUMA CHANNEL. DATA_IN [19] is the MSB of the LUMA input signal (pin 103). DATA_IN [10] is the LSB of the LUMA input signal (pin 114).
117, 118, 119, 120, 121, 122, 123, 124, 125, 126	DATA_IN [9:0] (CHROMA channel)	Synchronous wrt PCLK_IN	Input	**CHROMA Input Data Bus.** CHROMA CHANNEL DATA_IN [9] is the MSB of the CHROMA signal (pin 117). DATA_IN [0] is the LSB of the CHROMA signal (pin 126).

2. ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIUMUM RATINGS

PARAMETER	VALUE
Supply Voltage	-0.5V to +4.6V
Input Voltage Range (any input)	-0.5V < V_{IN} < 5.5V
Operating Temperature Range	0°C ≤ T_A ≤ 70°C
Storage Temperature Range	-40°C ≤ T_S ≤ 125°C
Lead Temperature (soldering 10 seconds)	260°C

2.2 DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.0 to 3.6V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Voltage	V_{DD}		3.0	3.3	3.6	V	
Supply Current	I_{DD}	f = 74.25MHz, T_A = 25°C	-	413	480	mA	
Input Logic LOW Voltage	V_{IL}	$I_{LEAKAGE}$ < 10µA	-	-	0.8	V	
Input Logic HIGH Voltage	V_{IH}	$I_{LEAKAGE}$ < 10µA	2.1	3.3	5.0	V	
Output Logic LOW Voltage	V_{OL}	V_{DD} = 3.0 to 3.6V, I_{OL}= 4mA	-	0.3	0.4	V	
Output Logic HIGH Voltage	V_{OH}	V_{DD} = 3.0 to 3.6V, I_{OH} = -4mA	2.6	-	-	V	

2.3 AC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.0 to 3.6V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Input Frequency	F_{HSCI}		-	74.25	80	MHz	Also supports 74.25/ 1.001MHz
Input Data Setup Time	t_{SU}		2.5	-	-	ns	50% levels
Input Data Hold Time	t_{IH}		1.5	-	-	ns	50% levels
Input Clock Duty Cycle			40	-	60	%	
Output Data Hold Time	t_{OH}	With 15pF load	2.0	-	-	ns	
Output Enable Time	t_{oen}	With 15pF load	-	-	8	ns	
Output Disable Time	t_{odis}	With 15pF load	-	-	10	ns	
Output Data Delay Time	t_{OD}	With 15pF load	-	-	10	ns	
Output Data Rise/Fall Time		With 15pF load	-	-	2.75	ns	20% to 80% levels

3. DETAILED DESCRIPTION

3.1 DATA INPUT AND OUTPUTS

Data enters and exits the device synchronous to the rising edge of PCLK_IN as shown in Figure 1.

3.2 INPUT BLANKER

Data words entering the GS1511 can be dynamically set to Luma and Chroma blanking levels if desired as shown in Figure 3. Blanking is applied to both the LUMA and CHROMA channels simultaneously.

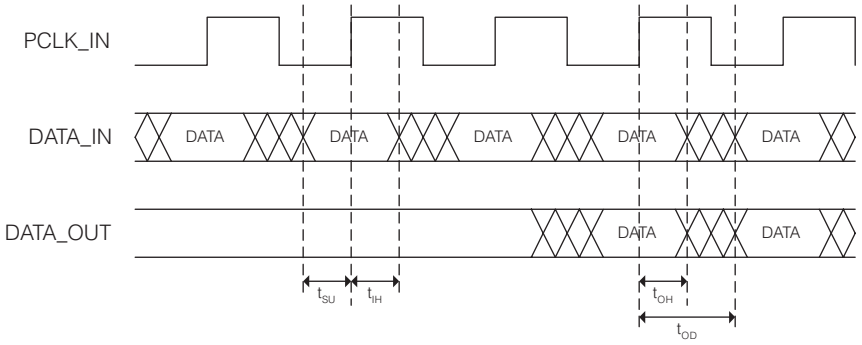


Fig. 1 Synchronous I/O Timing

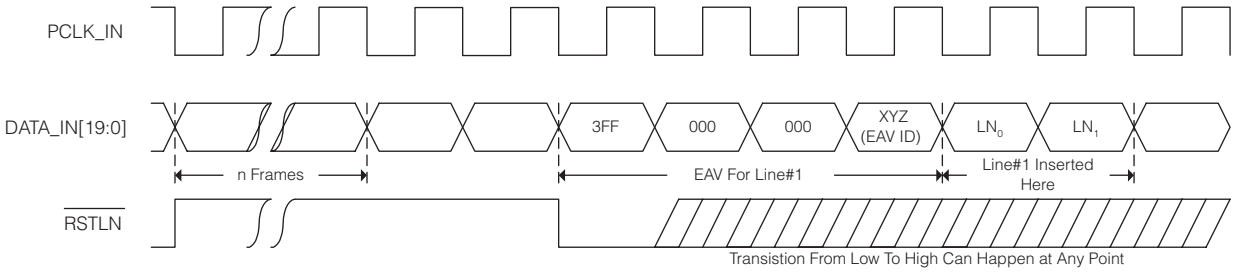


Fig. 2 $\overline{\text{RSTLN}}$ Timing

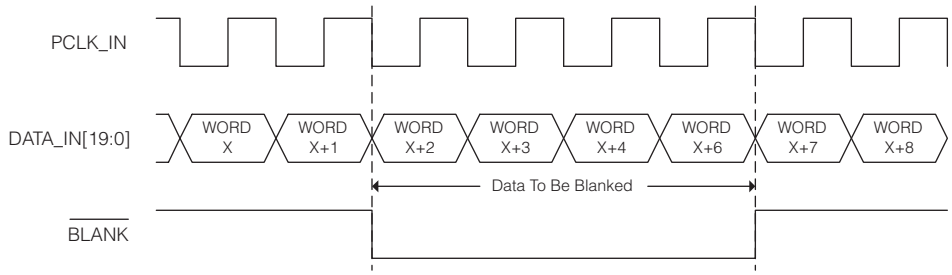


Fig. 3 Timing of Dynamic Data Blanking

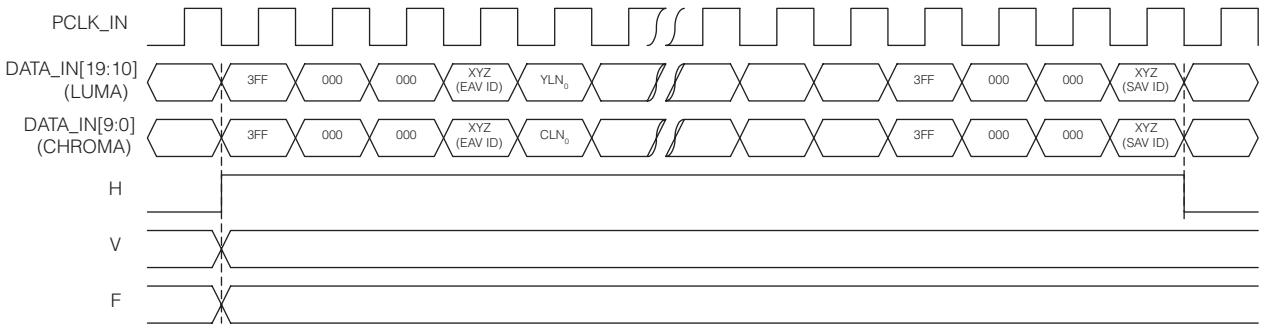


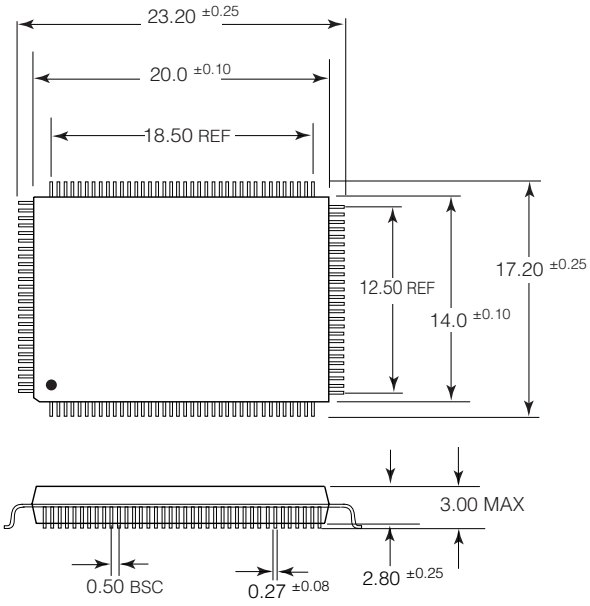
Fig. 4 HVF Input Timing

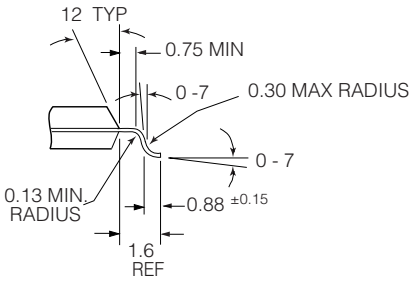
4. REFERENCES

Compliant with SMPTE 292M.

5. PACKAGE & ORDERING INFORMATION

5.1 PACKAGE DIMENSIONS





128 pin MQFP

All dimensions in millimetres

5.2 ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE	Pb-FREE AND GREEN
GS1511-CQR	128 pin MQFP	0°C to 70°C	No
GS1511-CQRE3	128 pin MQFP	0°C to 70°C	Yes

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES:
Added Pb-free and green information.

For latest product information, visit www.gennum.com

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