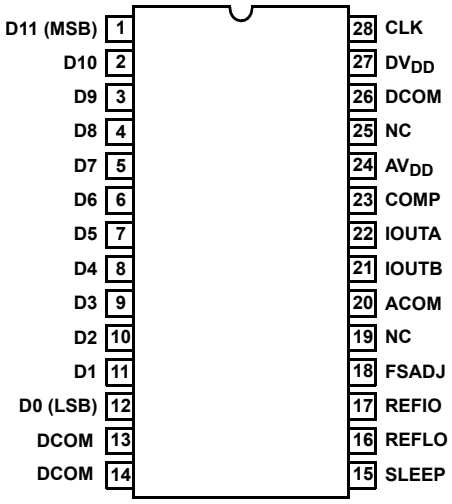
Data Sheet | December 23, 2013 | FN6720.2

12-Bit, +3.3V, 130MSPS, High Speed D/A Converter

The ISL76161 is a 12-bit, 130MSPS (Mega-Samples Per Second), CMOS, high speed, low power, D/A (digital to analog) converter, designed specifically for use in radar systems or high performance communication systems, such as base transceiver stations utilizing 2.5G or 3G cellular protocols.

Pinout

ISL76161
(28 LD TSSOP)
TOP VIEW



Features

- High Speed. 130MSPS
- Low Power . . . . . 103mW with 20mA Output at 130MSPS
- Adjustable Full Scale Output Current. . . . . 2mA to 20mA
- Excellent Spurious Free Dynamic Range (73dBc to Nyquist, f_S = 130MSPS, f_{OUT} = 10MHz)
- Automotive Qualified Component
- Extended Temperature Operation: -40°C to +105°C
- +3.3V Power Supply
- 3V LVCMOS Compatible Inputs
- UMTS Adjacent Channel Power = 70dB at 19.2MHz
- EDGE/GSM SFDR = 90dBc at 11MHz in 20MHz Window
- Pb-Free (RoHS Compliant)

Applications

- Automotive Radar Systems
  - 24GHz and 77GHz Radar for Adaptive Cruise Control
- Cellular Infrastructure - Single or Multi-Carrier: IS-136, IS-95, GSM, EDGE, CDMA2000, WCDMA, TDS-CDMA
- Wireless Communication Systems
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

Ordering Information

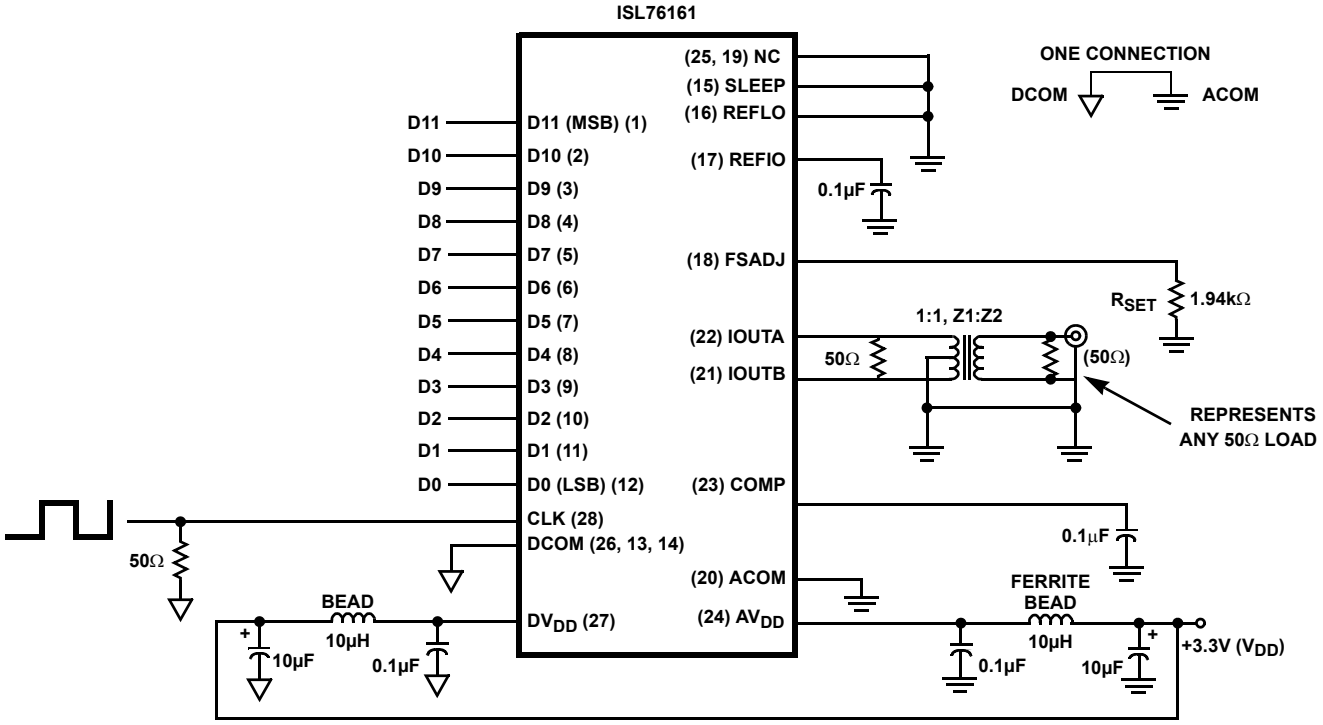
PART NUMBER (Note 1)	PART MARKING	CLOCK SPEED	TEMP. RANGE (°C)	PACKAGE (Pb-Free, Note 2)	PKG. DWG. #
ISL76161AVZ	ISL76161 AVZ	130MHz	-40 to +105	28 Ld TSSOP	M28.173
ISL76161AVZ-T*	ISL76161 AVZ	130MHz	-40 to +105	28 Ld TSSOP Tape and Reel	M28.173
ISL76161AVZ-TK*	ISL76161 AVZ	130MHz	-40 to +105	28 Ld TSSOP Tape and Reel	M28.173

*Please refer to TB347 for details on reel specifications.

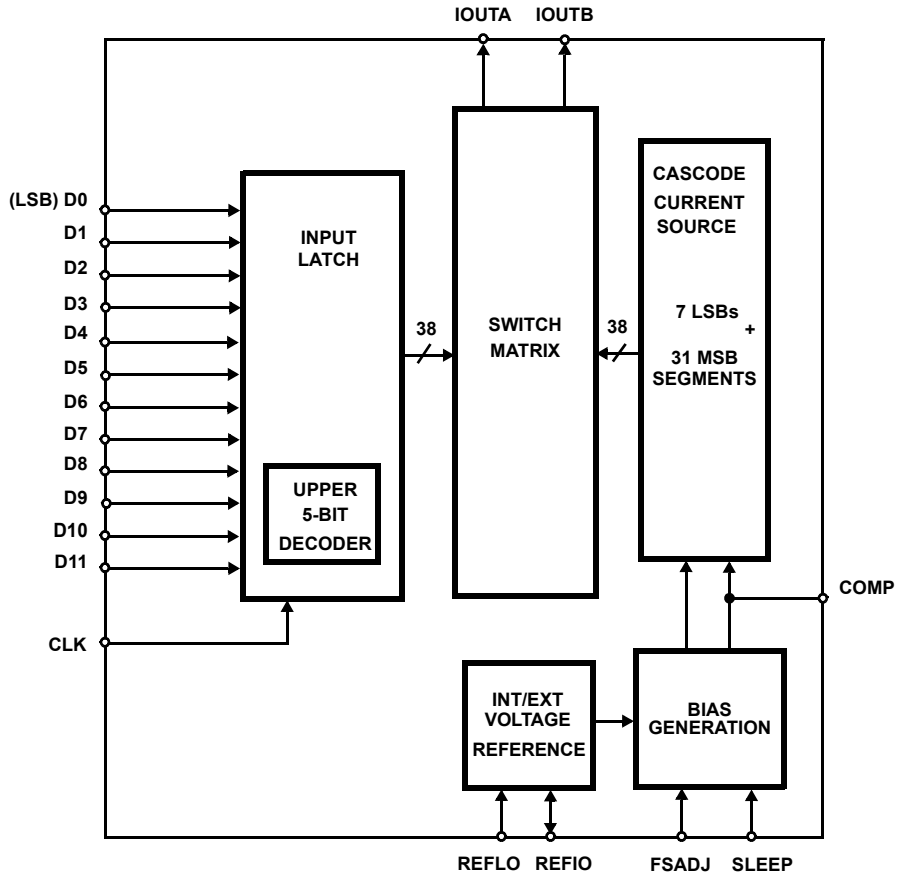
NOTES:

1. These parts have been qualified in accordance with AEC-Q100 rev F recommendations, some exceptions may apply. Request qualification plan for further details.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Typical Applications Circuit



Functional Block Diagram



Pin Descriptions

PIN NO.	PIN NAME	DESCRIPTION
1 through 12	D11 (MSB) through D0 (LSB)	Digital Data Bit 11, (Most Significant Bit) through Digital Data Bit 0, (Least Significant Bit).
15	SLEEP	Control Pin for Power-Down mode. Sleep Mode is active high; Connect to ground for Normal Mode. Sleep pin has internal 20µA active pull-down current.
16	REFLO	Connect to analog ground to enable internal 1.2V reference or connect to AV_{DD} to disable internal reference.
17	REFIO	Reference voltage input if internal reference is disabled. Reference voltage output if internal reference is enabled. Use 0.1µF cap to ground when internal reference is enabled.
18	FSADJ	Full Scale Current Adjust. Use a resistor to ground to adjust full scale output current. Full Scale Output Current = 32 x V_{FSADJ}/R_{SET}.
19, 25	NC	No Connect. These should be grounded, but can be left disconnected.
21	IOUTB	The complementary current output of the device. Full scale output current is achieved when all input bits are set to binary 0.
22	IOUTA	Current output of the device. Full scale output current is achieved when all input bits are set to binary 1.
23	COMP	Connect 0.1µF capacitor to ACOM.
24	AV_{DD}	Analog Supply (+3.0V to +3.6V).
20	ACOM	Connect to Analog Ground.
13, 14, 26	DCOM	Connect to Digital Ground.
27	DV_{DD}	Digital Supply (+3.0V to +3.6V).
28	CLK	Clock Input.

Absolute Maximum Ratings

Digital Supply Voltage DV_{DD} to DCOM . . . . . +4.0V
Analog Supply Voltage AV_{DD} to ACOM. . . . . +4.0V
Grounds, ACOM TO DCOM . . . . . -0.3V to +0.3V
Digital Input Voltages (D9-D0, CLK, SLEEP). . . . . DV_{DD} + 0.3V
Reference Input Voltage Range. . . . . AV_{DD} + 0.3V
Analog Output Current (I_{OUT}) 24mA

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA}(°C/W)
TSSOP Package	84

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . .-40°C to +105°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

AV_{DD} = DV_{DD} = +3.3V, V_{REF} = Internal 1.2V, IOUTFS = 20mA, T_A = +25°C for All Typical Values; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	TEST CONDITIONS	T_A = -40°C TO +105°C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		12	-	-	Bits
Integral Linearity Error, INL	“Best Fit” Straight Line (Note 9)	-1.25	±0.5	+1.25	LSB
Differential Linearity Error, DNL	(Note 9)	-1	±0.5	+1	LSB
Offset Error, I_{OS}	IOUTA (Note 9)	-0.006	-	+0.006	% FSR
Offset Drift Coefficient	(Note 9)	-	0.1	-	ppm FSR/°C
Full Scale Gain Error, FSE	With External Reference (Notes 4, 9)	-	±0.5	-	% FSR
	With Internal Reference (Notes 4, 9)	-3	±0.5	+3	% FSR
Full Scale Gain Drift	With External Reference (Note 9)	-	±50	-	ppm FSR/°C
	With Internal Reference (Note 9)	-	±100	-	ppm FSR/°C
Full Scale Output Current, I_{FS}	R_{SET} = 1.94kΩ (Maximum FS output)	-	20	-	mA
	R_{SET} = 20kΩ (Minimum FS output)	-	2	-	mA
Output Voltage Compliance - High Voltage Limit		-	1.25	-	V
Output Voltage Compliance - Low Voltage Limit		-	-1.0	-	V
DYNAMIC CHARACTERISTICS					
Maximum Clock Rate, f_{CLK}		130	150	-	MHz
Output Rise Time	Full Scale Step	-	1.5	-	ns
Output Fall Time	Full Scale Step	-	1.5	-	ns
Output Capacitance		-	10	-	pF
Output Noise	IOUTFS = 20mA	-	50	-	pA/$\sqrt{Hz}$
	IOUTFS = 2mA	-	30	-	pA/$\sqrt{Hz}$

Electrical Specifications $AV_{DD} = DV_{DD} = +3.3V$, V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = +25°C$ for All Typical Values; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	TEST CONDITIONS	T_A = -40°C TO +105°C			UNITS
		MIN	TYP	MAX	
AC CHARACTERISTICS (Using Figure 12 with $R_{DIFF} = 100\Omega$, $R_{LOAD} = R_A = R_B = 50\Omega$, Full Scale Output = -2.0dBm)					
Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 130MSPS, f_{OUT} = 20.2MHz, 20MHz Span (Notes 6, 8)	-	85	-	dBc
Spurious Free Dynamic Range, SFDR to Nyquist ($f_{CLK}/2$)	f_{CLK} = 130MSPS, f_{OUT} = 50.5MHz (Notes 6, 8)	-	57	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 40.4MHz (Notes 6, 8)	-	62	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 20.2MHz (Notes 6, 9)	-	69	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 10.1MHz (Notes 6, 8)	-	73	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 5.05MHz, T = +25°C (Notes 6, 8)	70	77	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 5.05MHz, T = -40°C to +105°C (Notes 6, 8)	67	-	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 40.4MHz (Notes 6, 8)	-	60	-	dBc
	f_{CLK} = 80MSPS, f_{OUT} = 30.3MHz (Notes 6, 8)	-	63	-	dBc
	f_{CLK} = 80MSPS, f_{OUT} = 20.2MHz (Notes 6, 8)	-	69	-	dBc
	f_{CLK} = 80MSPS, f_{OUT} = 10.1MHz (Notes 6, 8, 10)	-	70	-	dBc
	f_{CLK} = 80MSPS, f_{OUT} = 5.05MHz (Notes 6, 8)	-	76	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 20.2MHz (Notes 6, 8)	-	68	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 10.1MHz (Notes 6, 8)	-	73	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.05MHz (Notes 6, 8)	-	77	-	dBc
Spurious Free Dynamic Range, SFDR in a Window with Eight Tones	f_{CLK} = 130MSPS, f_{OUT} = 17.5MHz to 27.9MHz, 1.3MHz Spacing, 35MHz Span (Notes 6, 8)	-	68	-	dBc
	f_{CLK} = 80MSPS, f_{OUT} = 10.8MHz to 17.2MHz, 811kHz Spacing, 15MHz Span (Notes 6, 8)	-	75	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 6.7MHz to 10.8MHz, 490kHz Spacing, 10MHz Span (Notes 6, 8)	-	77	-	dBc
Spurious Free Dynamic Range, SFDR in a Window with EDGE or GSM	f_{CLK} = 78MSPS, f_{OUT} = 11MHz, in a 20MHz Window, RBW = 30kHz (Notes 6, 8, 10)	-	90	-	dBc
Adjacent Channel Power Ratio, ACPR with UMTS	f_{CLK} = 76.8MSPS, f_{OUT} = 19.2MHz, RBW = 30kHz (Notes 6, 8, 10)	-	70	-	dB
VOLTAGE REFERENCE					
Internal Reference Voltage, V_{FSADJ}	Pin 18 Voltage with Internal Reference	1.2	1.23	1.3	V
Internal Reference Voltage Drift		-	±40	-	ppm/°C
Internal Reference Output Current Sink/Source Capability	Reference is not intended to be externally loaded	-	0	-	µA
Reference Input Impedance		-	1	-	MΩ
Reference Input Multiplying Bandwidth	(Note 8)	-	1.0	-	MHz
DIGITAL INPUTS D11-D0, CLK					
Input Logic High Voltage with 3.3V Supply, V_{IH}	(Note 5)	0.7 * DV_{DD}	-	-	V
Input Logic Low Voltage with 3.3V Supply, V_{IL}	(Note 5)	-	-	0.3 * DV_{DD}	V
Sleep Input Current, I_{IH}		-25	-	+25	µA
Input Logic Current, $I_{IH, IL}$		-20	-	+20	µA
Clock Input Current, $I_{IH, IL}$		-10	-	+10	µA

Electrical Specifications AV_{DD} = DV_{DD} = +3.3V, V_{REF} = Internal 1.2V, IOUTFS = 20mA, T_A = +25°C for All Typical Values; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	TEST CONDITIONS	T_A = -40°C TO +105°C			UNITS
		MIN	TYP	MAX	
Digital Input Capacitance, C_{IN}		-	5	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 13	-	1.5	-	ns
Data Hold Time, t_{HLD}	See Figure 13	-	1.5	-	ns
Propagation Delay Time, t_{PD}	See Figure 13	-	1	-	Clock Period
Minimum CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 13, (Note 11)	-	2	-	ns
POWER SUPPLY CHARACTERISTICS (Note 5)					
AV_{DD} Power Supply	(Note 9)	2.7	3.3	3.6	V
DV_{DD} Power Supply	(Note 9)	2.7	3.3	3.6	V
Analog Supply Current (I_{AVDD})	3.3V, IOUTFS = 20mA	-	27.5	28.5	mA
	3.3V, IOUTFS = 2mA	-	10	-	mA
Digital Supply Current (I_{DVDD})	3.3V (Note 7)	-	3.7	5	mA
Supply Current (I_{AVDD}) Sleep Mode	3.3V, IOUTFS = Don't Care	-	1.5	-	mA
Power Dissipation	3.3V, IOUTFS = 20mA (Note 7)	-	103	111	mW
	3.3V, IOUTFS = 20mA	-	110	120	mW
	3.3V, IOUTFS = 2mA (Note 7)	-	45	-	mW
Power Supply Rejection	Single Supply (Note 8)	-0.125	-	+0.125	%FSR/V

NOTES:

4. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 625µA). Ideally, the ratio should be 32.
5. Power supply current measurements are performed with all digital inputs at either DV_{DD} or DCOM
6. Spectral measurements made with differential transformer coupled output and no external filtering. For multitone testing, the same pattern was used at different clock rates, producing different output frequencies but at the same ratio to the clock rate.
7. Measured with the clock at 130MSPS and the output frequency at 5MHz.
8. See "Definition of Specifications" on page 9.
9. Recommended operation is from 3.0V to 3.6V. Operation below 3.0V is possible with some degradation in spectral performance. Reduction in analog output current may be necessary to maintain spectral performance.
10. See "Typical Performance" plots on page 7.
11. Tested in production with a clock pulse width of 50% duty cycle.

Typical Performance (+3.3V Supply, Using Figure 11 with R_{DIFF} = 100Ω and R_{LOAD} = 50Ω)

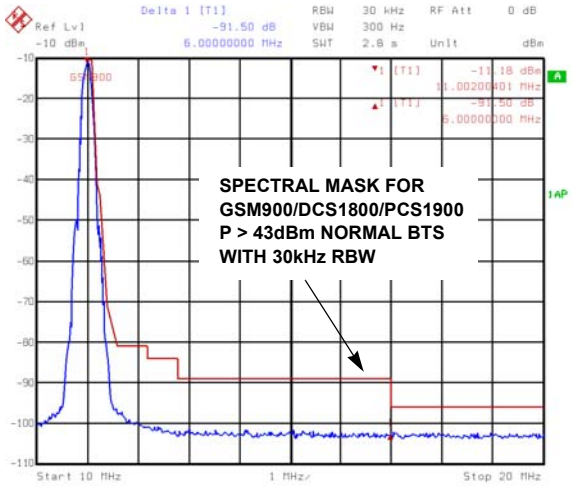


FIGURE 1. EDGE AT 11MHz, 78MSPS CLOCK (91+dBc @ Δf = +6MHz)

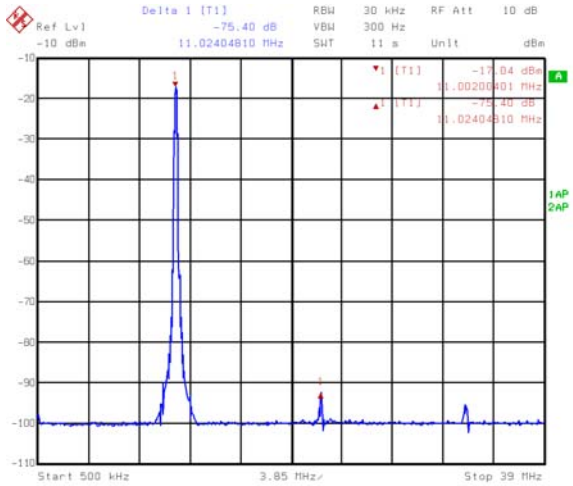


FIGURE 2. EDGE AT 11MHz, 78MSPS CLOCK (75dBc - NYQUIST, 6dB PAD)

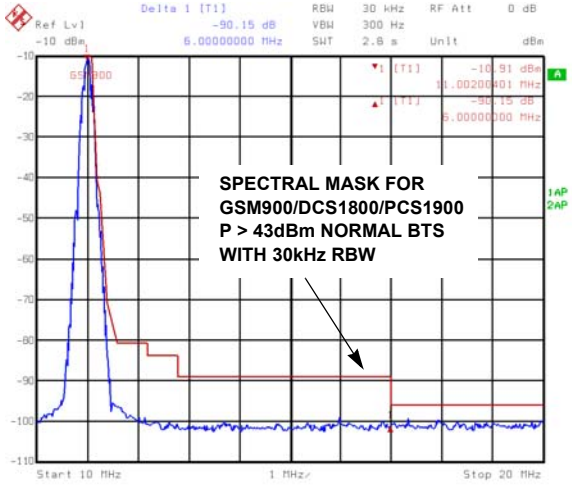


FIGURE 3. GSM AT 11MHz, 78MSPS CLOCK (90+dBc @ Δf = +6MHz, 3dB PAD)

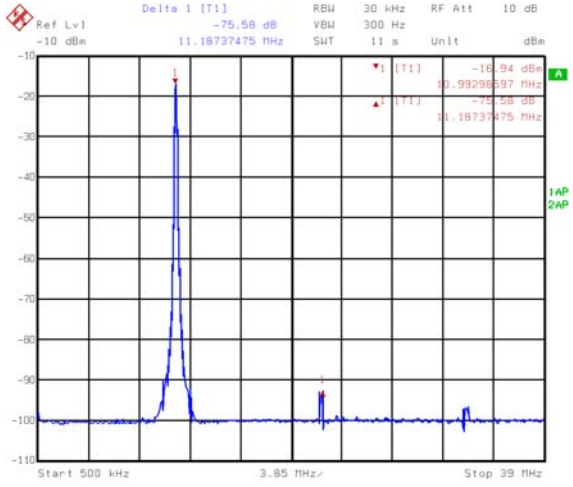


FIGURE 4. GSM AT 11MHz, 78MSPS CLOCK (75dBc - NYQUIST, 9dB PAD)

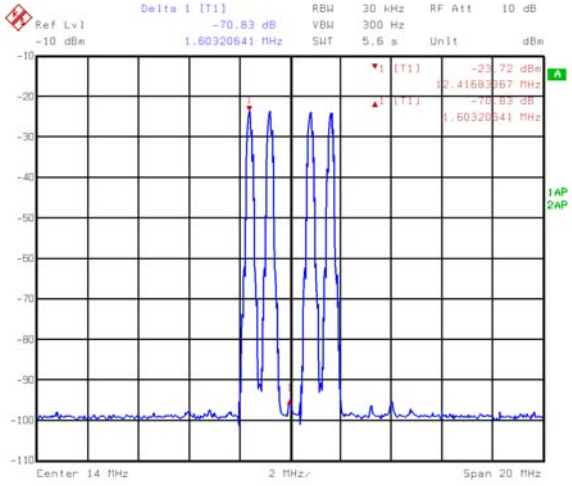


FIGURE 5. FOUR EDGE CARRIERS AT 12.4MHz TO 15.6MHz, 800kHz SPACING, 78MSPS (71dBc - 20MHz WINDOW)

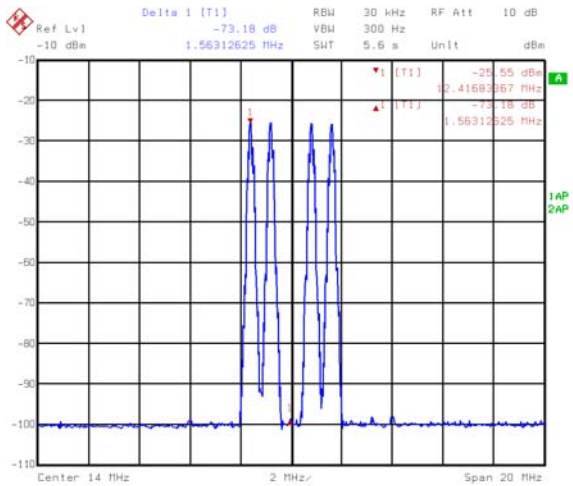


FIGURE 6. FOUR GSM CARRIERS AT 12.4MHz TO 15.6MHz, 78MSPS (73dBc - 20MHz WINDOW, 6dB PAD)

Typical Performance (+3.3V Supply, Using Figure 11 with R_{DIFF} = 100Ω and R_{LOAD} = 50Ω) (Continued)

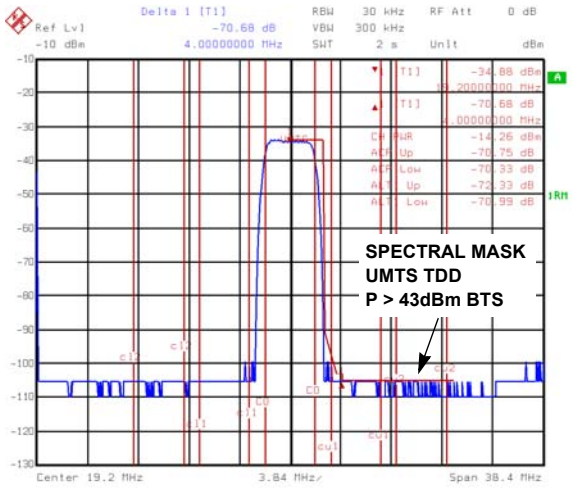


FIGURE 7. UMTS AT 19.2MHz, 76.8MSPS (70dB 1stACPR, 70dB 2ndACPR)

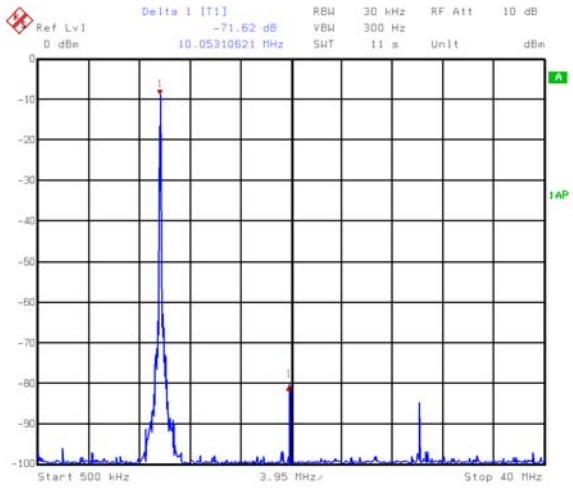


FIGURE 8. ONE TONE AT 10.1MHz, 80MSPS CLOCK (71dBc - NYQUIST, 6dB PAD)

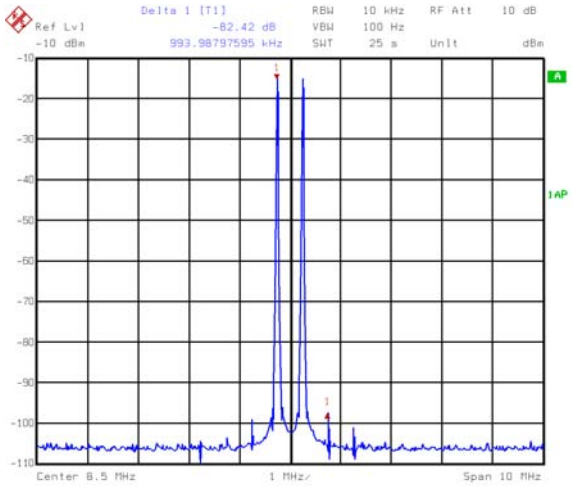


FIGURE 9. TWO TONES (CkHzF = 6) AT 8.5MHz, 50MSPS CLOCK, 500kHz SPACING (82dBc - 10MHz WINDOW, 6dB PAD)

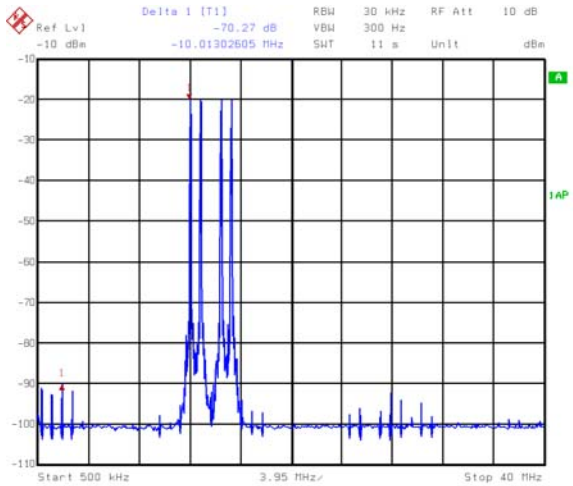


FIGURE 10. FOUR TONES (CF = 8.1) AT 14MHz, 80MSPS CLOCK, 800kHz SPACING (70dBc - NYQUIST, 6dB PAD)

Definition of Specifications

Adjacent Channel Power Ratio, ACPR, is the ratio of the average power in the adjacent frequency channel (or offset) to the average power in the transmitted frequency channel.

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally, the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

EDGE, Enhanced Data for Global Evolution, a TDMA standard for cellular applications which uses 200kHz BW, 8-PSK modulated carriers.

Full Scale Gain Drift, is measured by setting the data inputs to be all logic high (all 1s) and measuring the output voltage through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (full scale range) per °C.

Full Scale Gain Error, is the error from an ideal ratio of 32 between the output current and the full scale adjust current (through R_{SET}).

GSM, Global System for Mobile Communication, a TDMA standard for cellular applications which uses 200kHz BW, GMSK modulated carriers.

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Internal Reference Voltage Drift, is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm per °C.

Offset Drift, is measured by setting the data inputs to all logic low (all 0s) and measuring the output voltage at IOUTA through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (full scale range) per °C.

Offset Error, is measured by setting the data inputs to all logic low (all 0s) and measuring the output voltage of IOUTA through a known resistance. Offset error is defined as the maximum *deviation* of the IOUTA output current from a value of 0mA.

Output Voltage Compliance Range, is the voltage limit imposed on the output. The output impedance should be chosen such that the voltage developed does not violate the compliance range.

Power Supply Rejection, is measured using a single power supply. The nominal supply voltage is varied ±10% and the change in the DAC full scale output is noted.

Reference Input Multiplying Bandwidth, is defined as the 3dB bandwidth of the voltage reference input. It is measured by using a sinusoidal waveform as the external reference with the digital inputs set to all 1s. The frequency is increased until the amplitude of the output waveform is 0.707 (-3dB) of its original value.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from the fundamental signal to the largest harmonically or non-harmonically related spur within the specified frequency window.

Total Harmonic Distortion, THD, is the ratio of the RMS value of the fundamental output signal to the RMS sum of the first five harmonic components.

UMTS, **Universal Mobile Telecommunications System,** a W-CDMA standard for cellular applications which uses 3.84MHz modulated carriers.

Detailed Description

The ISL76161 is a 12-bit, current out, CMOS, digital to analog converter. The maximum update rate is at least 130MSPS and can be powered by a single power supply in the recommended range of +3.0V to +3.6V. Operation with clock rates higher than 130MSPS is possible; please contact the factory for more information. It consumes less than 120mW of power when using a +3.3V supply, the maximum 20mA of output current, and the data switching at 130MSPS. The architecture is based on a segmented current source arrangement that reduces glitch by reducing the amount of current switching at any one time. In previous architectures that contained all binary weighted current sources or a binary weighted resistor ladder, the converter may have had a substantially larger amount of current turning on and off at certain, worst-case transition points, such as midscale and quarter scale transitions. By greatly reducing the amount of current switching at these major transitions, the overall glitch of the converter is dramatically reduced, improving settling time, transient problems, and accuracy.

Digital Inputs and Termination

The ISL76161 digital inputs are guaranteed to 3V LVCMOS levels. The internal register is updated on the rising edge of the clock. To minimize reflections, proper transmission line termination should be implemented. If the lines driving the clock and the digital inputs are long 50Ω lines, then proper transmission line termination techniques should be used. Termination is not likely needed as long as the digital waveform source is within a few inches of the DAC. For digital drivers with very high speed edge rates, it is recommended that the user consider series resistors (50Ω to 200Ω) immediately prior to the DAC's inputs in order to reduce the amount of noise.

Power Supply

Separate digital and analog power supplies are recommended. The allowable supply range is +2.7V to +3.6V. The

recommended supply range is +3.0 to 3.6V (nominally +3.3V) to maintain optimum SFDR. However, operation down to +2.7V is possible with some degradation in SFDR. Reducing the analog output current can help the SFDR at +2.7V. The SFDR values stated in the "Electrical Specifications" table on page 4 were obtained with a +3.3V supply.

Ground Planes

Separate digital and analog ground planes should be used. All of the digital functions of the device and their corresponding components should be located over the digital ground plane and terminated to the digital ground plane. The same is true for the analog components and the analog ground plane.

Noise Reduction

To minimize power supply noise, 0.1µF capacitors should be placed as close as possible to the converter's power supply pins, AV_{DD} and DV_{DD}. Also, the layout should be designed using separate digital and analog ground planes and these capacitors should be terminated to the digital ground for DV_{DD} and to the analog ground for AV_{DD}. Additional filtering of the power supplies on the board is recommended.

Voltage Reference

The internal voltage reference of the device has a nominal value of +1.23V with a ±40ppm/°C drift coefficient over the full temperature range of the converter. It is recommended that a 0.1µF capacitor be placed as close as possible to the REFIO pin, connected to the analog ground. The REFLO pin (16) selects the reference. The internal reference can be selected if pin 16 is tied low (ground). If an external reference is desired, then pin 16 should be tied high (the analog supply voltage) and the external reference driven into REFIO, pin 17. The full scale output current of the converter is a function of the voltage reference used and the value of R_{SET}. I_{OUT} should be within the 2mA to 20mA range, though operation below 2mA is possible, with performance degradation.

If the internal reference is used, V_{FSADJ} will equal approximately 1.2V (pin 18). If an external reference is used, V_{FSADJ} will equal the external reference. The calculation for I_{OUT} (Full Scale) is:

$$I_{OUT}(\text{Full Scale}) = (V_{FSADJ}/R_{SET}) \times 32 \quad \text{(EQ. 1)}$$

If the full scale output current is set to approximately 20mA by using the internal voltage reference (1.2V) and a 1.94kΩ R_{SET} resistor, then the input coding to output current will resemble those shown in Table 1.

TABLE 1. INPUT CODING vs. OUTPUT CURRENT WITH INTERNAL REFERENCE AND R_{SET} = 1.91kΩ

INPUT CODE (D11-D0)	IOUTA (mA)	IOUTB (mA)
11 11111 11111	20	0
10 00000 00000	10	10
00 00000 00000	0	20

Analog Output

IOUTA and IOUTB are complementary current outputs. The sum of the two currents is always equal to the full scale output current minus one LSB. If single ended use is desired, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be either grounded or equally terminated. The voltage developed at the output must not violate the nominal output voltage compliance range of -1.0V to 1.25V. R_{OUT} (the impedance loading each current output) should be chosen so that the desired output voltage is produced in conjunction with the output full scale current. If a known line impedance is to be driven, then the output load resistor should be chosen to match this impedance. The output voltage equation is:

$$V_{OUT} = I_{OUT} \times R_{OUT} \quad \text{(EQ. 2)}$$

The most effective method for reducing the power consumption is to reduce the analog output current, which dominates the supply current. The maximum recommended output current is 20mA.

Differential Output

IOUTA and IOUTB can be used in a differential-to-single-ended arrangement to achieve better harmonic rejection. With R_{DIFF} = 50Ω and R_{LOAD} = 50Ω, the circuit in Figure 11 will provide a 500mV_{P-P} (-2dBm) signal at the output of the transformer if the full scale output current of the DAC is set to 20mA (used for the "Electrical Specifications" table on page 4). Values of R_{DIFF} = 100Ω and R_{LOAD} = 50Ω were used for the "Typical Performance" curves on page 7. The center tap in Figure 11 must be grounded.

In the circuit in Figure 12, the user is left with the option to ground or float the center tap. The DC voltage that will exist at either IOUTA or IOUTB if the center tap is floating is $IOUT_{DC}$ x 2 x (R_A//R_B) V because R_{DIFF} is DC shorted by the transformer, and the DC currents from each output add constructively. If the center tap is grounded, the DC voltage is 0V. Recommended values for the circuit in Figure 12 are R_A = R_B = 50Ω, R_{DIFF} = 100Ω, assuming R_{LOAD} = 50Ω. The performance of Figure 11 and Figure 12 is basically the same, however leaving the center tap of Figure 12 floating allows the circuit to find a more balanced virtual ground, theoretically improving the even order harmonic rejection, but likely reducing the signal swing available due to the output voltage compliance range limitations.

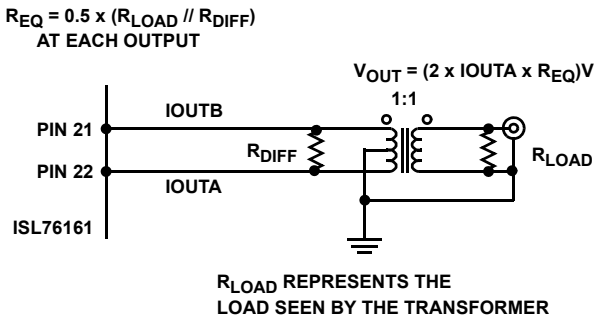


FIGURE 11. OUTPUT LOADING FOR DATASHEET MEASUREMENTS

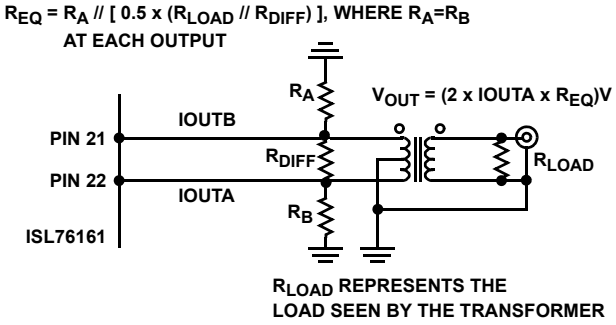


FIGURE 12. ALTERNATIVE OUTPUT LOADING

Timing Diagram

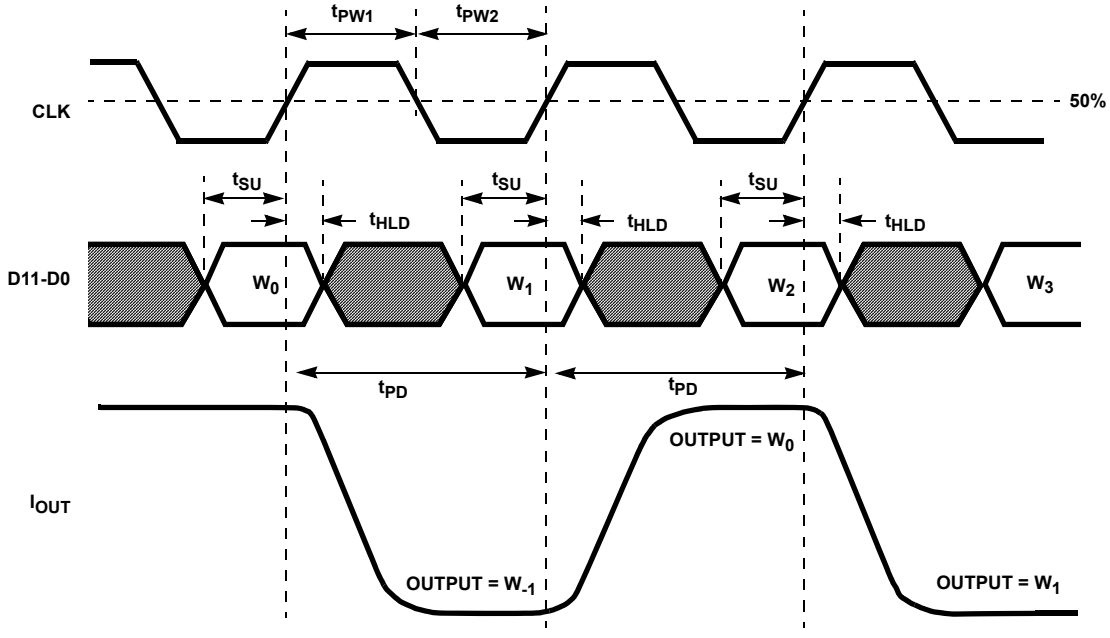
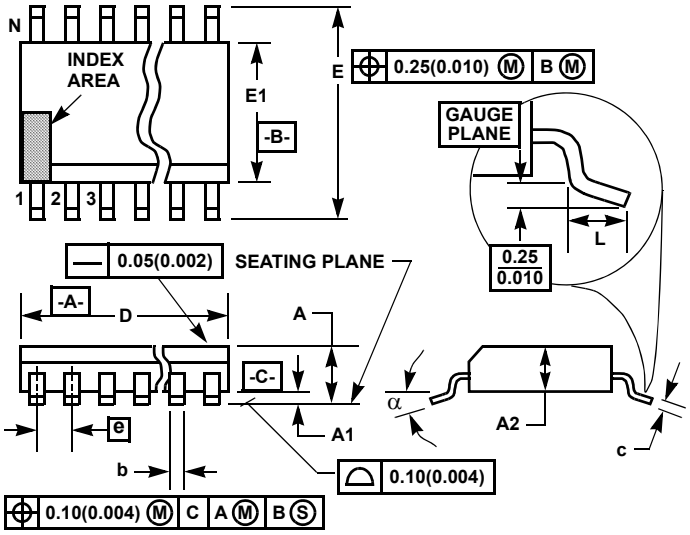


FIGURE 13. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Propagation Delay

The converter requires two clock rising edges for data to be represented at the output. Each rising edge of the clock captures the present data word and outputs the previous data. The propagation delay is therefore 1/CLK, plus <2ns of settling. See Figure 13.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AE, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M28.173

28 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.378	0.386	9.60	9.80	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 6/98