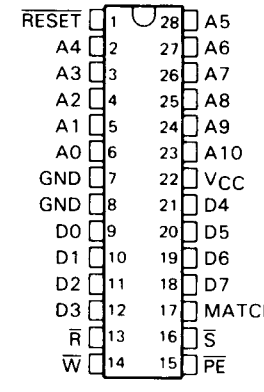
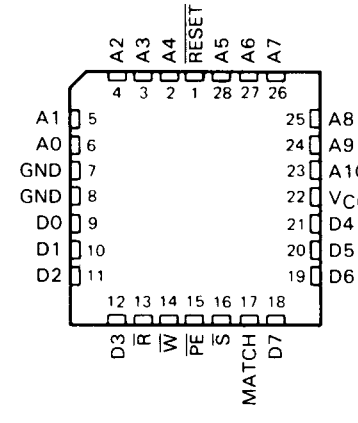
D3156, DECEMBER 1988 – REVISED MARCH 1990

- **Fast Address to Match Delay 25 or 25 ns Max**
- **Common I/O with Read Feature**
- **On-Chip Address/Data Comparator**
- **On-Chip Parity Generator and Checking**
- **Parity Error Output, Force Parity Error Input**
- **Easily Expandable**
- **Choice of Open-Drain or Totem-Pole MATCH Output**
- **EPIC™ (Enhanced Performance Implanted CMOS) 1-μm Process**
- **Fully TTL-Compatible**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The 'ACT2152A and 'ACT2154A cache address comparators consist of a high-speed 2K × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. They are fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. These cache address comparators are easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with these devices. The 'ACT2152A has a totem-pole MATCH output while the 'ACT2154A has an open-drain MATCH output for easy AND-tying.

If $\overline{S}$ is low and $\overline{W}$ and $\overline{R}$ are high, the cache address comparator compares the contents of the memory location addressed by A0-A10 with the data D0-D7 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level output on $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated odd parity are written in the 9-bit memory location addressed by A0-A10. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

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A read mode is provided with the 'ACT2152 and 'ACT2154, which allows the contents of RAM to be read at the D0-D7 pins. The read mode is selected when $\overline{R}$ and $\overline{S}$ are low, and $\overline{W}$ is high.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 2K × 9 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high after reset for every addressed memory location, indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit must be tied high regardless of the address width.

These cache address comparators operate from a single +5-V supply and are offered in 28-pin 600-mil ceramic side-brazed, plastic dual-in-line, or PLCC packages.

The 'ACT2152 and 'ACT2154 are characterized for operation from 0°C to 70°C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A10] = D0-D7 + parity,
or: $\overline{RESET}$ = V_{IL},
or: $\overline{S}$ = V_{IH},
or: $\overline{W}$ = V_{IL}

MATCH = V_{OL} if: [A0-A10] ≠ D0-D7 + parity,
with $\overline{RESET}$ = V_{IH},
$\overline{S}$ = V_{IL}, and $\overline{W}$ = V_{IH}

FUNCTION TABLE

INPUTS				OUTPUTS		I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{RESET}$	MATCH	$\overline{PE}$	D0-D7	
H	L	L	H	L	H	Output	Read
H	H	L	H	L	L	Input	Parity error
				L	H		Not equal
				H	L		Undefined error
				H	H		Equal
L	X	L	H	H	IN	Input	Write
X	X	H	H	H	H	Hi-Z	Device disabled
X	X	X	L	H	†	†	Memory reset

†The state of these pins is dependent on inputs $\overline{W}$, $\overline{R}$, and $\overline{S}$.

for complete data sheet

The complete version of this data sheet and application information can be found in the *Cache Memory Management Data Book*, Literature #SCAD002. To obtain a copy of this data book, contact your local TI sales representative or call the TI Customer Response Center at 1-800-223-3200.