

**CY74FCT163244**  
**CY74FCT163H244**  
**CY74FCT163LD244**  
**CY74FCT163LDH244**

## 16 Bit Buffers/Line Drivers

### Features

- Low power, pin-compatible replacement for LCX, LPT, LVC, LVCH & LVT families
- 5V tolerant inputs and outputs\*
- 6 mA & 24 mA balanced drive outputs
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for reduced noise
- FCT-C speed at 4.1 ns
- Latch-up performance exceeds JEDEC standard no. 17
- Typical output skew < 250 ps
- Industrial temperature range of -40°C to +85°C
- TSSOP (19.6-mil pitch) or SSOP (25-mil pitch)
- Typical  $V_{olp}$  (ground bounce) performance exceeds Mil Std 883D
- $V_{CC} = 2.7V$  to 3.6V
- ESD (HBM) > 2000V

*CY74FCT163H244, CY74FCT163LDH244*

- Bus hold on data inputs
- Eliminates the need for external pull-up or pull-down resistors
- \*Devices with bus hold are not recommended for translating rail-to-rail CMOS signals to 3.3V logic levels

*CY74FCT163LD244*

- Lite Drive™ option for low noise applications
- FCT-A speed at 4.8 ns

- $V_{CC} = 3.0$  to 3.5V
- ESD (HBM) > 1100V

### Functional Description

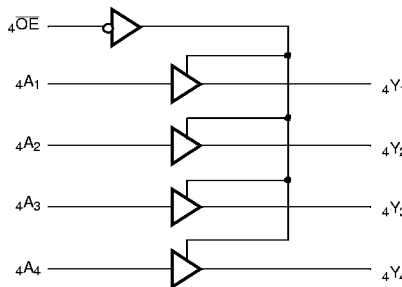
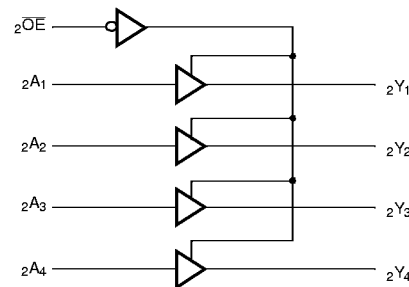
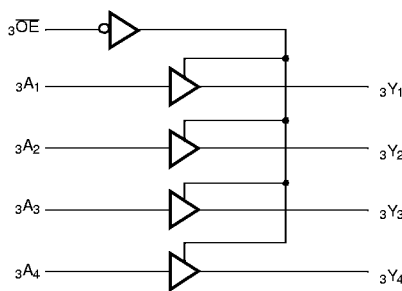
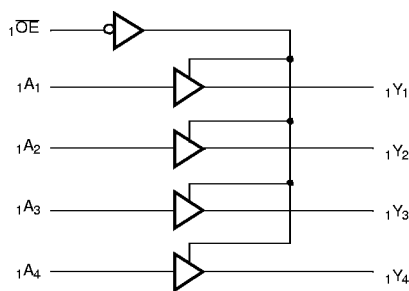
These 16-bit buffers/line drivers are designed for use in memory driver, clock driver, or other bus interface applications, where high-speed and low power are required. The three-state controls are designed to allow 4-bit, 8-bit or combined 16-bit operation. Flow-through pinout and small shrink packaging simplifies board layout.

The CY74FCT163244 has 24-mA balanced output drivers with current limiting resistors in the outputs. The CY74FCT163LD244 has 6-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce.

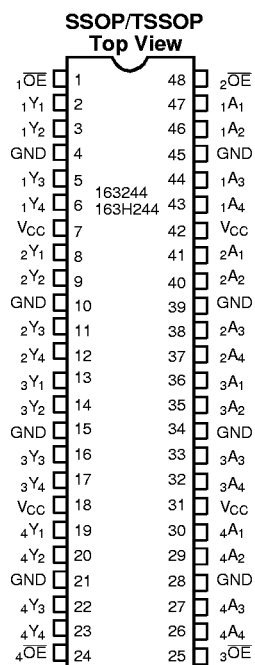
The CY74FCT163H244 and CY74FCT163LDH244 have "bus hold" on the data inputs, which retain the last state of the input whenever the source driving the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

The CY74FCT163244 and the CY74FCT163LD244 are designed with inputs and outputs capable of being driven by 5.0V buses, allowing them to be used in mixed voltage systems as translators. The outputs are also designed with a power off disable feature enabling them to be used in applications requiring live insertion.

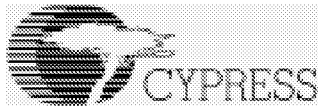
### Logic Block Diagrams CY74FCT163244, CY74FCT163H244 CY74FCT163LD244, CY74FCT163LDH244



### Pin Configuration



Lite Drive is a trademark of Cypress Semiconductor Corporation.



## Pin Description

Name	Description
OE	Three-State Output Enable Inputs (Active LOW)
A	Data Inputs <sup>[1]</sup>
Y	Three-State Outputs

## Function Table<sup>[2]</sup>

Inputs		Outputs
OE	A	Y
L	L	L
L	H	H
H	X	Z

## Maximum Ratings<sup>[3,4]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	-55°C to +125°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage Range.....	0.5V to +4.6V
DC Input Voltage.....	-0.5V to +7.0V
DC Output Voltage.....	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin).....	-60 to +120 mA
Power Dissipation.....	1.0W

## Operating Range

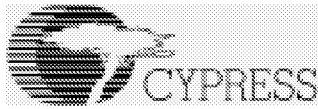
Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	2.7V to 3.6V

## Electrical Characteristics for Non Bus Hold Devices Over the Operating Range V<sub>CC</sub>=2.7V to 3.6V

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	All Inputs	2.0		5.5	V
V <sub>IL</sub>	Input LOW Voltage				0.8	V
V <sub>H</sub>	Input Hysteresis <sup>[6]</sup>			100		mV
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>I</sub> =5.5			±1	µA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>I</sub> =GND			±1	µA
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =5.5V			±1	µA
I <sub>OZL</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND			±1	µA
I <sub>OS</sub>	Short Circuit Current <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND	-60	-135	-240	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> ≤4.5V			±100	µA
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>IN</sub> ≤0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V, V <sub>CC</sub> =Max.		0.1	10	µA
ΔI <sub>CC</sub>	Quiescent Power Supply Current (TTL inputs HIGH)	V <sub>IN</sub> =V <sub>CC</sub> -0.6V <sup>[8]</sup> , V <sub>CC</sub> =Max.		2.0	30	µA

### Notes:

- On the CY74FCT163H244 and the CY74FCT163LDH244 these pins have "bus hold."
- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- With the exception of inputs with bus hold, unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- Typical values are at V<sub>CC</sub>=3.3V, T<sub>A</sub> = +25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- Per TTL driven input; all other inputs at V<sub>CC</sub> or GND.



**Electrical Characteristics For Bus Hold Devices** Over the Operating Range  $V_{CC}=2.7V$  to  $3.6V$

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage	All Inputs	2.0		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage				0.8	V
$V_H$	Input Hysteresis <sup>[6]</sup>			100		mV
$V_{IK}$	Input Clamp Diode Voltage	$V_{CC}=\text{Min.}, I_{IN}=-18\text{ mA}$		-0.7	-1.2	V
$I_{IH}$	Input HIGH Current	$V_{CC}=\text{Max.}, V_I=V_{CC}$			$\pm 100$	$\mu\text{A}$
$I_{IL}$	Input LOW Current				$\pm 100$	$\mu\text{A}$
$I_{BBH}$ $I_{BBL}$	Bus Hold Sustain Current on Bus Hold Input <sup>[9]</sup>	$V_{CC}=\text{Min.}$ $V_I=2.0V$	-50			$\mu\text{A}$
		$V_I=0.8V$	+50			$\mu\text{A}$
$I_{BHHO}$ $I_{BHLO}$	Bus Hold Overdrive Current on Bus Hold Input <sup>[9]</sup>	$V_{CC}=\text{Max.}, V_I=1.5V$			$\pm 500$	$\mu\text{A}$
$I_{OZH}$	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}, V_{OUT}=V_{CC}$			$\pm 1$	$\mu\text{A}$
$I_{OZL}$	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}, V_{OUT}=\text{GND}$			$\pm 1$	$\mu\text{A}$
$I_{OS}$	Short Circuit Current <sup>[7]</sup>	$V_{CC}=\text{Max.}, V_{OUT}=\text{GND}$	-60	-135	-240	mA
$I_{OFF}$	Power-Off Disable	$V_{CC}=0V, V_{OUT}\leq 4.5V$			$\pm 100$	$\mu\text{A}$
$I_{CC}$	Quiescent Power Supply Current	$V_{IN}\leq 0.2V,$ $V_{IN}\geq V_{CC}-0.2V$			+40	$\mu\text{A}$
$\Delta I_{CC}$	Quiescent Power supply Current (TTL inputs HIGH)	$V_{IN}=V_{CC}-0.6V$ <sup>[8]</sup>			+350	$\mu\text{A}$

**Electrical Characteristics For Balanced Drive Devices** Over the Operating Range  $V_{CC}=2.7V$  to  $3.6V$

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
$I_{ODL}$	Output LOW Dynamic Current <sup>[7]</sup>	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	45		180	mA
$I_{ODH}$	Output HIGH Dynamic Current <sup>[7]</sup>	$V_{CC}=3.3V, V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=1.5V$	-45		-180	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC}=\text{Min.}, I_{OH}=-0.1\text{ mA}$	$V_{CC}-0.2$			V
		$V_{CC}=3.0V, I_{OH}=-8\text{ mA}$	2.4 <sup>[10]</sup>	3.0		V
		$V_{CC}=3.0V, I_{OH}=-24\text{ mA}$	2.0	3.0		V
$V_{OL}$	Output LOW Voltage	$V_{CC}=\text{Min.}, I_{OL}=0.1\text{ mA}$			0.2	V
		$V_{CC}=\text{Min.}, I_{OL}=24\text{ mA}$		0.3	0.55	V

**Notes:**

9. Pins with bus hold are described in Pin Description.
10.  $V_{OH} = V_{CC} - 0.6V$  at rated current.



**Electrical Characteristics For Balanced Lite Drive Devices** Over the Operating Range  $V_{CC}=3.0V$  to  $3.6V$

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
$I_{ODL}$	Output LOW Current <sup>[7]</sup>	$V_{CC}=3.3V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ , $V_{OUT}=1.5V$	15.0		45	mA
$I_{ODH}$	Output HIGH Current <sup>[7]</sup>	$V_{CC}=3.3V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ , $V_{OUT}=1.5V$	-15.0		-45	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC}=3.0V$ , $I_{OH}=-6mA$	2.4	3.0		V
$V_{OL}$	Output LOW Voltage	$V_{CC}=3.0V$ , $I_{OL}=6mA$			0.55	V

**Capacitance<sup>[6]</sup>** ( $T_A = +25^\circ C$ ,  $f = 1.0 MHz$ )

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	4.5	6.0	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	5.5	8.0	pF

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit	
$I_{CCD}$	Dynamic Power Supply Current <sup>[10]</sup>	$V_{CC}=\text{Max.}$ , One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}=\text{GND}$	$V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	50	75	$\mu A/MHz$
$I_C$	Total Power Supply Current <sup>[11]</sup>	$V_{CC}=\text{Max.}$ , $f_1=10 MHz$ , 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}=\text{GND}$	$V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	0.5	0.8	mA
			$V_{IN}=V_{CC}-0.6V$ or $V_{IN}=\text{GND}$	0.5	0.8	mA
		$V_{CC}=\text{Max.}$ , $f_1=2.5 MHz$ , 50% Duty Cycle, Outputs Open, Six- teen Bits Toggling, $\overline{OE}=\text{GND}$	$V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	2.0	3.0 <sup>[12]</sup>	mA
			$V_{IN}=V_{CC}-0.6V$ or $V_{IN}=\text{GND}$	2.0	3.3 <sup>[12]</sup>	mA

**Notes:**

11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN}=3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.



**Switching Characteristics Over the Operating Range  $V_{CC}=3.0V$  to  $3.6V$  [14,15]**

Parameter	Description	CY74FCT163244A CY74FCT163H244A		CY74FCT163244C CY74FCT163H244C		Unit	Fig. No. [16]
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output	1.5	4.8	1.5	4.1	ns	1, 3
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	1.5	6.2	1.5	5.8	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	1.5	5.6	1.5	5.2	ns	1, 7, 8
t <sub>SK(O)</sub>	Output Skew [17]		0.5		0.5	ns	—

**Switching Characteristics Over the Operating Range  $V_{CC}=3.0V$  to  $3.6V$  [14,15]**

Parameter	Description	CY74FCT163LD244 [18] CY74FCT163LDH244		CY74FCT163LD244A [18] CY74FCT163LDH244A		Unit	Fig. No. [16]
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output	1.5	6.5	1.5	4.8	ns	1, 3
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	1.5	8.0	1.5	6.2	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	1.5	7.0	1.5	5.6	ns	1, 7, 8
t <sub>SK(O)</sub>	Output Skew [17]		0.5		0.5	ns	—

**Notes:**

14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. For  $V_{CC}=2.7$ , propagation delay, output enable and output disable times should be degraded by 20%.
16. See "Parameter Measurement Information" in the General Information section.
17. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
18. The load capacitance is 30 pF for Lite Drive devices. For all others it is 50 pF.

**Ordering Information CY74FCT163244**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT163244CPAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163244CPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT163244APAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163244APVC	O48	48-Lead (300-Mil) SSOP	

**Ordering Information CY74FCT163H244**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT163H244CPAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163H244CPVC	O48	48-Lead (300-Mil) SSOP	
4.8	CY74FCT163H244APAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163H244APVC	O48	48-Lead (300-Mil) SSOP	



**Ordering Information CY74FCT163LD244**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.8	CY74FCT163LD244APAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163LD244APVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT163LD244PAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163LD244PVC	O48	48-Lead (300-Mil) SSOP	

**Ordering Information CY74FCT163LDH244**

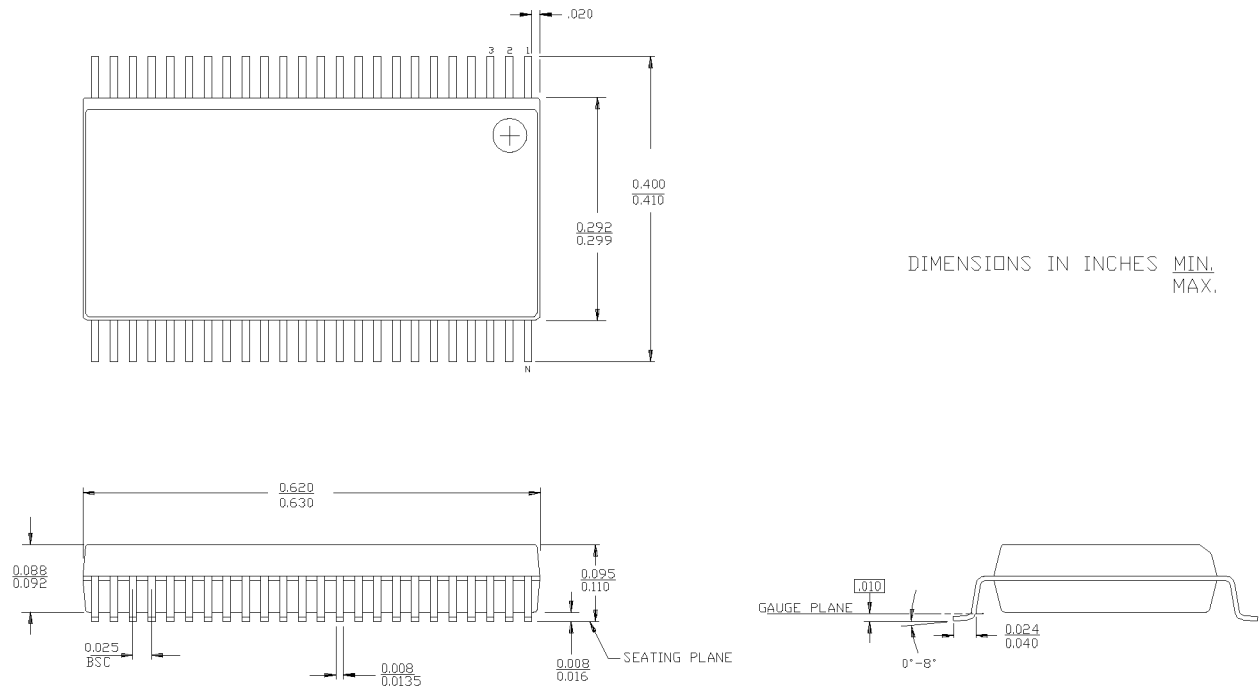
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.8	CY74FCT163LDH244APAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163LDH244APVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT163LDH244PAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163LDH244PVC	O48	48-Lead (300-Mil) SSOP	

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Package Diagrams

48-Lead Shrunken Small Outline Package O48



48-Lead Thin Shrunken Small Outline Package Z48

