NCP81212

Three Output Controller with Single SVID Interface for Desktop and Notebook CPU Applications

The NCP81212 (2 + 2 + 1 phase) three−output buck solution is optimized for Intel's IMVP8 CPUs.

The two multi−phase rail control systems are based on Dual−Edge pulse−width modulation (PWM) combined with DCR current sensing providing an ultra fast initial response to dynamic load events and reduced system cost.

The single−phase rail makes use of ON Semiconductor's patented high performance RPM operation. RPM control maximizes transient response while allowing for smooth transitions between discontinuous−frequency−scaling operation and continuous−mode full−power operation. The NCP81212 has an ultra−low offset current monitor amplifier with programmable offset compensation for high−accuracy current monitoring.

Multi−Phase Rail Features

- Dual Edge Modulation for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- Digital Soft Start Ramp
- Dynamic Reference Injection (Patent #US7057381)
- Accurate Total Summing Current Amplifier (Patent #US6683441)
- Dual High Impedance Differential Voltage and Total Current Sense Amplifiers
- Phase−to−Phase Dynamic Current Balancing
- True Differential Current Balancing Sense Amplifiers for Each Phase
- Adaptive Voltage Positioning (AVP)
- Switching Frequency Range of 300 kHz – 1.2 MHz
- Vin range 4.5 V to 25 V
- Startup into Pre−Charged Loads While Avoiding False OVP
- UltraSonic Operation

Single−Phase Rail Features

- Enhanced RPM Control System
- Ultra Low Offset IOUT Monitor
- Dynamic VID Feed−Forward
- Programmable Droop Gain
- Zero Droop Capable
- Thermal Monitor
- UltraSonic Operation
- Adjustable Vboot
- Digitally Controlled Operating Frequency

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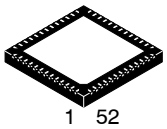
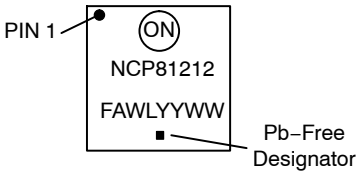


QFN52 6 × 6, 0.4P
CASE 485BE

MARKING DIAGRAM



F = Wafer Fab
A = Assembly Site
WL = Lot ID
YY = Year
WW = Work Week
▪ = Pb−Free Designator

ORDERING INFORMATION

Device	Package	Shipping†
NCP81212MNTXG	52 QFN	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Applications

- Desktop & Notebook Processors
- Gaming

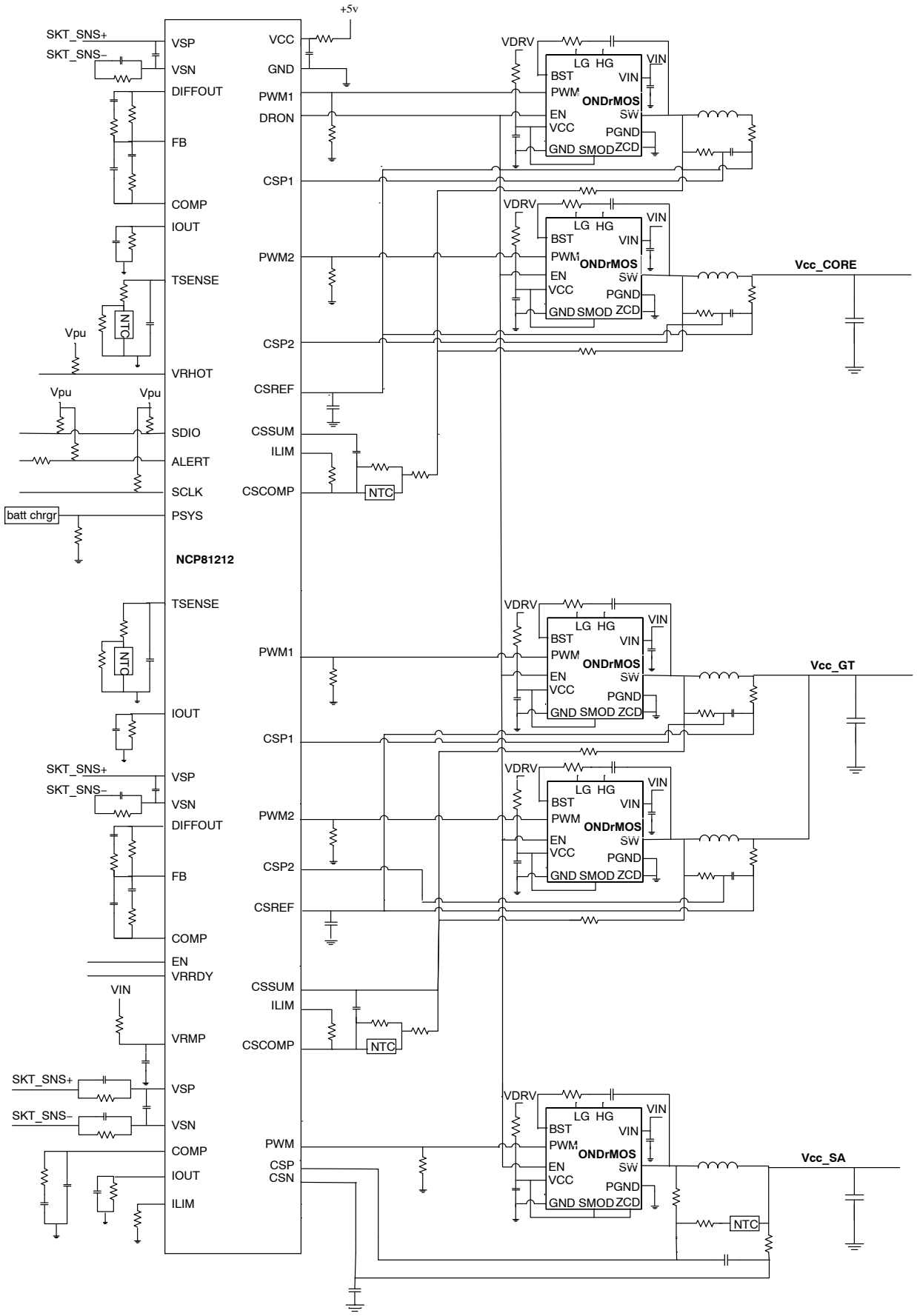

+5v
SKT_SNS+
SKT_SNS−
VSP
VSN
DIFFOUT
FB
COMP
IOUT
TSENSE
NTC
Vpu
VRHOT
Vpu
Vpu
SDIO
ALERT
SCLK
batt chrgr
PSYS
NCP81212
VCC
GND
PWM1
DRON
CSP1
PWM2
CSP2
CSREF
CSSUM
ILIM
CSCOMP
NTC
VDRV
LG HG
BST
VIN
PWM
ONDrMOS
EN
SW
VCC
PGND
GND SMOD ZCD
Vcc_CORE
Vcc_GT
Vcc_SA
EN
VRRDY
VIN
VRMP
PWM
CSP
CSN

Figure 1.

Pinout

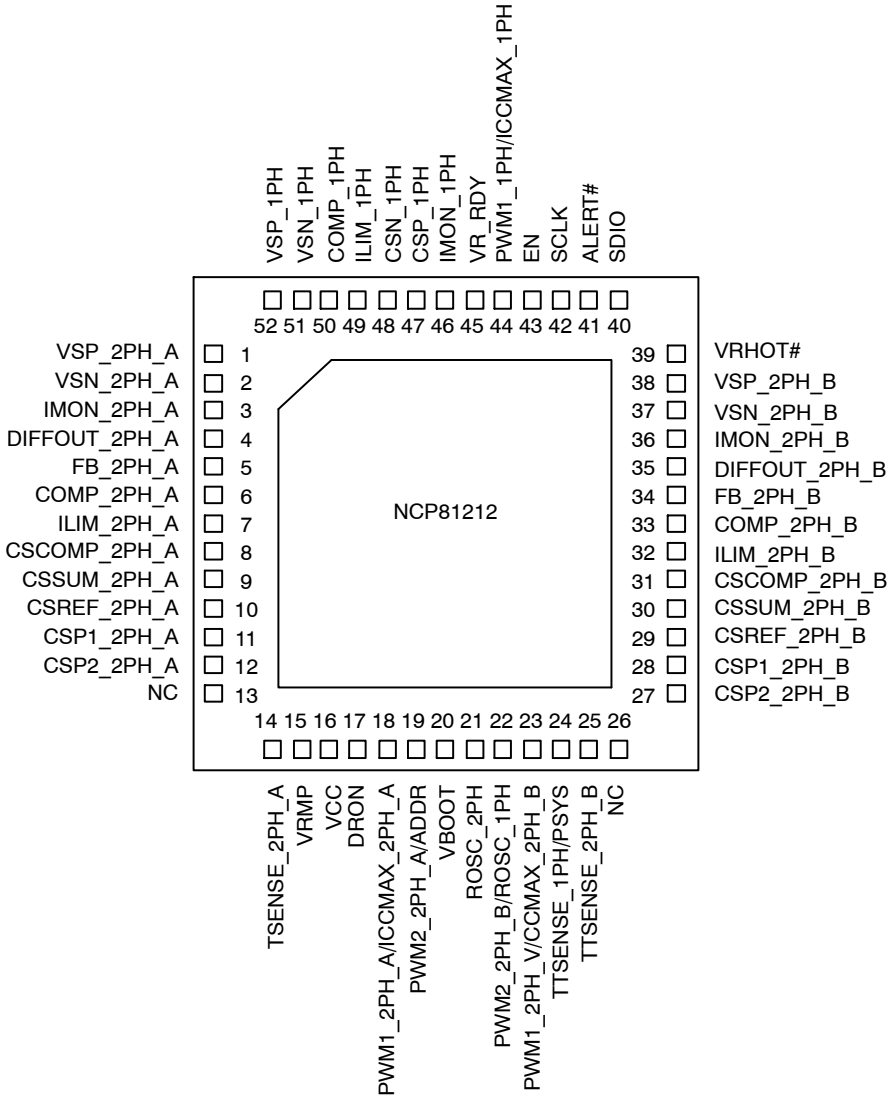


Figure 2. Pinout Diagram

Pin Function Description

Table 1. QFN52 PIN LIST DESCRIPTION

Pin	Name	Description
1	VSP_2PH_A	Differential output voltage sense positive for multi−phase rail “A”
2	VSN_2PH_A	Differential output voltage sense negative for multi−phase rail “A”
3	IMON_2PH_A	A resistor to ground programs IOUT gain for multi−phase rail “A”
4	DIFFOUT_2PH_A	Output of multi−phase rail “A” differential remote sense amplifier
5	FB_2PH_A	Error amplifier voltage feedback for multi−phase rail “A”
6	COMP_2PH_A	Error amplifier output and PWM comparator inverting input for multi−phase rail “A”
7	ILIM_2PH_A	A resistor to CSCOMP_2PH_A programs the over−current threshold for multi−phase rail “A”
8	CSCOMP_2PH_A	Total−current−sense amplifier output for multi−phase rail “A”
9	CSSUM_2PH_A	Inverting input of total−current−sense amplifier for multi−phase rail “A”
10	CSREF_2PH_A	Total−current−sense amplifier reference voltage input for multi−phase rail “A”
11	CSP1_2PH_A	Current−balance amplifier positive input for Phase 1 of multi−phase rail “A”
12	CSP2_2PH_A	Current−balance amplifier positive input for Phase 2 of multi−phase rail “A”
13	NC	No connect
14	TTSENSE_2PH_A	Temperature sense input for multi−phase rail “A”
15	VRMP	Vin feed−forward input. Controls a current used to generate the ramps of the modulators
16	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground
17	DRON	External FET driver enable for discrete driver or DrMOS
18	PWM1_2PH_A / ICCMAX_2PH_A	Phase 1 PWM output of multi−phase rail “A” / A resistor to ground programs ICCMAX for multi−phase rail “A”
19	PWM2_2PH_A / ADDR	Phase 2 PWM output of multi−phase rail “A” / A resistor to ground configures SVID addresses for all 3 rails (ADDR)
20	VBOOT	A resistor to ground configures boot voltage for all 3 rails (VBOOT)
21	ROSC_2PH	A resistor to ground configures Fsw for both “A” and “B” multi−phase rails (ROSC_2PH)
22	PWM2_2PH_B / ROSC_1PH	Phase 2 PWM output of multi−phase rail “B” / A resistor to ground configures Fsw for 1ph rail (ROSC_1ph)
23	PWM1_2PH_B / ICCMAX_2PH_B	Phase 1 PWM output of multi−phase rail “B” / A resistor to ground programs ICCMAX for multi−phase rail “B”
24	TTSENSE_1PH / PSYS	Temperature sense input for the single−phase rail / System input power monitor. A resistor to ground scales this signal
25	TTSENSE_2PH_B	Temperature sense input for multi−phase rail “B”
26	NC	No Connect
27	CSP2_2PH_B	Current−balance amplifier positive input for Phase 2 of multi−phase rail “B”
28	CSP1_2PH_B	Current−balance amplifier positive input for Phase 1 of multi−phase rail “B”
29	CSREF_2PH_B	Total−current−sense amplifier reference voltage input for multi−phase rail “B”
30	CSSUM_2PH_B	Inverting input of total−current−sense amplifier for multi−phase rail “B”
31	CSCOMP_2PH_B	Total−current−sense amplifier output for multi−phase rail “B”
32	ILIM_2PH_B	A resistor to CSCOMP_2PH_B programs the over−current threshold for multi−phase rail “B”
33	COMP_2PH_B	Error amplifier output and PWM comparator inverting input for multi−phase rail “B”
34	FB_2PH_B	Error amplifier voltage feedback for multi−phase rail “B”
35	DIFFOUT_2PH_B	Output of multi−phase rail “B” differential remote sense amplifier
36	IMON_2PH_B	A resistor to ground programs IOUT gain for multi−phase rail “B”
37	VSN_2PH_B	Differential output voltage sense negative for multi−phase rail “B”
38	VSP_2PH_B	Differential output voltage sense positive for multi−phase rail “B”
39	VR_HOT#	Thermal logic output for over−temperature condition on TTSENSE pins
40	SDIO	Serial VID data interface
41	ALERT#	Serial VID ALERT#

Table 1. QFN52 PIN LIST DESCRIPTION (continued)

Pin	Name	Description
42	SCLK	Serial VID clock
43	EN	Enable input. High enables all three rails
44	PWM_1PH / ICCMAX_1PH	PWM output of the single−phase rail / A resistor to ground programs ICCMAX for the single−phase rail
45	VR_RDY	VR_RDY indicates all three rails are ready to accept SVID commands
46	IMON_1PH	A resistor to ground programs IOUT gain for the single−phase rail
47	CSP_1PH	Differential current sense positive for the single−phase rail
48	CSN_1ph	Differential current sense negative for the single−phase rail
49	ILIM_1ph	A resistor to ground programs ILIM gain for the single−phase rail
50	COMP_1ph	Compensation for single−phase rail
51	VSN_1ph	Differential output voltage sense negative for single−phase rail
52	VSP_1ph	Differential output voltage sense positive for single−phase rail
53	Tab	GND

Electrical Information

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMPX	VCC + 0.3 V	−0.3 V	2 mA	2 mA
CSCOMPX	VCC + 0.3 V	−0.3 V	2 mA	2 mA
VSN	GND + 300 mV	GND − 300 mV	1 mA	1 mA
VRDY	VCC + 0.3 V	−0.3 V	N/A	2 mA
VCC	6.5 V	−0.3 V	N/A	N/A
VRMP	+25 V	−0.3 V		
All Other Pins	VCC + 0.3 V	−0.3 V		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. All signals referenced to GND unless noted otherwise.

Thermal Information

Table 3. THERMAL INFORMATION

Description	Symbol	Typ	Unit
Thermal Characteristic, QFN Package (Note 2)	R_{JA}	68	°C/W
Operating Junction Temperature Range (Note 3)	T_J	−10 to 125	°C
Operating Ambient Temperature Range		−10 to 100	°C
Maximum Storage Temperature Range	T_{STG}	− 40 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	

1. The maximum package power dissipation must be observed
2. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
3. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

Table 4. ELECTRICAL CHARACTERISTICS
(Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; CVCC = 0.1μF)

Parameter	Test Conditions	MIN	TYP	MAX	Units
ERROR AMPLIFIER					
Input Bias Current		−900		900	nA
Open Loop DC Gain	CL = 20 pF to GND, RL = 10 KΩ to GND		80		dB
Open Loop Unity Gain Bandwidth	CL = 20 pF to GND, RL = 10 KΩ to GND		20		MHz
Slew Rate	ΔVin = 100 mV, G = −10 V/V, ΔVout = 0.75 V − 1.52 V, CL = 20 pF to GND, DC Load = 10 k to GND		5		V/μs
Maximum Output Voltage	I_{SOURCE} = 2.0 mA	3.5	–	–	V
Minimum Output Voltage	I_{SINK} = 2.0 mA	–	–	1	V
DIFFERENTIAL SUMMING AMPLIFIER					
Input Bias Current		−25	–	25	nA
VSP Input Voltage Range		−0.3	–	3.0	V
VSN Input Voltage Range		−0.3	–	0.3	V
−3dB Bandwidth	CL = 20 pF to GND, RL = 10 KΩ to GND		22.5		MHz
Closed Loop DC gain VS to DIFF	VS+ to VS− = 0.5 to 1.3 V		1.0		V/V
Maximum Output Voltage	I_{SOURCE} = 2 mA	3.5	–	–	V
Minimum Output Voltage	I_{SINK} = 2 mA	–	–	0.8	V
CURRENT SUMMING AMPLIFIER					
Offset Voltage (Vos)		−300		300	μV
Input Bias Current	CSSUM = CSREF = 1V	−7.5		7.5	μA
Open Loop Gain			80		dB
Current Sense Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 KΩ to GND		15		MHz
Maximum CSCOMP (A) Output Voltage	Isource = 2 mA	3.5	–	–	V
Minimum CSCOMP(A) Output Voltage	Isink = 500 μA	–	–	0.15	V
CURRENT BALANCE AMPLIFIER					
Input Bias Current	CSPX − CSPX + 1 = 1.2 V	−50	–	50	nA
Common Mode Input Voltage Range	CSPx = CSREF	0	–	2.3	V
Differential Mode Input Voltage Range	CSNx = 1.2 V	−100	–	100	mV
Closed loop Input Offset Voltage Matching	CSPx = 1.2 V, Measured from the average	−1.5	–	1.5	mV
Current Sense Amplifier Gain	0 V < CSPx < 0.1 V,	5.7	6.0	6.3	V/V
Multiphase Current Sense Gain Matching	CSREF = CSP = 10 mV to 30 mV	−3		3	%
−3 dB Bandwidth			8		MHz
BIAS SUPPLY					
Supply Voltage Range		4.75		5.25	V
VCC Quiescent Current	PS0		33	45	mA
VCC Quiescent Current	PS3		20		mA
VCC Quiescent Current	PS4 at 25°C		400		μA

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; CVCC = 0.1μF)

Parameter	Test Conditions	MIN	TYP	MAX	Units
BIAS SUPPLY					
VCC Quiescent Current	Enable low			60	μA
UVLO Threshold	VCC rising			4.5	V
	VCC falling	4			V
VCC UVLO Hysteresis			250		mV
VRMP					
Supply Range		4.5		20	V
UVLO Threshold	VRamp rising			4.25	V
	VRamp falling	3			V
UVLO Hysteresis			675		mV
DAC SLEW RATE					
Slew Rate Fast			>10		mV/μs
Soft Start Slew Rate			1/2 SR Fast		mV/μs
Slew Rate Slow			1/2 SR Fast		mV/μs
ENABLE INPUT					
Enable High Input Leakage Current	Enable = 0	−1		1	μA
Upper Threshold	V_{UPPER}	0.8			V
Lower Threshold	V_{LOWER}			0.3	V
Enable Delay Time	Measure time from Enable transitioning HI , VBOOT is not 0 V			2.5	ms
DRON					
Output High Voltage	Sourcing 500 μA	3.0	–	–	V
Output Low Voltage	Sinking 500 μA	–	–	0.1	V
Pull Up Resistances			2.0		kΩ
Rise/Fall Time	CL (PCB) = 20pF, ΔVo = 10% to 90%	–	160		ns
Internal Pull Down Resistance	VCC = 0 V		70		kΩ
OVERCURRENT PROTECTION					
Ilim Threshold Current (delayed OCP shutdown)	PS0	9	10	11	μA
	PS1, PS2, PS3 (N = PS0 phase count)		10/N		μA
Ilim Threshold Current (immediate OCP shutdown)	PS0	13.5	15	16.5	μA
	PS1, PS2, PS3 (N = PS0 phase count)		15/N		μA
Shutdown Delay	Immediate		300		ns
	Delayed		50		μs
ILIM Output Voltage Offset	Ilim sourcing 10 μA Measured relative to CSRef	−2		2	mV
IOUT_4PH /IOUT_2PH OUTPUT					
Output Offset Current	V_{Ilim} = 5 V			0.25	μA
Output current max	Ilimit sink current 20 μA		200		μA
Current Gain	(Iout current)/(Ilimit Current) Rlim = 20 K, Riout = 5 K DAC = 0.8 V, 1.25 V, 1.52 V	9.5	10	10.5	A/A
OSCILLATOR					

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; CVCC = 0.1μF)

Parameter	Test Conditions	MIN	TYP	MAX	Units
OSCILLATOR					
Switching Frequency Range		300	–	1200	kHz
Switching Frequency Accuracy	300KHz < Fsw < 1MHz	−10	–	10	%
PSYS					
Input Current	R_{psys} = 20 kΩ			100	μA
ADC resolution	8 bit		7.81		mV/LSB
Register update rate				500	μs
Disable Threshold				4.5	V
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Over Voltage Threshold During Soft−Start		1.9	2.0	2.1	V
Over Voltage Threshold Above DAC	VSP rising	370	400	430	mV
Over Voltage Delay	VSP rising to PWMx low		25		ns
Under Voltage Threshold Below DAC−DROOP	VSP falling	225	300	370	mV
Under−voltage Hysteresis	VSP rising		25		mV
Under−Voltage Delay			5		μs
SVID DAC					
System Voltage Accuracy	.75 V ≤ DAC < 1.52 V 0.5V < DAC < .745 V 0.25 V DAC < 0.495 V	−0.5 −8 −10		0.5 8 10	% mV mV
MODULATORS (PWM COMPARATORS) FOR A RAIL & B RAIL					
Minimum Pulse Width	Fsw = 350 KHz		40		ns
0% Duty Cycle	COMP voltage when the PWM outputs remain LO		1.3	–	V
100% Duty Cycle	COMP voltage when the PWM outputs remain HI VRMP=12.0 V	–	2.5	–	V
PWM Phase Angle Error	Between adjacent phases		±5		°
TSENSE					
VRHOT Assert Threshold			468		mV
VRHOT Rising Threshold			488		mV
Alert Assertion Threshold			488		mV
Alert Rising Threshold			510		mV
TSENSE Bias Current		115	120	125	μA
VRHOT					
Output Low Saturation Voltage	I_{VR_HOT} = −4 mA			0.3	V
Output Leakage Current	High Impedance State	−1	–	1	μA
ADC					
Voltage Range		0		2	V
Total Unadjusted Error (TUE)		−1		1	%
Differential Nonlinearity (DNL)	8−bit			1	LSB
Power Supply Sensitivity			+/−1		%
Conversion Time			7.4		μs
Round Robin			206		μs
VRDY OUTPUT					
Output Low Saturation Voltage	I_{VR_RDY} = 4 mA,	–	–	0.3	V

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; CVCC = 0.1μF)

Parameter	Test Conditions	MIN	TYP	MAX	Units
VRDY OUTPUT					
Rise Time	External pull−up of 1 KΩ to 3.3 V C_{TOT} = 45 pF, ΔVo = 10% to 90%	−	−	150	ns
Fall Time	External pull−up of 1 KΩ to 3.3 V C_{TOT} = 45 pF, ΔVo = 90% to 10%	−	−	150	ns
Output Leakage Current When High	VR_RDY= 5.0 V	−1	−	1	μA
VR_RDY Delay (rising)	En rising to VR_RDY rising (TA)	−	−	2.5	ms
VR_RDY Delay (falling)	Due to OCP or OVP	−	0.3	−	μs
	En falling to VR_RDY falling (TD + $\overline{TE}$)	−	−	1.5	μs
PWM OUTPUTS					
Output High Voltage	Sourcing 500 μA	VCC − 0.2 V	−	−	V
Output Mid Voltage	No Load	1.9	2.0	2.1	V
Output Low Voltage	Sinking 500 μA	−	−	0.7	V
Rise and Fall Time	CL (PCB) = 50pF, ΔVo =10% to 90% of VCC	−	5		ns
Tri−State Output Leakage	Gx = 2.0 V, x = 1−2, EN = Low	−1	−	1	μA
PHASE DETECTION					
CSPX Phase Disable Voltage		4.75			V
SCLK, SDIO, ALERT#					
V_{IL}	Input Low Voltage			.45	V
VIH	Input High Voltage	.65			V
VOH	Output High Voltage		1.05		V
VOL	SDIO, ALERT#			0.3	V
Leakage Current		−1		1	μA
Pin Capacitance	@25°C only		9		pF
VR clock to data delay (Tco)				12	ns
Setup time (Tsu)		7			ns
Hold time (Thld)		14			ns
ERROR AMPLIFIER					
Input Bias Current		−25	−	25	nA
VSP Input Voltage Range		−0.3	−	3.0	V
VSN Input Voltage Range		−0.3	−	0.3	V
gm		1.34	1.6	1.85	mS
Output Offset Current		−15		15	μA
Open loop Gain	Load= 1nF in series with 1 kΩ in parallel with 10 pF to ground	70	73		dB
Source Current	Input Differential −200 mV		280		μA
Sink Current	Input Differential 200 mV		280		μA
−3 dB Bandwidth	Load= 1nF in series with 1 kΩ in parallel with 10 pF to ground		20		MHz

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; CVCC = 0.1μF)

Parameter	Test Conditions	MIN	TYP	MAX	Units
IOUT					
gm		0.97	1	1.03	mS
Output Offset Current	CSP = CSN	−250		250	nA
DROOP					
gm		0.96	1	1.04	mS
Output Offset Current	CSP = CSN	−1.5		1.5	μA
OVERCURRENT PROTECTION					
ILIMIT Threshold		1.275	1.3	1.325	V
ILIMIT Delay			200		ns
ILIMIT Gain	I_{ILIMIT}/(CSP-CSN) CSP-CSN=20mV	0.925	1	1.075	mS
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Over Voltage Threshold During Soft-Start			2.0		V
Over Voltage Threshold Above DAC	VSP - VSN - VID setting	370		430	mV
Over Voltage Delay	VSP rising to PWMx low		25		ns
Over Voltage VR_RDY Delay	VSP rising to VR_RDY low		350		ns
Under Voltage Threshold	VSP - VSN falling	215	300	385	mV
Under-voltage Hysteresis	VSP - VSN falling/rising		25		mV
Under-voltage Blanking Delay	VSP-VSN falling to VR_RDY falling		5		μs
CSP−CSN ZCD COMPARATOR					
Offset Accuracy			±1.5		mV

Table 5. IMVP8 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	Hex
0	0	0	0	0	0	0	0	Off	00
0	0	0	0	0	0	0	1	0.25	01
0	0	0	0	0	0	1	0	0.255	02
0	0	0	0	0	0	1	1	0.26	03
0	0	0	0	0	1	0	0	0.265	04
0	0	0	0	0	1	0	1	0.27	05
0	0	0	0	0	1	1	0	0.275	06
0	0	0	0	0	1	1	1	0.28	07
0	0	0	0	1	0	0	0	0.285	08
0	0	0	0	1	0	0	1	0.29	09
0	0	0	0	1	0	1	0	0.295	0A
0	0	0	0	1	0	1	1	0.3	0B
0	0	0	0	1	1	0	0	0.305	0C
0	0	0	0	1	1	0	1	0.31	0D
0	0	0	0	1	1	1	0	0.315	0E
0	0	0	0	1	1	1	1	0.32	0F
0	0	0	1	0	0	0	0	0.325	10
0	0	0	1	0	0	0	1	0.33	11
0	0	0	1	0	0	1	0	0.335	12
0	0	0	1	0	0	1	1	0.34	13
0	0	0	1	0	1	0	0	0.345	14
0	0	0	1	0	1	0	1	0.35	15
0	0	0	1	0	1	1	0	0.355	16
0	0	0	1	0	1	1	1	0.36	17
0	0	0	1	1	0	0	0	0.365	18
0	0	0	1	1	0	0	1	0.37	19
0	0	0	1	1	0	1	0	0.375	1A
0	0	0	1	1	0	1	1	0.38	1B
0	0	0	1	1	1	0	0	0.385	1C
0	0	0	1	1	1	0	1	0.39	1D
0	0	0	1	1	1	1	0	0.395	1E
0	0	0	1	1	1	1	1	0.4	1F
0	0	1	0	0	0	0	0	0.405	20
0	0	1	0	0	0	0	1	0.41	21
0	0	1	0	0	0	1	0	0.415	22
0	0	1	0	0	0	1	1	0.42	23
0	0	1	0	0	1	0	0	0.425	24
0	0	1	0	0	1	0	1	0.43	25
0	0	1	0	0	1	1	0	0.435	26
0	0	1	0	0	1	1	1	0.44	27
0	0	1	0	1	0	0	0	0.445	28
0	0	1	0	1	0	0	1	0.45	29
0	0	1	0	1	0	1	0	0.455	2A
0	0	1	0	1	0	1	1	0.46	2B
0	0	1	0	1	1	0	0	0.465	2C
0	0	1	0	1	1	0	1	0.47	2D
0	0	1	0	1	1	1	0	0.475	2E

Table 5. IMVP8 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	Hex
0	0	1	0	1	1	1	1	0.48	2F
0	0	1	1	0	0	0	0	0.485	30
0	0	1	1	0	0	0	1	0.49	31
0	0	1	1	0	0	1	0	0.495	32
0	0	1	1	0	0	1	1	0.5	33
0	0	1	1	0	1	0	0	0.505	34
0	0	1	1	0	1	0	1	0.51	35
0	0	1	1	0	1	1	0	0.515	36
0	0	1	1	0	1	1	1	0.52	37
0	0	1	1	1	0	0	0	0.525	38
0	0	1	1	1	0	0	1	0.53	39
0	0	1	1	1	0	1	0	0.535	3A
0	0	1	1	1	0	1	1	0.54	3B
0	0	1	1	1	1	0	0	0.545	3C
0	0	1	1	1	1	0	1	0.55	3D
0	0	1	1	1	1	1	0	0.555	3E
0	0	1	1	1	1	1	1	0.56	3F
0	1	0	0	0	0	0	0	0.565	40
0	1	0	0	0	0	0	1	0.57	41
0	1	0	0	0	0	1	0	0.575	42
0	1	0	0	0	0	1	1	0.58	43
0	1	0	0	0	1	0	0	0.585	44
0	1	0	0	0	1	0	1	0.59	45
0	1	0	0	0	1	1	0	0.595	46
0	1	0	0	0	1	1	1	0.6	47
0	1	0	0	1	0	0	0	0.605	48
0	1	0	0	1	0	0	1	0.61	49
0	1	0	0	1	0	1	0	0.615	4A
0	1	0	0	1	0	1	1	0.62	4B
0	1	0	0	1	1	0	0	0.625	4C
0	1	0	0	1	1	0	1	0.63	4D
0	1	0	0	1	1	1	0	0.635	4E
0	1	0	0	1	1	1	1	0.64	4F
0	1	0	1	0	0	0	0	0.645	50
0	1	0	1	0	0	0	1	0.65	51
0	1	0	1	0	0	1	0	0.655	52
0	1	0	1	0	0	1	1	0.66	53
0	1	0	1	0	1	0	0	0.665	54
0	1	0	1	0	1	0	1	0.67	55
0	1	0	1	0	1	1	0	0.675	56
0	1	0	1	0	1	1	1	0.68	57
0	1	0	1	1	0	0	0	0.685	58
0	1	0	1	1	0	0	1	0.69	59
0	1	0	1	1	0	1	0	0.695	5A
0	1	0	1	1	0	1	1	0.7	5B
0	1	0	1	1	1	0	0	0.705	5C
0	1	0	1	1	1	0	1	0.71	5D

Table 5. IMVP8 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	Hex
0	1	0	1	1	1	1	0	0.715	5E
0	1	0	1	1	1	1	1	0.72	5F
0	1	1	0	0	0	0	0	0.725	60
0	1	1	0	0	0	0	1	0.73	61
0	1	1	0	0	0	1	0	0.735	62
0	1	1	0	0	0	1	1	0.74	63
0	1	1	0	0	1	0	0	0.745	64
0	1	1	0	0	1	0	1	0.75	65
0	1	1	0	0	1	1	0	0.755	66
0	1	1	0	0	1	1	1	0.76	67
0	1	1	0	1	0	0	0	0.765	68
0	1	1	0	1	0	0	1	0.77	69
0	1	1	0	1	0	1	0	0.775	6A
0	1	1	0	1	0	1	1	0.78	6B
0	1	1	0	1	1	0	0	0.785	6C
0	1	1	0	1	1	0	1	0.79	6D
0	1	1	0	1	1	1	0	0.795	6E
0	1	1	0	1	1	1	1	0.8	6F
0	1	1	1	0	0	0	0	0.805	70
0	1	1	1	0	0	0	1	0.81	71
0	1	1	1	0	0	1	0	0.815	72
0	1	1	1	0	0	1	1	0.82	73
0	1	1	1	0	1	0	0	0.825	74
0	1	1	1	0	1	0	1	0.83	75
0	1	1	1	0	1	1	0	0.835	76
0	1	1	1	0	1	1	1	0.84	77
0	1	1	1	1	0	0	0	0.845	78
0	1	1	1	1	0	0	1	0.85	79
0	1	1	1	1	0	1	0	0.855	7A
0	1	1	1	1	0	1	1	0.86	7B
0	1	1	1	1	1	0	0	0.865	7C
0	1	1	1	1	1	0	1	0.87	7D
0	1	1	1	1	1	1	0	0.875	7E
0	1	1	1	1	1	1	1	0.88	7F
1	0	0	0	0	0	0	0	0.885	80
1	0	0	0	0	0	0	1	0.89	81
1	0	0	0	0	0	1	0	0.895	82
1	0	0	0	0	0	1	1	0.9	83
1	0	0	0	0	1	0	0	0.905	84
1	0	0	0	0	1	0	1	0.91	85
1	0	0	0	0	1	1	0	0.915	86
1	0	0	0	0	1	1	1	0.92	87
1	0	0	0	1	0	0	0	0.925	88
1	0	0	0	1	0	0	1	0.93	89
1	0	0	0	1	0	1	0	0.935	8A
1	0	0	0	1	0	1	1	0.94	8B
1	0	0	0	1	1	0	0	0.945	8C

Table 5. IMVP8 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	Hex
1	0	0	0	1	1	0	1	0.95	8D
1	0	0	0	1	1	1	0	0.955	8E
1	0	0	0	1	1	1	1	0.96	8F
1	0	0	1	0	0	0	0	0.965	90
1	0	0	1	0	0	0	1	0.97	91
1	0	0	1	0	0	1	0	0.975	92
1	0	0	1	0	0	1	1	0.98	93
1	0	0	1	0	1	0	0	0.985	94
1	0	0	1	0	1	0	1	0.99	95
1	0	0	1	0	1	1	0	0.995	96
1	0	0	1	0	1	1	1	1	97
1	0	0	1	1	0	0	0	1.005	98
1	0	0	1	1	0	0	1	1.01	99
1	0	0	1	1	0	1	0	1.015	9A
1	0	0	1	1	0	1	1	1.02	9B
1	1	0	1	0	0	0	0	1.285	D0
1	1	0	1	0	0	0	1	1.29	D1
1	1	0	1	0	0	1	0	1.295	D2
1	1	0	1	0	0	1	1	1.3	D3
1	1	0	1	0	1	0	0	1.305	D4
1	1	0	1	0	1	0	1	1.31	D5
1	1	0	1	0	1	1	0	1.315	D6
1	1	0	1	0	1	1	1	1.32	D7
1	1	0	1	1	0	0	0	1.325	D8
1	1	0	1	1	0	0	1	1.33	D9
1	1	0	1	1	0	1	0	1.335	DA
1	1	0	1	1	0	1	1	1.34	DB
1	1	0	1	1	1	0	0	1.345	DC
1	1	0	1	1	1	0	1	1.35	DD
1	1	0	1	1	1	1	0	1.355	DE
1	1	0	1	1	1	1	1	1.36	DF
1	1	1	0	0	0	0	0	1.365	E0
1	1	1	0	0	0	0	1	1.37	E1
1	1	1	0	0	0	1	0	1.375	E2
1	1	1	0	0	0	1	1	1.38	E3
1	1	1	0	0	1	0	0	1.385	E4
1	1	1	0	0	1	0	1	1.39	E5
1	1	1	0	0	1	1	0	1.395	E6
1	1	1	0	0	1	1	1	1.4	E7
1	1	1	0	1	0	0	0	1.405	E8
1	1	1	0	1	0	0	1	1.41	E9
1	1	1	0	1	0	1	0	1.415	EA
1	1	1	0	1	0	1	1	1.42	EB
1	1	1	0	1	1	0	0	1.425	EC
1	1	1	0	1	1	0	1	1.43	ED
1	1	1	0	1	1	1	0	1.435	EE
1	1	1	0	1	1	1	1	1.44	EF

Table 5. IMVP8 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	Hex
1	1	1	1	0	0	0	0	1.445	F0
1	1	1	1	0	0	0	1	1.45	F1
1	1	1	1	0	0	1	0	1.455	F2
1	1	1	1	0	0	1	1	1.46	F3
1	1	1	1	0	1	0	0	1.465	F4
1	1	1	1	0	1	0	1	1.47	F5
1	1	1	1	0	1	1	0	1.475	F6
1	1	1	1	0	1	1	1	1.48	F7
1	1	1	1	1	0	0	0	1.485	F8
1	1	1	1	1	0	0	1	1.49	F9
1	1	1	1	1	0	1	0	1.495	FA
1	1	1	1	1	0	1	1	1.5	FB
1	1	1	1	1	1	0	0	1.505	FC
1	1	1	1	1	1	0	1	1.51	FD
1	1	1	1	1	1	1	0	1.515	FE
1	1	1	1	1	1	1	1	1.52	FF
1	0	0	1	1	1	0	0	1.025	9C
1	0	0	1	1	1	0	1	1.03	9D
1	0	0	1	1	1	1	0	1.035	9E
1	0	0	1	1	1	1	1	1.04	9F
1	0	1	0	0	0	0	0	1.045	A0
1	0	1	0	0	0	0	1	1.05	A1
1	0	1	0	0	0	1	0	1.055	A2
1	0	1	0	0	0	1	1	1.06	A3
1	0	1	0	0	1	0	0	1.065	A4
1	0	1	0	0	1	0	1	1.07	A5
1	0	1	0	0	1	1	0	1.075	A6
1	0	1	0	0	1	1	1	1.08	A7
1	0	1	0	1	0	0	0	1.085	A8
1	0	1	0	1	0	0	1	1.09	A9
1	0	1	0	1	0	1	0	1.095	AA
1	0	1	0	1	0	1	1	1.1	AB
1	0	1	0	1	1	0	0	1.105	AC
1	0	1	0	1	1	0	1	1.11	AD
1	0	1	0	1	1	1	0	1.115	AE
1	0	1	0	1	1	1	1	1.12	AF
1	0	1	1	0	0	0	0	1.125	B0
1	0	1	1	0	0	0	1	1.13	B1
1	0	1	1	0	0	1	0	1.135	B2
1	0	1	1	0	0	1	1	1.14	B3
1	0	1	1	0	1	0	0	1.145	B4
1	0	1	1	0	1	0	1	1.15	B5
1	0	1	1	0	1	1	0	1.155	B6
1	0	1	1	0	1	1	1	1.16	B7
1	0	1	1	1	0	0	0	1.165	B8
1	0	1	1	1	0	0	1	1.17	B9
1	0	1	1	1	0	1	0	1.175	BA

Table 5. IMVP8 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	Hex
1	0	1	1	1	0	1	1	1.18	BB
1	0	1	1	1	1	0	0	1.185	BC
1	0	1	1	1	1	0	1	1.19	BD
1	0	1	1	1	1	1	0	1.195	BE
1	0	1	1	1	1	1	1	1.2	BF
1	1	0	0	0	0	0	0	1.205	C0
1	1	0	0	0	0	0	1	1.21	C1
1	1	0	0	0	0	1	0	1.215	C2
1	1	0	0	0	0	1	1	1.22	C3
1	1	0	0	0	1	0	0	1.225	C4
1	1	0	0	0	1	0	1	1.23	C5
1	1	0	0	0	1	1	0	1.235	C6
1	1	0	0	0	1	1	1	1.24	C7
1	1	0	0	1	0	0	0	1.245	C8
1	1	0	0	1	0	0	1	1.25	C9
1	1	0	0	1	0	1	0	1.255	CA
1	1	0	0	1	0	1	1	1.26	CB
1	1	0	0	1	1	0	0	1.265	CC
1	1	0	0	1	1	0	1	1.27	CD
1	1	0	0	1	1	1	0	1.275	CE
1	1	0	0	1	1	1	1	1.28	CF

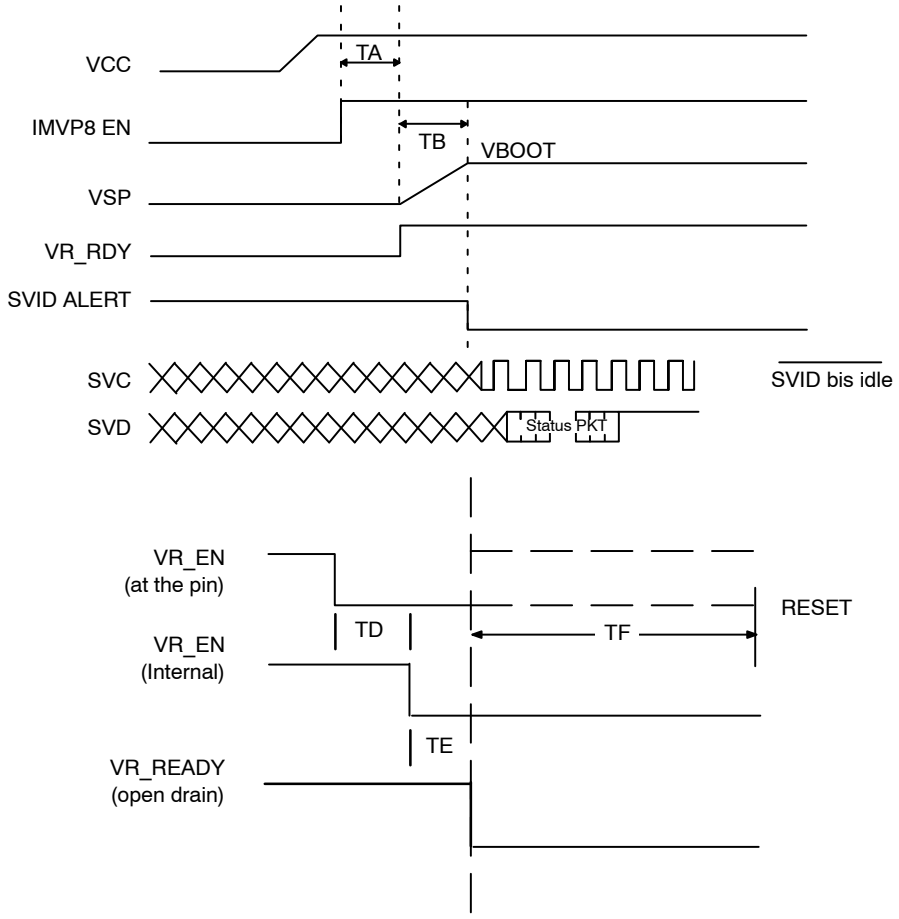


Figure 3. Startup Timing

Table 6.

	MIN	TYP	MAX
TA			2.5 ms
TB			VID / Slow
TD	0 us		1 us
TE			500 ns

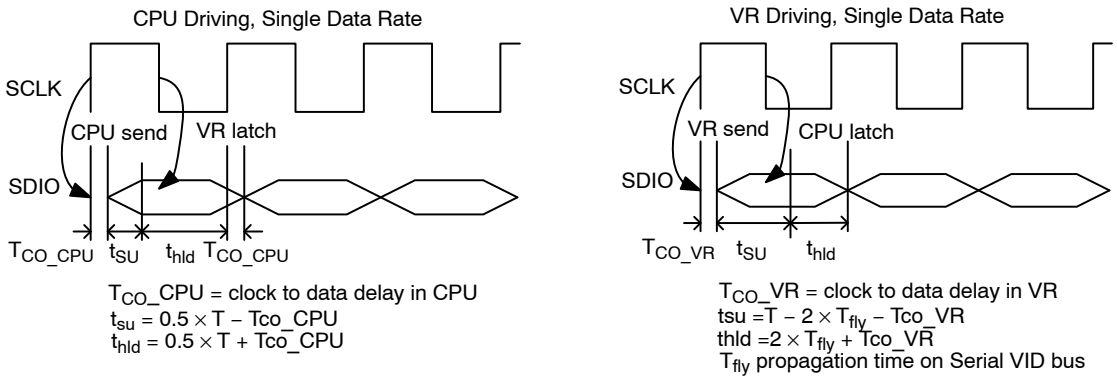


Figure 4. SVID Timing Diagram

GENERAL

The NCP81212 is a three rail 2 + 2 + 1 phase PWM controller with a single serial SVID control interface.

Serial VID

The NCP81212 supports the Intel serial VID interface. It communicates with the microprocessor through three wires (SCLK, SDIO, ALERT#). The table of supported registers for Domains 00h, 01h, and 02/03h is shown below. The SVID register set for Domain 0Dh is smaller and contains the following registers: 00h, 01h, 02h, 05h, 10h, 11h, and 1Bh.

Table 7.

Index	Name	Description	Access	Default 00h/01h/02h	PSYS 0Dh
00h	Vendor ID	Uniquely identifies the VR vendor. The vendor ID assigned by Intel to ON Semiconductor is 0x1A	R	1Ah	1Ah
01h	Product ID	Uniquely identifies the VR product. The VR vendor assigns this number. 2Ch = NCP81212	R	2Ch	2Ch
02h	Product Revision	Uniquely identifies the revision or stepping of the VR control IC. The VR vendor assigns this data.	R		
03h	Product date code ID		R		
05h	Protocol ID	Identifies the SVID Protocol the controller supports. 05h = IMVP8	R	05h	05h
06h	Capability	Informs the Master of the controller's Capabilities Bit0 = Iout ADC (15h) = 1 Bit1 = Vout ADC (16h) = 0 Bit2 = Pout ADC (18h) = 0 Bit3 = I input ADC (19h) = 0 Bit4 = V input ADC (1Ah) = 1 Bit5 = P input ADC (1Bh) = 0 Bit6 = Temperature ADC (17h) = 1 Bit7 = 1 if (15h) is Iout = 1	R	D1h	N/A
10h	Status_1	Data register read after the ALERT# signal is asserted. Conveying the status of the VR.	R	00h	00h
11h	Status_2	Data register showing optional status_2 data.	R	00h	00h
12h	Temp zone	Data register showing temperature zones the system is operating in	R	00h	N/A
15h	I_out	8 bit binary word ADC of current. This register reads 0xFF when the output current is at Icc_Max	R		N/A
17h	VR_Temp	8 bit binary word ADC of voltage. Binary format in deg C, IE 100C=64h. A value of 00h indicates this function is not supported	R		N/A
1Bh	Input Power	Required for Input Power Domain Address 0Dh	R	N/A	
1Ch	Status2_last read	When the status 2 register is read its contents are copied into this register. The format is the same as the Status 2 Register	R	00h	N/A
21h	Icc_Max	Data register containing the Icc_Max the platform supports. The value is measured on the ICCMAX pin on power up and placed in this register. From that point on the register is read only	R	00h	N/A
22h	Temp_Max	Data register containing the max temperature the platform supports and the level VR_hot asserts. This value defaults to 100°C and programmable over the SVID Interface	R/W	64h	N/A
24h	SR_fast	Slew Rate for SetVID_fast commands. Binary format in mV/us	R	1Eh	N/A
25h	SR_slow	Slew Rate for SetVID_slow commands. Determined by SR_Slow selector register (2Ah)	R	0Fh	N/A

Table 7. (continued)

Index	Name	Description	Access	Default 00h/01h/02h	PSYS 0Dh
26h	Vboot	Vboot is resistor programmed at startup. The controller will ramp to Vboot and hold at Vboot until it receives a new SetVID command to move to a different voltage.	R	00h	N/A
2Ah	SR_Slow selector	Fast_SR/2: default Fast_SR/4 Fast_SR/8 Fast_SR/16	R/W	01h	N/A
2Bh	PS4 exit latency	Reflects the latency of exiting PS4 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID Slow/Fast command to the output voltage beginning to ramp	R	8Ch	N/A
2Ch	PS3 exit latency	Reflects the latency of exiting PS3 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID/SetPS command until the controller is capable of supplying max current of the command PS state	R	55h	N/A
2Dh	EN to Ready for SVID command (TA)	Reflects the latency from enable assertion to the VR controller being ready to accept SVID commands	R	CAh	N/A
2Eh	Pin Max	Input Power Sensor Scaling	RW	N/A	FFh
30h	Vout_Max	Programmed by master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with “not supported” acknowledge. IMVP8 VID format	RW	FBh	N/A
31h	VID setting	Data register containing currently programmed VID voltage. VID data format	RW	00h	N/A
32h	Pwr State	Register containing the current programmed power state	RW	00h	N/A

33h	Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0=positive margin, 1= negative margin. Remaining 7 BITS are # VID steps for margin 2s complement.
		00h = no margin
		01h = +1 VID step
		02h = +2 VID steps
		FFh = −1 VID step
		FEh = −2 VID steps
			RW	00h	N/A

34h	MultiVR Config			01h	N/A
42h	IVID1−VID		RW	00h	N/A
43h	IVID1−I	Maximum instantaneous current for single phase operation	RW		N/A
44h	IVID2−VID		RW	00h	N/A
45h	IVID2−I	Maximum instantaneous current for IVID 2 state	RW		N/A
46h	IVID3−VID		RW	00h	N/A
47h	IVID3−I	Maximum instantaneous current for DCM/CCM decision threshold	RW		N/A

VID code change is supported by SVID interface with three options as below:

Table 8.

Option	SVID Command Code	Feature Description	Register Address (Indicating the slew rate of VID code change)
SetVID_Fast	01h	30 mV/us	24h
SetVID_Slow	02h	Adjustable Default setting is 1/2 of Fast Slew Rate	25h
SetVID_Decay	03h	No control, VID code down	N/A

The NCP81212 is optimized to meet Intel's IMVP8 specification and implements PS0, PS1, PS2, PS3 and PS4 power saving states.

Table 9.

Power State	PWM Output Operating Mode of 2−Phase Rails
PS0	Multi−phase PWM interleaving output
PS1	Single−phase RPM CCM mode
PS2	Single−phase RPM DCM mode
PS3	Single−phase RPM DCM mode
PS4	Vout to 0 V, no phase state

NCP81212 Configurations

The NCP81212 has four Configuration pins that are secondary−functions on PWM pins. On power up a 10 μA current is sourced from these pins through a resistor connected to this pin and the resulting voltage is measured. The following features will be programmed:

- SVID address
  - 00h (IA) and 01h (GT) options for both multi−phase rails
  - Single−phase rail can be 02h (SA) or 03h (GTUS)
- Phase doubler
  - The multi−phase A rail can use a Phase Doubler from ON Semiconductor
  - Options to enable doubling on the A rail is provided in the Vboot configuration table
- Switching Frequency
  - Both multi−phase rails' per−phase switching frequency will be the same programmable value.
  - The 1−phase Fsw is programmed independently
  - The Fsw values are shown in the ROSC table
- Vboot
  - Addresses 00h, 01h, and 03 POR Vboot is 0 V
  - Address 02h POR Vboot is 1.05 V
  - Vboot options are shown in the VBOOT table

Boot Voltage

Vboot for the NCP81212 is externally programmed using a single resistor.

See Vboot pin voltages and the corresponding Vboot level in the table below. During startup, the pin voltage is measured. This value cannot be changed after the initial power up sequence is complete.

Table 10. VBOOT PIN 20 CONFIGURATION

Resistor	2PH_A VBOOT	2PH_B VBOOT	1PH VBOOT	Rail A Doubler
6.19 kΩ	0 V	0 V	0 V	No
14.7 kΩ	0 V	0 V	0 V	Yes
24.9 kΩ	0 V	0 V	1.05 V	No
37.4 kΩ	0 V	0 V	1.05 V	Yes
53.6 kΩ	0 V	0 V	0.95 V	No
73.2 kΩ	0 V	0 V	0.95 V	Yes
97.6 kΩ	0 V	0 V	0.8 V	No
130 kΩ	0 V	0 V	0.8 V	Yes
169 kΩ	1.05 V	1.05 V	1.05 V	No
215 kΩ	1.05 V	1.05 V	1.05 V	Yes

SVID Address Pin

Table 11. NCP81212 (2 + 2 + 1)

Pull−Down Resistor	Slew Rate mV/us	2PH_A Address	2PH_B Address	1PH Address	Pin 24 TSENSE/PSYS	A Max Phases	B Max Phases
4.3 kΩ	30	00h	01h	02h	PSYS	2	2
12.1 kΩ		00h	01h	03h	TSENSE	2	2
19.6 kΩ		01h	00h	02h	PSYS	2	2
31.6 kΩ		01h	00h	03h	TSENSE	2	2
49.9 kΩ	10	00h	01h	02h	PSYS	2	2
78.7 kΩ		00h	01h	03h	TSENSE	2	2
121 kΩ		01h	00h	02h	PSYS	2	2
174 kΩ		01h	00h	03h	TSENSE	2	2

PSYS

The PSYS pin is an analog input to the NCP81212. It is a system input power monitor that facilitates the monitoring of the total platform system power. The system power is sensed at the platform charging device, the NCP81212 facilitates reporting back current and through the SVID interface at address 0Dh.

Remote Sense Amplifier (Multiphase)

A high performance high input impedance true differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage to:

$$V_{DIFOUT} = (V_{VSP} - V_{VSN)} + (1.3\ V - V_{DAC)} + (V_{DROOP} - V_{CSREF)} \quad \text{(eq. 1)}$$

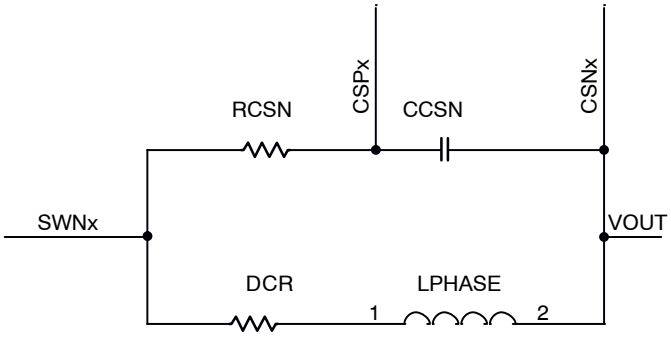
This signal then goes through a standard error compensation network and into the inverting input of the error amplifier. The non−inverting input of the error amplifier is connected to the same 1.3 V reference used for the differential sense amplifier output bias.

High Performance Voltage Error Amplifier (Multiphase)

A high performance error amplifier is provided for high bandwidth transient performance. A standard type III compensation circuit is normally used to compensate the system.

Differential Current Feedback Amplifiers (Multiphase)

Each phase has a low offset differential amplifier to sense that phase current for current balance. The inputs to the CSPx pins are high impedance inputs. It is also recommended that the voltage sense element be no less than 0.5mOhm for accurate current balance. Fine tuning of this time constant is generally not required. The individual phase current is summed into the PWM comparator feedback this way current is balanced via a current mode control approach.



$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} \times DCR} \quad \text{(eq. 2)}$$

Figure 5.

Total Current Sense Amplifier (Multiphase)

The NCP81212 uses a patented approach to sum the phase currents into a single temperature compensated total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The total current signal is floating with respect to CSREF. The current signal is the difference between CSCOMP and CSREF. The Ref(n) resistors sum the signals from the output side of the inductors to create a low impedance virtual ground. The amplifier actively filters and gains up the voltage applied across the inductors to recover the voltage drop across the inductor series resistance (DCR). Rth is placed near an inductor to sense the temperature of the inductor. This allows the filter time constant and gain to be a function of the Rth NTC resistor and compensate for the change in the DCR with temperature.

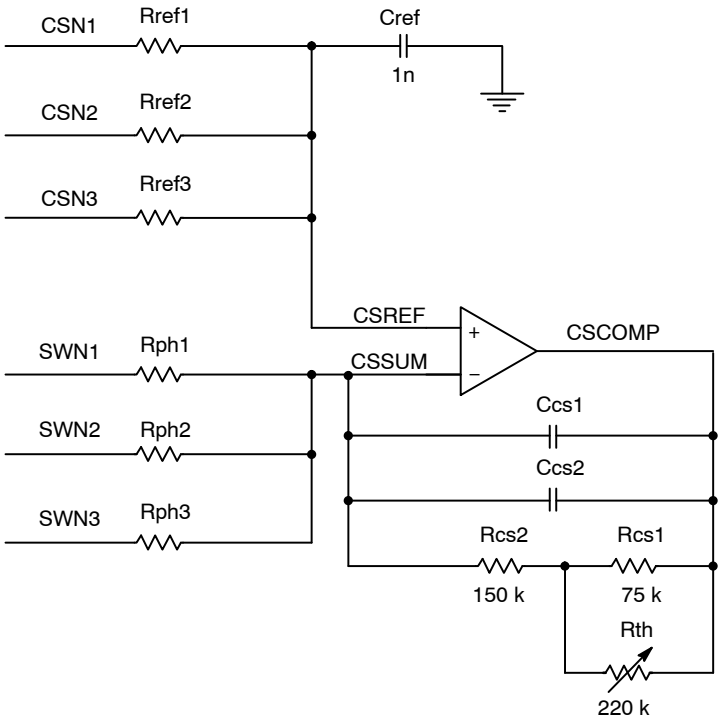


Figure 6.

The DC gain equation for the current sensing:

$$V_{CSCOMP-CSREF} = -\frac{R_{CS}2 + \frac{R_{CS}1 \times R_{th}}{R_{CS}1 + R_{th}}}{R_{ph}} \times (Iout_{Total} \times DCR) \quad \text{(eq. 3)}$$

Set the gain by adjusting the value of the Rph resistors. The DC gain should be set to the output voltage droop. If the voltage from CSCOMP to CSREF is less than 100 mV at ICCMAX then it is recommend increasing the gain of the CSCOMP amp. This is required to provide a good current signal to offset voltage ratio for the ILIMIT pin. When no droop is needed, the gain of the amplifier should be set to provide ~100 mV across the current limit programming resistor at full load. The values of Rcs1 and Rcs2 are set based on the 220 k NTC and the temperature effect of the inductor and should not need to be changed. The NTC should be placed near the closest inductor. The output voltage droop should be set with the droop filter divider.

The pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor. This allows the circuit to recover the inductor DCR voltage drop current signal. Ccs1 and Ccs2 are in parallel to allow for fine tuning of the time constant using commonly available values. It is best to fine tune this filter during transient testing.

$$F_Z = \frac{DCR@25C}{2 \times PI \times L_{Phase}} \quad \text{(eq. 4)}$$

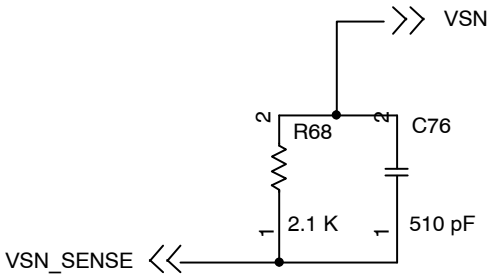
Programming the Current Limit (Multiphase)

The current limit thresholds are programmed with a resistor between the ILIMIT and CSCOMP pins. The ILIMIT pin mirrors the voltage at the CSREF pin and mirrors the sink current internally to IOUT (reduced by the IOUT Current Gain) and the current limit comparators. The 100% current limit trips if the ILIMIT sink current exceeds 10 μA for 50 μs. The 150% current limit trips with minimal delay if the ILIMIT sink current exceeds 15 μA. Set the value of the current limit resistor based on the CSCOMP−CSREF voltage as shown below.

$$R_{LIMIT} = \frac{R_{CS}2 + \frac{R_{CS}1 \times R_{th}}{R_{CS}1 + R_{th}} \times (Iout_{Total} \times DCR)}{10\mu} \quad \text{OR} \quad R_{LIMIT} = \frac{V_{CSCOMP} - CSREF@ILIMIT}{10\mu} \qquad \text{(eq. 5)}$$

Programming DAC Feed−Forward Filter (Multiphase)

The DAC feed−forward implementation is realized by having a filter on the VSN pin. Programming Rvsn sets the gain of the DAC feed−forward and Cvsn provides the time constant to cancel the time constant of the system per the following equations. Cout is the total output capacitance and Rout is the output impedance of the system.



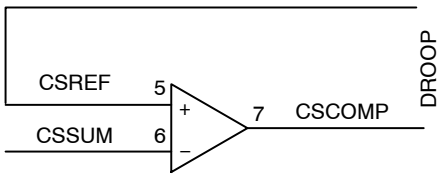
$$R_{vsn} = C_{out} \times R_{out} \times 453.6 \times 10^6$$

$$C_{vsn} = \frac{R_{out} \times C_{out}}{R_{vsn}} \qquad \text{(eq. 6)}$$

Figure 7.

Programming DROOP (Multiphase)

The signals CSCOMP and CSREF are differentially summed with the output voltage feedback to add precision voltage droop to the output voltage.



$$Droop = DCR \times (R_{CS}/R_{ph}) \qquad \text{(eq. 7)}$$

Figure 8.

Programming IOUT (Multiphase)

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A pull−up resistor from 5 V VCC can be used to offset the IOUT signal positive if needed.

$$R_{IOUT} = \frac{2.0V \times R_{LIMIT}}{10 \times \frac{R_{CS}2 + \frac{R_{CS}1 \times R_{th}}{R_{CS}1 + R_{th}}}{R_{ph}} \times (Iout_{ICC\_MAX} \times DCR)} \qquad \text{(eq. 8)}$$

Programming ICC_MAX (Multiphase)

The SVID interface provides the platform ICC_MAX value at register 21h for. A resistor to ground on the IMAX pin programs these registers at the time the part is enabled. 10 μA is sourced from these pins to generate a voltage on the program resistor. The value of the register is 1 A per LSB and is set by the equation below. The resistor value should be no less than 10 k.

$$ICC\_MAX_{21h} = \frac{R \times 10\ \mu A \times 256\ A}{2\ V} \qquad \text{(eq. 9)}$$

Programming TSENSE

A temperature sense inputs are provided. A precision current is sourced out the output of the TSENSE pin to generate a voltage on the temperature sense network. The voltage on the temperature sense input is sampled by the internal A/D converter. A 100 k NTC similar to the VISHAY ERT−J1VS104JA should be used. Rcomp1 is mainly used for noise. See the specification table for the thermal sensing voltage thresholds and source current.

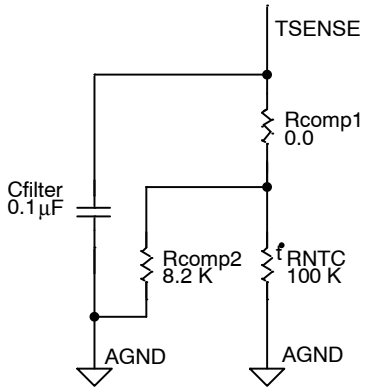


Figure 9.

Precision Oscillator

A programmable precision oscillator is provided. The clock oscillator serves as the master clock to the ramp generator circuit. This oscillator is programmed by a resistor to ground on the ROSC pin. The oscillator frequency range is between 300 KHz/phase to 1.2 MHz/phase. The ROSC pin provides approximately 2 V out and the source current is mirrored into the internal ramp oscillator. The oscillator frequency is approximately proportional to the current flowing in the ROSC resistor.

Table 12. 2 PHASE / 1 PHASE FSW V ROSC (PIN21 / PIN22)

Resistor	Per phase Fsw MPH_A	Per phase Fsw MPH_B	Per phase Fsw 1PH
6.19 kΩ	1.2 MHz	1.2 MHz	1.2 MHz
14.7 kΩ	1.1 MHz	1.1 MHz	1.1 MHz
24.9 kΩ	1.0 MHz	1.0 MHz	1.0 MHz
37.4 kΩ	900 kHz	900 kHz	900 kHz
53.6 kΩ	800 kHz	800 kHz	800 kHz
73.2 kΩ	700 kHz	700 kHz	700 kHz
97.6 kΩ	600 kHz	600 kHz	600 kHz
130 kΩ	500 kHz	500 kHz	500 kHz
169 kΩ	400 kHz	400 kHz	400 kHz
215 kΩ	300 kHz	300 kHz	300 kHz

The oscillator generates triangle ramps that are 0.5~2.5 V in amplitude depending on the VRMP pin voltage to provide input voltage feed forward compensation. The ramps are equally spaced out of phase with respect to each other and the signal phase rail is set half way between phases 1 and 2 of the multi−phase rail for minimum input ripple current.

For use with ON Semiconductor's phase doubler, the NCP81212 offers the user the ability to multiply the frequency of multiphase rail A. On the NCP81212, the switching frequency is increased by a factor of 2 when the phase doubler configuration is used.

Programming the Ramp Feed−Forward Circuit

The ramp generator circuit provides the ramp used by the PWM comparators. The ramp generator provides voltage feed−forward control by varying the ramp magnitude with respect to the VRMP pin voltage. The VRMP pin also has a 4 V UVLO function. The VRMP UVLO is only active after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled.

The PWM ramp time is changed according to the following:

$$V_{RAMP_{PP}} = 0.1 \times V_{VRMP} \quad \text{(eq. 10)}$$

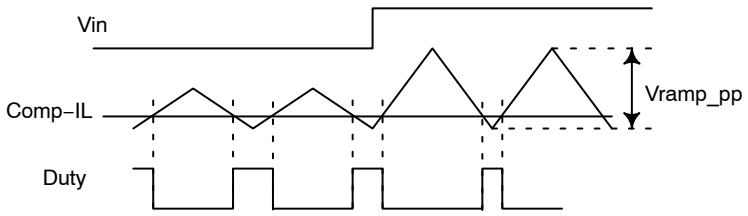


Figure 10.

PWM Comparators

The non−inverting input of the comparator for each phase is connected to the summed output of the error amplifier (COMP) and each phase current (IL × DCR × Phase Balance Gain Factor). The inverting input is connected to the oscillator ramp voltage with a 1.3 V offset. The operating input voltage range of the comparators is from 0 V to 3.0 V and the output of the comparator generates the PWM output

During steady state operation, the duty cycle is centered on the valley of the sawtooth ramp waveform. The steady state duty cycle is still calculated by approximately Vout/Vin. During a transient event, the controller will operate in a hysteretic mode with the duty cycles pull in for all phases as the error amp signal increases with respect to all the ramps.

Pase Detection Sequence

The NCP81212 normally operates as a 2−ph VccCORE + 2−ph VccGT + 1−ph VccSA. Phases of the multi−phase rails can be disabled by pulling up CSP pins to VCC.

For example, to configure one of the 2 phase rails of the NCP81212 as a 1 phase rail, CSP2 of that rail must be pulled up to Vcc on startup.

Both the single−phase rail and the multi−phase rail B can be disabled by pulling all of their associated CSP pins to Vcc. Phase 1 of multi−phase rail A cannot be disabled.

The PWM outputs are logic−level devices intended for driving fast response external gate drivers or DrMOS. As each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one PWM output can be on at the same time to allow overlapping phases.

PROTECTION FEATURES

Under voltage Lockouts

There are several under voltage monitors in the system. Hysteresis is incorporated within the comparators. NCP81212 monitors the 5 V VCC supply. The gate driver monitors both the gate driver VCC and the BST voltage. When the voltage on the gate driver is insufficient it will pull DRON low and prevents the controller from being enabled. The gate driver will hold DRON low for a minimum period of time to allow the controller to hold off its startup sequence. In this case the PWM is set to the MID state to begin soft start.

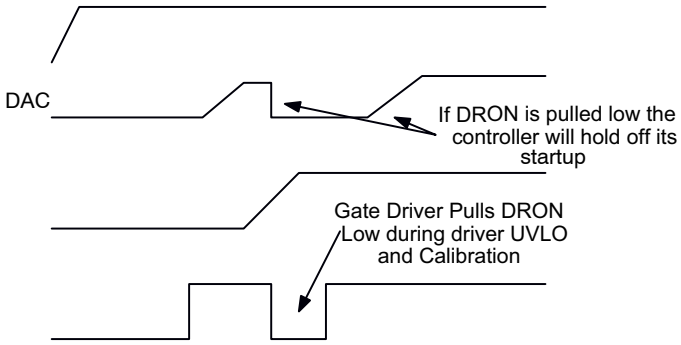


Figure 11. Gate Driver UVLO Restart

Soft start

Soft start is implemented internally. A digital counter steps the DAC up from zero to the target voltage based on the predetermined rate in the spec table. The PWM signals will start out open with a test current to collect data on phase count and for setting internal registers. After the configuration data is collected, if the controller is enabled the PWMs will be set to 2.0V MID state to indicate that the drivers should be in diode mode. DRON will then be asserted. As the DAC ramps the PWM outputs will begin to fire. Each phase will move out of the MID state when the first PWM pulse is produced. When the controller is disabled the PWM signal will return to the MID state.

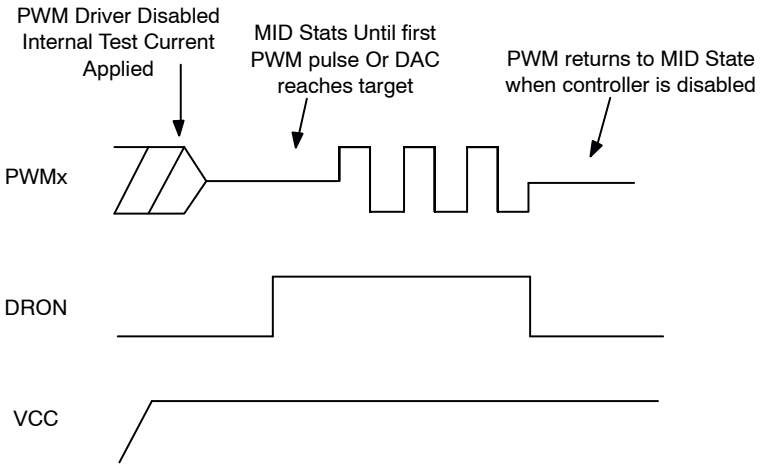


Figure 12.

Over Current Latch− Off Protection (Multiphase)

The NCP81212 compares a programmable current−limit set point to the voltage from the output of the current−summing amplifier. The level of current limit is set with the resistor from the ILIM pin to CSCOMP. The current through the external resistor connected between ILIM and CSCOMP is then compared to the internal current limit current I_{CL}. If the current generated through this resistor into the ILIM pin (Ilim) exceeds the internal current−limit threshold current (I_{CL}), an internal latch−off counter starts, and the controller shuts down if the fault is not removed after 50 μs(shut down immediately for 150% load current) after which the outputs will remain disabled until the Vcc voltage or EN is toggled.

The voltage swing of CSCOMP cannot go below ground. This limits the voltage drop across the DCR through the current balance circuitry. An inherent per−phase current limit protects individual phases if one or more phases stop functioning because of a faulty component. The over−current limit is programmed by a resistor on the ILIM pin. The resistor value can be calculated by the following equations,

Equation related to the NCP81212 multiphase rails:

$$R_{ILIM} = \frac{I_{LIM} \times DCR \times R_{CS}/R_{PH}}{I_{CL}} \qquad \text{(eq. 11)}$$

Where I_{CL} = 10 μA

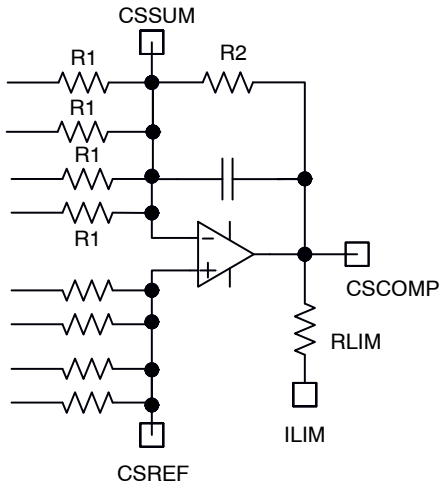


Figure 13.

Under Voltage Monitor

The output voltage is monitored at the output of the differential amplifier for UVLO. If the output falls more than 300 mV below the DAC−DROOP voltage the UVLO comparator will trip sending the VR_RDY signal low. The 300 mV limit can be reprogrammed using the VR_Ready_Low Limit register.

Over Voltage Protection

The output voltage is also monitored at the output of the differential amplifier for OVP. During normal operation, if the output voltage exceeds the DAC voltage by 400 mV, the VR_RDY flag goes low, and the output voltage will be ramped down to 0 V. The part will stay in this mode until the Vcc voltage or EN is toggled

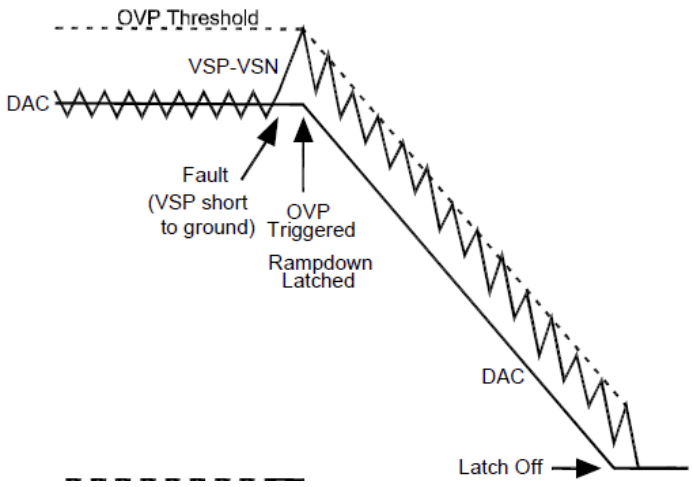


Figure 14.

During start up, the OVP threshold is set to 2.0 V. This allows the controller to start up without false triggering the OVP.

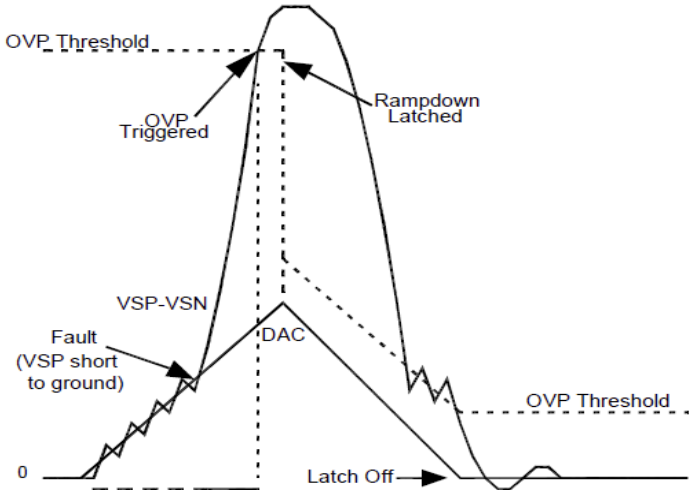


Figure 15.

Single−phase Rail

The architecture of the single−phase rail makes use of a digitally enhanced, high performance, current mode RPM control method that provides excellent transient response while minimizing transient aliasing. The average operating frequency is digitally stabilized to remove frequency drift under all continuous mode operating conditions. At light load the single−phase rail automatically transitions into DCM operation to save power.

Single−phase Rail Remote Sense Error Amplifier

A high performance, high input impedance, true differential transconductance amplifier is provided to accurately sense the regulator output voltage and provide high bandwidth transient performance. The VSP and VSN inputs should be connected to the regulator's output voltage sense points through filter networks described in the following Droop section and the DAC Feedforward filter section. The remote sense error amplifier outputs a current proportional to the difference between the output voltage and the DAC voltage:

$$I_{COMP} = gm[V_{DAC} - (V_{VSP} - V_{VSN})] \quad \text{(eq. 12)}$$

This current is applied to a standard Type II compensation network.

Single−phase Rail Voltage Compensation

The Remote Sense Amplifier outputs a current that is applied to a Type II compensation network formed by external tuning components CLF, RZ and CHF.

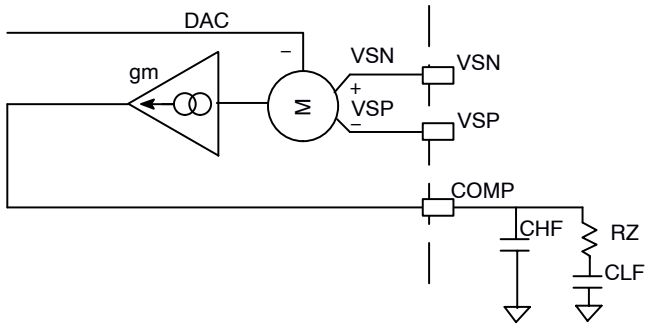


Figure 16.

Single−phase Rail – Differential Current Feedback Amplifier

The single−phase controller has a low offset, differential amplifier to sense output inductor current. An external lowpass filter can be used to superimpose a reconstruction of the AC inductor current onto the DC current signal sensed across the inductor. The lowpass filter time constant should match the inductor L/DCR time constant by setting the filter pole frequency equal to the zero of the output inductor. This makes the filter AC output mimic the product of AC inductor current and DCR, with the same gain as the filter DC output. It is best to perform fine tuning of the filter pole during transient testing.

$$F_z = \frac{DCR@25C}{2 \times \pi \times L} \qquad F_P = \frac{1}{2 \times \pi \times \left(\frac{R_{PHSP} \times (R_{th} + R_{CSSP})}{R_{PHSP} + R_{th} + R_{CSSP}}\right) \times C_{CSSP}} \quad \text{(eq. 13)}$$

Forming the lowpass filter with an NTC thermistor (Rth) placed near the output inductor, compensates both the DC gain and the filter time constant for the inductor DCR change with temperature. The values of RPHSP and RCSSP are set based on the effect of temperature on both the thermistor and inductor. The CSP and CSN pins are high impedance inputs, but it is recommended that the lowpass filter resistance not exceed 10kOhm in order to avoid offset due to leakage current. It is also recommended that the voltage sense element (inductor DCR) be no less than 0.5mOhm for sufficient current accuracy. Recommended values for the external filter components are:

R_{PHSP} = 7.68 kOhm
R_{CSSP} = 14.3 kOhm
Rth = 100 kOhm, Beta = 4300

$$F_P = \frac{1}{2 \times \pi \times \left(\frac{R_{PHSP} \times (R_{th} + R_{CSSP})}{R_{PHSP} + R_{th} + R_{CSSP}}\right) \times C_{CSSP}} \quad \text{(eq. 14)}$$

Using 2 parallel capacitors in the lowpass filter allows fine tuning of the pole frequency using commonly available capacitor values.

The DC gain equation for the current sense amplifier output is:

$$V_{CURR} = \frac{R_{th} + R_{CSSP}}{R_{PHSP} + R_{th} + R_{CSSP}} \times Iout \times DCR \quad \text{(eq. 15)}$$

To improve the noise immunity of the current feedback amplifier, it is recommended to use an RC low pass filter (R_F and C_F in Figure below) on the CSN pin of the amplifier placed as close as possible to the controller. The bandwidth of this filter should be ~5 MHz with $R_F < 20\ \Omega$. To mitigate against noise due to excessive ringing that may be present on the inductor side of R_{PHSP}, it is recommended to use a capacitor in parallel with the inductor. The value of the capacitor should be chosen such that:

$$\sqrt{L} \times C \ll \frac{1}{2 \times \pi \times \text{Ringing Fraquency}} \quad \text{(eq. 16)}$$

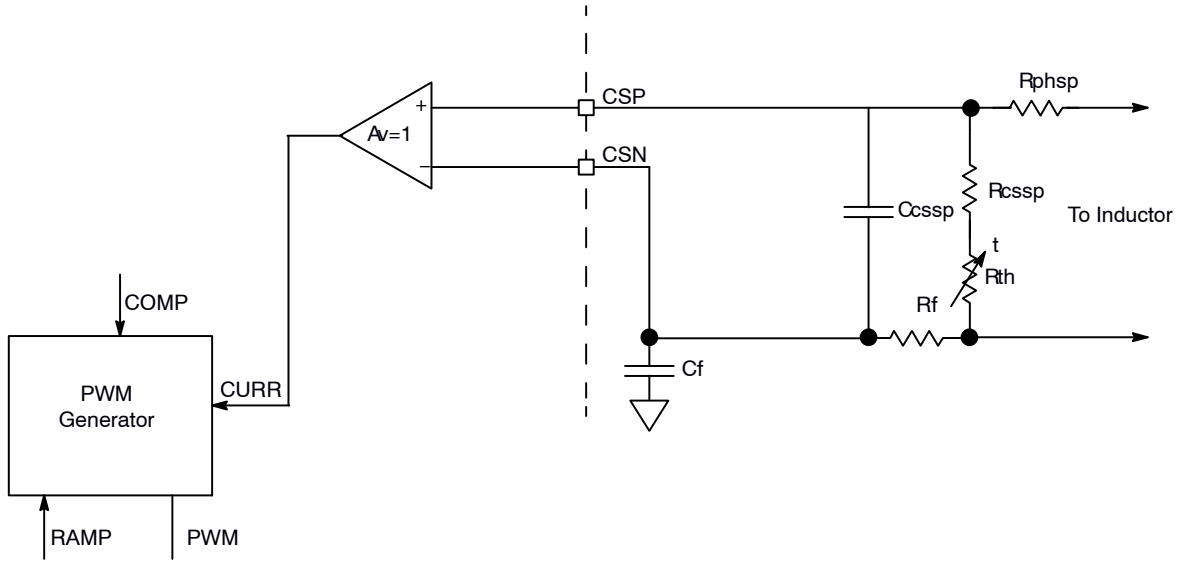


Figure 17.

The amplifier output signal is combined with the COMP and RAMP signals at the PWM comparator inputs to produce the Ramp Pulse Modulation (RPM) PWM signal.

Single−phase Rail – Loadline Programming (DROOP)

An output loadline is a power supply characteristic wherein the regulated (DC) output voltage decreases by a voltage V_{DROOP}, proportional to load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transients faster than those to which the regulation loop can respond. In the NCP81212, a loadline is produced by adding a signal proportional to output load current (V_{DROOP}) to the output voltage feedback signal – thereby satisfying the voltage regulator at an output voltage reduced proportional to load current. V_{DROOP} is developed across a resistance between the VSP pin and the output voltage sense point.

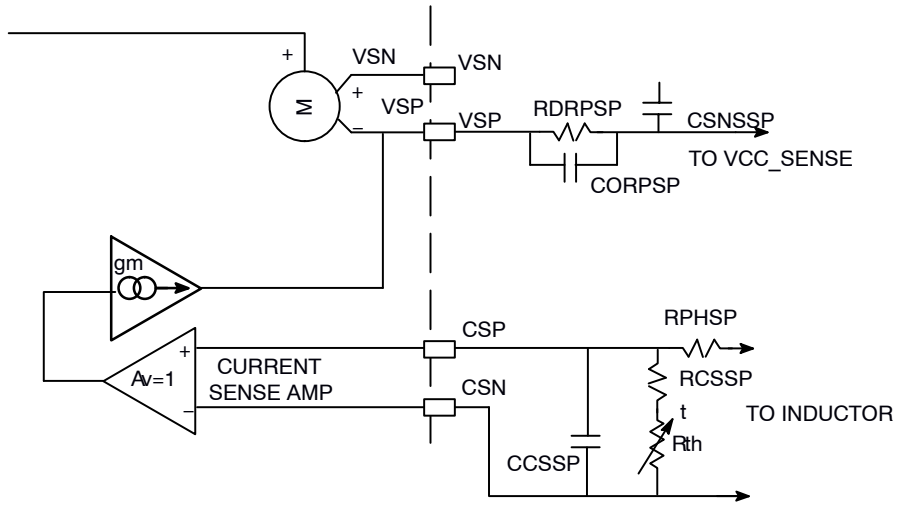


Figure 18.

$$V_{Droop} = R_{DRPSP} \times gm \times \frac{R_{th} + R_{CSSP}}{R_{PHSP} + R_{TH} + R_{CSSP}} \times I_{out} \times DCR \qquad \text{(eq. 17)}$$

The loadline is programmed by choosing R_{DRPSP} such that the ratio of voltage produced across R_{DRPSP} to output current is equal to the desired loadline.

$$R_{DRPSP} = \frac{Loadline}{gm \times DCR} \times \frac{R_{PHSP} + R_{th} + R_{CSSP}}{R_{th} + R_{CSSP}} \qquad \text{(eq. 18)}$$

Single−phase Rail − Programming the DAC Feed−Forward Filter

The DAC feed−forward implementation for the single−phase rail is the same as for the multi−phase rails. The NCP81212 outputs a pulse of current from the VSN pin upon each increment of the internal DAC following a DVID UP command. A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN. This causes the output voltage during DVID to be regulated slightly higher, in order to compensate for the response of the Droop function to the inductor current flowing into the charging output capacitors. RFFSP sets the gain of the DAC feed−forward and CFFSP provides the time constant to cancel the time constant of the system per the following equations. Cout is the total output capacitance of the system.

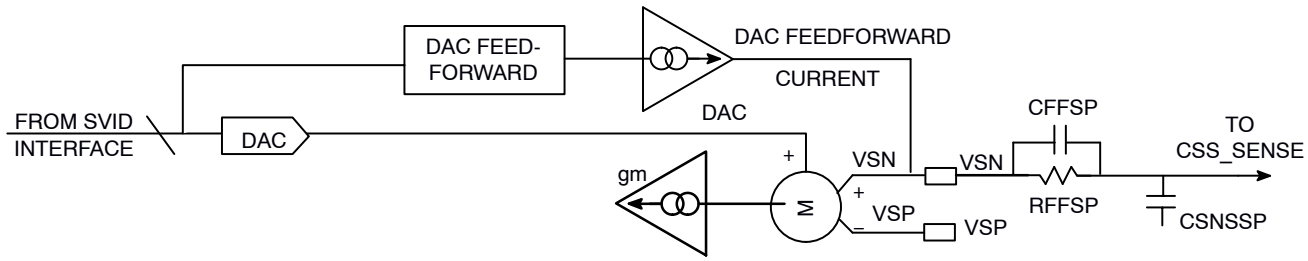


Figure 19.

$$R_{FFSP} = \frac{Loadline \times C_{out}}{1.35 \times 10^{-9}\ \Omega} \qquad C_{FFSP} = \frac{20}{R_{FFSP}\ nF} \qquad \text{(eq. 19)}$$

Single−phase Rail − Programming the Current Limit

The current limit threshold is programmed with a resistor (R_{ILIMSP}) from the ILIM pin to ground. The current limit latches the single−phase rail off immediately if the ILIM pin voltage exceeds the ILIM Threshold. Set the value of the current limit resistor based on the equation shown below. A capacitor can be placed in parallel with the programming resistor to slightly delay activation of the latch if some tolerance of short overcurrent events is desired.

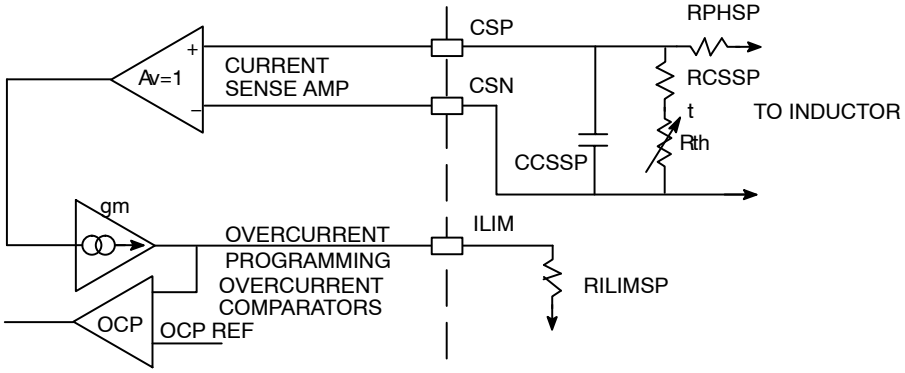


Figure 20.

$$R_{ILIMSP} = \frac{1.3\ V}{gm \times \frac{R_{th} + R_{CSSP}}{R_{PHSP} + R_{th} + R_{CSSP}} \times Iout_{LIMIT} \times DCR} \qquad \text{(eq. 20)}$$

When selecting the current limit it is necessary to take into account the additional inductor current due to the slew rate of the output voltage across the output capacitance during VID changes, as this excess current may cause the OCP limit to be exceeded. This excess current is given by:

$$I = Cout \times \frac{\delta Vout}{\delta t},\ \text{where}\ \frac{\delta Vout}{\delta t}\ \text{is the maximum slew rate} \qquad \text{(eq. 21)}$$

Single−phase Rail – Programming IOUT

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A pull−up resistor from 5 V VCC can be used to offset the IOUT signal positive if needed.

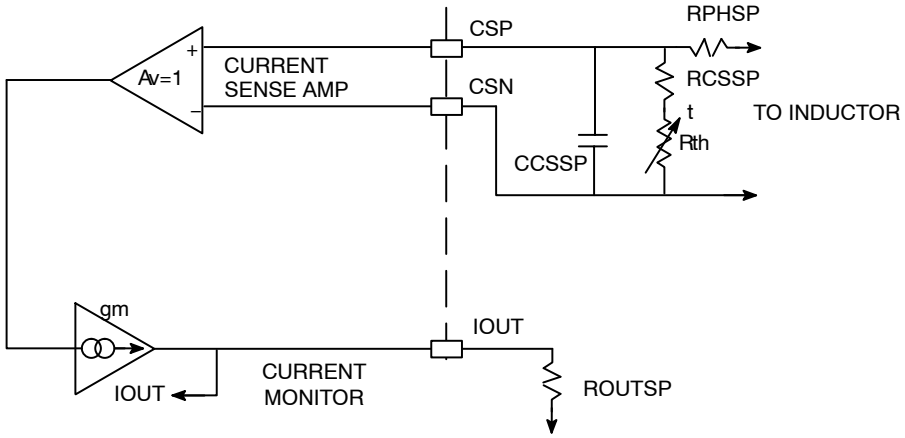


Figure 21.

$$R_{IOUTSP} = \frac{2\ V}{gm \times \frac{R_{th} + R_{CSSP}}{R_{PHSP} + R_{th} + R_{CSSP}} \times IccMax \times DCR} \quad \text{(eq. 22)}$$

Single−phase Rail PWM Comparator

A PWM pulse starts when the error amp signal (COMP voltage) rises above the trigger threshold plus gained−up inductor current, and stops when the artificial ramp plus gained−up inductor current crosses the COMP voltage. Both edges of the PWM signals are modulated. During a transient event, the duty cycle can increase rapidly as the COMP voltage increases with respect to the ramps, to provide a highly linear and proportional response to the step load.

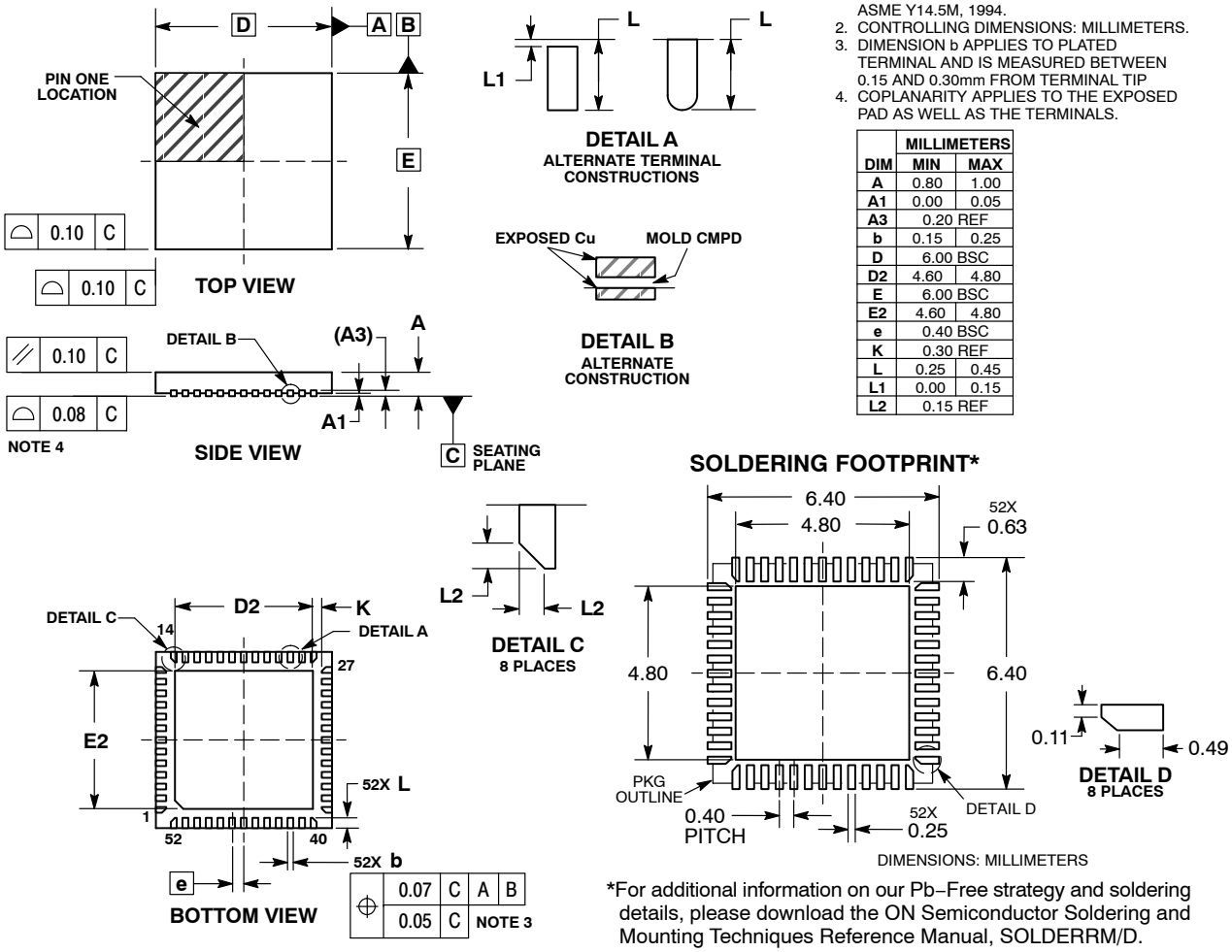
Programming ICC_MAX (single phase)

The SVID interface provides the platform ICC_MAX value at register 21h for. A resistor to ground on the IMAX pin programs these registers at the time the part is enabled. 10 μA is sourced from these pins to generate a voltage on the program resistor. The value of the register is 1A per LSB and is set by the equation below. The resistor value should be no less than 10 k.

$$ICC\_MAX_{21h} = \frac{Rmax \times 10\ \mu A \times 256\ A}{4 \times 2\ V} \quad \text{(eq. 23)}$$

PACKAGE DIMENSIONS

QFN52 6x6, 0.4P
CASE 485BE
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.60	4.80
E	6.00 BSC	
E2	4.60	4.80
e	0.40 BSC	
K	0.30 REF	
L	0.25	0.45
L1	0.00	0.15
L2	0.15 REF	

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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