

CD54AC74/3A CD54ACT74/3A

SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3$ ns, $C_L = 50$ pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays, CP to Q, \bar{Q}	t_{PLH} t_{PHL}	1.5	—	125	ns
		3.3* 5†	4.2 3	14 10•	
R, S to Q, \bar{Q}	t_{PLH}	1.5	—	132	ns
		3.3 5	4.4 3.15	14.7 10.5•	
	t_{PHL}	1.5	—	144	ns
		3.3 5	4.8 3.4	16.1 11.5•	
Power Dissipation Capacitance	$C_{PD}\S$	—	55 Typ.		pF
Input Capacitance	C_I	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3$ ns, $C_L = 50$ pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays, CP to Q, \bar{Q}	t_{PLH} t_{PHL}	5†	2.9	9.5•	ns
		\bar{R}, \bar{S} to Q	t_{PLH}	5	
t_{PHL}	5		3.8	12.5•	
Power Dissipation Capacitance	$C_{PD}\S$	—	55 Typ.		pF
Input Capacitance	C_I	—	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

(Limits with black dots (•) are tested 100%.)

§ C_{PD} is used to determine the dynamic power consumption, per flip-flop.

For AC, $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$

For ACT, $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC}\Delta I_{CC}$ where

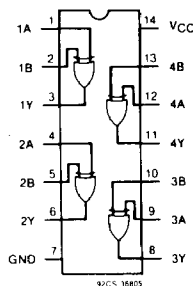
- f_i = input frequency
- f_o = output frequency
- C_L = output load capacitance
- C = supply voltage

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Quad 2-Input Exclusive-OR Gate

CD54AC86/3A CD54ACT86/3A

The RCA CD54AC86/3A and CD54ACT86/3A are quad 2-input Exclusive-OR gates that utilize the new RCA ADVANCED CMOS LOGIC technology. The CD54AC86/3A and CD54ACT86/3A are supplied in 14-lead dual-in-line ceramic packages (F suffix). The CD74AC86/3A and CD54ACT86/3A are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix).



Package Specifications

See Section 11, Fig. 10

FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

CD54AC86/3A CD54ACT86/3A

Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS	
	V _i (V)	I _o (mA)		+25		-55 to +125			
				MIN.	MAX.	MIN.	MAX.		
Quiescent Supply Current (SSI)	I _{CC}	V _{CC} or GND	0	5.5	—	4•	—	80•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
All	0.48

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V _{CC} (6V)	OPEN	GROUND	V _{CC} (6V)
CD54AC/ACT86	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
Dynamic	OPEN	GROUND	1/2 V _{CC} (3V)	V _{CC} (6V)	OSCILLATOR	
CD54AC/ACT86	—	7	3,6,8,11	14	50 kHz	25 kHz
					1,2,4,5,9,10,12,13	—

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V _{CC} (V)	-55 to +125° C		UNITS
			MIN.	MAX.	
Propagation Delay Input to Output	t _{PLH}	1.5	—	135	ns
	t _{PHL}	3.3*	2.8	18.9	
Power Dissipation Capacitance	C _{PD} §	—	57 Typ.		pF
Input Capacitance	C _i	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V _{CC} (V)	-55 to +125° C		UNITS
			MIN.	MAX.	
Propagation Delay Input to Output	t _{PLH} t _{PHL}	5†	2.5	14.6•	ns
Power Dissipation Capacitance	C _{PD} §	—	81 Typ.		pF
Input Capacitance	C _i	—	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption per gate.

For AC, P_D = V_{CC}² f_i (C_{PD} + C_L)

For ACT, P_D = V_{CC}² f_i (C_{PD} + C_L) + V_{CC} ΔI_{CC} where f_i = input frequency

C_L = output load capacitance
V_{CC} = supply voltage

(Limits with black dots (•) are tested 100%.)