SINGLE-CHIP CHARGE AND SYSTEM POWER-PATH MANAGEMENT IC (bqTINY™-III)

FEATURES

- **Small 3,5 mm × 4,5 mm QFN Package**
- **Designed for Single-Cell Li-Ion- or Li-Polymer-Based Portable Applications**
- **Integrated Dynamic Power-Path Management (DPPM) Feature Allowing the AC Adapter or the USB Port to Simultaneously Power the System and Charge the Battery**
- **Power Supplement Mode Allows Battery to Supplement the USB or AC Input Current**
- **Autonomous Power Source Selection (AC Adapter or USB)**
- **Integrated USB Charge Control With Selectable 100-mA and 500-mA Maximum Input Current Regulation Limits**
- **Dynamic Total Current Management for USB**
- **Supports Up to 2-A Total Current**
- **3.3-V Integrated LDO Output**
- **Thermal Regulation for Charge Control**
- **Charge Status Outputs for LED or System Interface Indicates Charge and Fault Conditions**
- **Reverse Current, Short-Circuit, and Thermal Protection**
- **Power Good (AC Adapter and USB Port Present) Status Outputs**
- **Charge Voltage Options: 4.2 V or 4.36 V**

APPLICATIONS

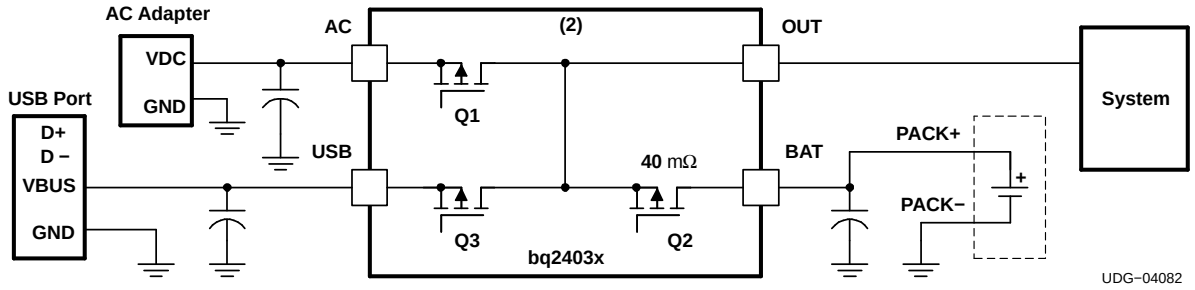
- **Smart Phones and PDA**
- **MP3 Players**
- **Digital Cameras Handheld Devices**
- **Internet Appliances**

DESCRIPTION

The bqTINY™-III series of devices are highly integrated Li-ion linear chargers and system power-path management devices targeted at space-limited portable applications. The bqTINY-III series offer integrated USB-port and DC supply (AC adapter), power-path management with autonomous power-source selection, power FETs and current sensors, high accuracy current and voltage regulation, charge status, and charge termination, in a single monolithic device.

The bqTINY-III powers the system while independently charging the battery. This feature reduces the charge and discharge cycles on the battery, allows for proper charge termination and allows the system to run with an absent or defective battery pack. This feature also allows for the system to instantaneously turn on from an external power source in the case of a deeply discharged battery pack. The IC design is focused on supplying continuous power to the system when available from the AC, USB, or battery sources.

POWER FLOW DIAGRAM (1)



(1) See Figure 2 and functional block diagram for more detailed feature information.

(2) P-FET back gate body diodes are disconnected to prevent body diode conduction.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOSFET gates.

DESCRIPTION (CONTINUED)

The power select pin, PSEL, defines which input source is to be used first (primary source – AC or USB). If the primary source is not available, then the IC automatically switches over to the other *secondary* source if available or the battery as the last option. If the PSEL is set low, the USB input is selected first and if not available, the AC line is selected (if available) but programmed to a USB input limiting rate (100 mA/500 mA max). This feature allows the use of one input connector, where the host programs the PSEL pin according to what source is connected (AC adaptor or USB port).

The bq24038 replaces $\overline{\text{USBPG}}$ with pin VBSEL, to enable user selection of the charge voltage. In addition, pin $\overline{\text{ACPG}}$ was modified to $\overline{\text{PG}}$. $\overline{\text{PG}}$ is active low when either ac power or USB power is detected.

The ISET1 pin programs the battery's fast charge constant current level with a resistor. During normal AC operation, the input supply provides power to both the OUT (System) and BAT pins. For peak or excessive loads (typically when operating from the USB power, PSEL = Low) that would cause the input source to enter current limit (or Q3 - USB FET limiting current) and its source and system voltage (OUT pin) to drop, the dynamic power-path management (DPPM) feature reduces the charging current attempting to prevent any further drop in system voltage. This feature allows the selection of a lower current rated adaptor based on the average load ($I_{SYS-AVG}$ + $I_{BAT-PGM}$) rather than a high peak transient load.

ORDERING INFORMATION(1)

T_A	BATTERY VOLTAGE (V)	OUT PIN FOR AC INPUT CONDITIONS	PART NUMBER(2)(3)	STATUS	PACKAGE MARKING
–40°C to 125°C	4.2	Regulated to 6 V(4)	bq24030RHLR	Released	ANB
	4.2	Regulated to 6 V(4)	bq24030RHLT	Preview	ANB
	4.2	Regulated to 4.4 V(4)	bq24032RHLR	Released	AMZ
	4.2	Regulated to 4.4 V(4)	bq24032ARHLR	Released	BPE
	4.2	Regulated to 4.4 V(4)	bq24032ARHLT	Released	BPE
	4.2	Cutoff for AC overvoltage(5)	bq24035RHLR	Released	ANA
	4.2	Cutoff for AC overvoltage(5)	bq24035RHLT	Preview	ANA
	4.2/4.36 Selectable	Regulated to 4.4 V	bq24038RHLR	Released	BOW
	4.2/4.36 Selectable	Regulated to 4.4 V	bq24038RHLT	Released	BOW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) The RHL package is available in the following options:
R - taped and reeled in quantities of 3,000 devices per reel.
T - taped and reeled in quantities of 250 devices per reel.
(3) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.
(4) If AC < $V_{O(OUT-REG)}$, the AC is connected to the OUT pin by a P-FET, (Q1).
(5) If AC > $V_{(CUT-OFF)}$ the P-FET disconnects the OUT pin from the AC.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		bq24030, bq24032, bq24032A, bq24035, bq24038
Input voltage	AC (DC voltage wrt (with respect to) VSS)	–0.3 V to 18 V
	USB (DC voltage wrt VSS)	–0.3 V to 7 V
Input voltage	BAT, CE, DPPM, $\overline{ACPG}$, PSEL, OUT, ISET1, ISET2, STAT1, STAT2, TS, $\overline{USBPG}$, $\overline{PG}$, VBSEL (all DC voltages wrt VSS)	–0.3 V to 7 V
	LDO (DC voltage wrt VSS)	–0.3 V to $V_{O(OUT)}$ + 0.3 V
	TMR	–0.3 V to $V_{O(LDO)}$ + 0.3 V
Input current	AC	3.5 A
	USB	1000 mA
Output current	OUT	4 A
	BAT(2)	–4 A to 3.5 A
Output source current (in regulation at 3.3 V LDO)	LDO	30 mA
Output sink current	$\overline{ACPG}$, STAT1, STAT2, $\overline{USBPG}$, $\overline{PG}$	1.5 mA
Storage temperature range, T_{stg}		–65°C to 150°C
Junction temperature range, T_J		–40°C to 150°C
Lead temperature (soldering, 10 seconds)		300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) Negative current is defined as current flowing into the BAT pin.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage (from AC input) (1)(2)	bq24030/2/2A/5, bq24038 (at VBSEL = LOW)	4.35	16	V
		bq24038 (at VBSEL = HIGH)	4.55	16	
V_{CC}	Supply voltage (from USB input) (1)		4.35	6	
I_{AC}	Input current, AC			2	A
I_{USB}	Input current, USB			0.5	
T_J	Operating junction temperature range		–40	125	°C

(1) V_{CC} is defined as the greater of AC or USB input.
(2) Verify that power dissipation and junction temperatures are within limits at maximum V_{CC} .

DISSIPATION RATINGS

PACKAGE	$T_A \le 40°C$ POWER RATING	DERATING FACTOR $T_A > 40°C$	θ_{JA}
20-pin RHL(1)	1.81 W	21 mW/°C	46.87 °C/W

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a 2×3 via matrix.

ELECTRICAL CHARACTERISTICS

over junction temperature range (0°C ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT BIAS CURRENTS							
$I_{CC(SPLY)}$	Active supply current, VCC		$V_{VCC} > V_{VCC(min)}$		1	2	mA
$I_{CC(SLP)}$	Sleep current (current into BAT pin)		$V_{(AC)} < V_{(BAT)}$, $V_{(USB)} < V_{(BAT)}$, 2.6 V ≤ $V_{I(BAT)}$ ≤ $V_{O(BAT-REG)}$, Excludes load on OUT pin		2	5	μA
$I_{CC(AS-STDBY)}$	AC standby current		$V_{I(AC)}$ ≤ 6V, Total current into AC pin with chip disabled, Excludes all loads, CE=LOW, after $t_{(CE-HOLDOFF)}$ delay			200	
$I_{CC(USB-STDBY)}$	USB standby current		Total current into USB pin with chip disabled, Excludes all loads, CE=LOW, after $t_{(CE-HOLDOFF)}$ delay			200	
$I_{CC(BAT-STDBY)}$	BAT standby current		Total current into BAT pin with AC and/or USB present and chip disabled; Excludes all loads (OUT and LDO), CE=LOW, after $t_{(CE-HOLDOFF)}$ delay, 0°C ≤ T_J ≤ 85°C (1)		45	60	
$I_{IB(BAT)}$	Charge done current, BAT		Charge DONE, AC or USB supplying the load		1	5	
HIGH AC CUTOFF MODE							
$V_{CUT-OFF}$	Input ac cutoff voltage, bq24035		$V_{I(AC)}$ > 6.8 V, AC FET (Q1) turns off, USB FET (Q3) turns on if USB power present, otherwise BAT FET (Q2) turns on.	6.1	6.4	6.8	V
LDO OUTPUT							
$V_{O(LDO)}$	Output regulation voltage		Active only if AC or USB is present, $V_{I(OUT)}$ ≥ $V_{O(LDO)}$ + ($I_{O(LDO)}$ × $R_{DS(on)}$)		3.3		V
	Regulation accuracy (2)			–5%		5%	
$I_{O(LDO)}$	Output current					20	mA
$R_{DS(on)}$	On resistance		OUT to LDO			50	Ω
$C_{(OUT)}$ (3)	Output capacitance					1	μF
OUT PIN-VOLTAGE REGULATION							
$V_{O(OUT-REG)}$	Output regulation voltage	bq24030	$V_{I(AC)}$ ≥ 6 V+V_{DO}		6.0	6.3	V
		bq24032/2A	$V_{I(AC)}$ ≥ 4.4 V+V_{DO}		4.4	4.5	
		bq24038	VBSEL = HIGH or VBSEL = LOW, $V_{I(AC)}$ > 4.4 V+V_{DO}		4.4	4.5	
OUT PIN – DPPM REGULATION							
$V_{(DPPM-SET)}$	DPPM set point (4)		$V_{DPPM-SET} < V_{OUT}$	2.6		5	V
$I_{(DPPM-SET)}$	DPPM current source		AC or USB present	95	100	105	μA
SF	DPPM scale factor		$V_{(DPPM-REG)}$ = $V_{(DPPM-SET)}$ × SF	1.139	1.150	1.162	

(1) This includes the quiescent current for the integrated LDO.
(2) In standby mode (CE low) the accuracy is ±10%.
(3) LDO output capacitor not required but one with a value of 0.1 μF is recommended.
(4) $V_{(DPPM-SET)}$ is scaled up by the scale factor for controlling the output voltage $V_{(DPPM-REG)}$.

ELECTRICAL CHARACTERISTICS (continued)

over junction temperature range (0°C ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT PIN – FET (Q1, Q3, AND Q2) DROP-OUT VOLTAGE (RDSon)						
$V_{(ACDO)}$	AC to OUT dropout voltage (5)	$V_{I(AC)} \geq V_{CC(min)}$, PSEL = High, $I_{I(AC)}$ = 1 A, ($I_{O(OUT)}$+ $I_{O(BAT)}$), or no AC		300	475	mV
$V_{(USBDO)}$ (6)	USB to OUT dropout voltage	$V_{I(USB)} \geq V_{CC(min)}$, PSEL = Low, ISET2 = High, $I_{I(USB)}$ = 0.4 A, ($I_{O(OUT)}$+$I_{O(BAT)}$), or no AC		140	180	mV
		$V_{I(USB)} \geq V_{CC(min)}$, PSEL = Low, ISET2 = Low, $I_{I(USB)}$ = 0.08 A, ($I_{O(OUT)}$+ $I_{O(BAT)}$)		28	36	mV
$V_{(BATDO)}$	BAT to OUT dropout voltage (discharging)	$V_{I(BAT)} \geq$ 3 V, $I_{I(BAT)}$= 1.0 A, $V_{CC} < V_{I(BAT)}$		40	100	mV
OUT PIN - BATTERY SUPPLEMENT MODE						
V_{BSUP1}	Enter battery supplement mode (battery supplements OUT current in the presence of input source	$V_{I(BAT)}$> 2 V	$V_{I(OUT)} \leq V_{I(BAT)}$ – 60 mV			V
V_{BSUP2}	Exit battery supplement mode	$V_{I(BAT)}$> 2 V			$V_{I(OUT)} \geq V_{I(BAT)}$ – 20 mV	V
OUT PIN - SHORT CIRCUIT						
I_{OSH1}	BAT to OUT short-circuit recovery	Current source between BAT to OUT for short-circuit recovery to $V_{I(OUT)} \leq V_{I(BAT)}$ –200 mV		10		mA
R_{SHAC}	AC to OUT short-circuit limit	$V_{I(OUT)} \leq$ 1 V		500		Ω
R_{SHVSB}	USB to OUT short-circuit limit	$V_{I(OUT)} \leq$ 1 V		500		Ω
BAT PIN CHARGING – PRECHARGE						
$V_{(LOWV)}$	Precharge to fast-charge transition threshold	Voltage on BAT	2.9	3	3.1	V
$T_{DGL(F)}$	Deglitch time for fast-charge to precharge transition (7)	t_{FALL} = 100 ns, 10 mV overdrive, $V_{I(BAT)}$ decreasing below threshold		22.5		ms
$I_{O(PRECHG)}$	Precharge range	1 V < $V_{I(BAT)}$ < $V_{(LOWV)}$, t < $t_{(PRECHG)}$, $I_{O(PRECHG)}$ = ($K_{(SET)}$ × $V_{(PRECHG)}$)/ R_{SET}	10		150	mA
$V_{(PRECHG)}$	Precharge set voltage	1 V < $V_{I(BAT)}$ < $V_{(LOWV)}$, t < $t_{(PRECHG)}$	230	250	270	mV
BAT PIN CHARGING - CURRENT REGULATION						
$I_{O(BAT)}$	AC battery charge current range (8)	$V_{I(BAT)}$ > $V_{(LOWV)}$, $V_{I(OUT)}$ - $V_{I(BAT)}$ > $V_{(DO-MAX)}$, PSEL = High $I_{OUT(BAT)}$ = ($K_{(SET)}$ × $V_{(SET)}$ / R_{SET}), V_I(OUT) > V_O(OUT-REG) + $V_{(DO-MAX)}$	100	1000	1500	mA
R_{PBAT}	BAT to OUT pullup	$V_{I(BAT)}$< 1 V		1000		Ω
R_{POUT}	AC to OUT and USB to OUT short-circuit pullup	$V_{I(OUT)}$ < 1 V		500		Ω
$V_{(SET)}$	Battery charge current set voltage (9)	Voltage on ISET1, $V_{VCC} \geq$ 4.35 V, $V_{I(OUT)}$- $V_{I(BAT)}$ > $V_{(DO-MAX)}$, $V_{I(BAT)}$ > $V_{(LOWV)}$	2.475	2.500	2.525	V
$K_{(SET)}$	Charge current set factor, BAT	100 mA ≤ $I_{O(BAT)}$ ≤ 1 A	400	425	450	
		10 mA ≤ $I_{O(BAT)}$ ≤ 100 mA (10)	300	450	600	

(5) $V_{DO(max)}$, dropout voltage is a function of the FET, $R_{DS(on)}$, and drain current. The dropout voltage increases proportionally to the increase in current.
(6) $R_{DS(on)}$ of USB FET Q3 is calculated by: (V_{USB} – V_{OUT}) / (I_{OUT} + I_{BAT}) when $I_{I(USB)} \leq I_{I(USB-MIN)}$ (FET fully on, not in regulation).
(7) All deglitch periods are a function of the timer setting and is modified in DPPM or thermal regulation modes by the percentages that the program current is reduced.
(8) When input current remains below 2 A, the battery charging current may be raised until the thermal regulation limits the charge current.
(9) For half-charge rate, $V_{(SET)}$ is 1.25 V ± 25 mV for bq24032/32A/38 only.
(10) Specification is for monitoring charge current via the ISET1 pin during voltage regulation mode, not for a reduced fast-charge level.

ELECTRICAL CHARACTERISTICS (continued)

over junction temperature range (0°C ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB PIN INPUT CURRENT REGULATION							
$I_{(USB)}$	USB input current range, bq24030/2/2A/5/8 (11)		$V_{I(BAT)} > V_{(LOWV)}$, $V_{I(USB)} - V_{I(BAT)} > V_{(DO-MAX)}$, ISET2= Low, PSEL = Low, or no AC (12)			100	mA
			$V_{I(BAT)} > V_{(LOWV)}$, $V_{I(USB)} - V_{I(BAT)} > V_{(DO-MAX)}$, ISET2= High, PSEL = Low, or no AC (11)	400		500	
BAT PIN CHARGING VOLTAGE REGULATION, $V_{O\ (BAT-REG)} + V_{(DO-MAX)} < V_{CC}$, $I_{TERM} < I_{BAT(OUT)} \leq 1$ A							
$V_{O(BAT-REG)}$	Battery charge voltage	bq24030/2/2A/5			4.2		V
		bq24038	VBSEL = HI		4.36		
			VBSEL = LO		4.2		
	Battery charge voltage regulation accuracy		T_A = 25°C	–0.5%		0.5%	
				–1%		1%	
CHARGE TERMINATION DETECTION							
$I_{(TERM)}$	Charge termination detection range		$V_{I(BAT)} < V_{(RCH)}$, $I_{(TERM)} = (K_{(SET)} \times V_{(TERM)}) / R_{SET}$	10		150	mA
$V_{(TERM-AC/USB)}$ bq24032	Charge termination set voltage, measured on ISET1		$V_{I(BAT)} > V_{(RCH)}$	235	250	265	mV
$V_{(TERM-AC)}$ bq24030/2A/5/8	AC-charge termination detection voltage, measured on ISET1		$V_{I(BAT)} > V_{(RCH)}$, PSEL = High, $\overline{ACPG}$ = Low	235	250	265	mV
$V_{(TAPER-USB)}$ bq24030/2A/5/8	USB-charge termination detection voltage, measured on ISET1		$V_{I(BAT)} > V_{(RCH)}$, $\overline{PSEL}$ = Low or PSEL = High and $\overline{ACPG}$ = High	95	100	130	mV
$T_{DGL(TERM)}$	Deglitch time for termination detection		t_{FALL} = 100 ns, 10 mV overdrive, I_{CHG} increasing above or decreasing below threshold		22.5		ms
TEMPERATURE SENSE COMPARATORS							
V_{LTF}	High voltage threshold		Temp fault at V(TS) > V_{LTF}	2.465	2.500	2.535	V
V_{HTF}	Low voltage threshold		Temp fault at V(TS) < V_{HTF}	0.485	0.500	0.515	V
I_{TS}	Temperature sense current source			94	100	106	µA
$T_{DGL(TF)}$	Deglitch time for temperature fault detection (13)		$R_{(TMR)}$ = 50 kΩ, $V_{I(BAT)}$ increasing or decreasing above and below; 100-ns fall time, 10-mv overdrive		22.5		ms
BATTERY RECHARGE THRESHOLD							
V_{RCH}	Recharge threshold voltage			$V_{O(BAT-REG)}$ –0.075	$V_{O(BAT-REG)}$ –0.100	$V_{O(BAT-REG)}$ –0.125	V
$T_{DGL(RCH)}$	Deglitch time for recharge detection (13)		$R_{(TMR)}$ = 50 kΩ, $V_{I(BAT)}$ increasing or decreasing below threshold, 100-ns fall time, 10-mv overdrive		22.5		ms

(11) With the PSEL= low, the bqTINY-III defaults to USB charging. If USB input is ≤ V_{BAT}, then the bqTINY-III charges from the AC input at the USB charge rate. In this configuration, the specification is 400 mA (min) and 500 mA (max) for bq24030/2A/5/8 only; and 350 mA (min) and 500 mA (max) for bq24032.

(12) With the PSEL= low, the bqTINY-III defaults to USB charging. If USB input is ≤ V_{BAT}, then the bqTINY-III charges from the AC input at the USB charge rate. In this configuration, the specification is 80 mA (min) and 100 mA (max) for bq24030/2A/5/8 only; 75 mA (min) and 100 mA (max) for bq24032.

(13) All deglitch periods are a function of the timer setting and is modified in DPPM or thermal regulation modes by the percentages that the program current is reduced.

ELECTRICAL CHARACTERISTICS (continued)

over junction temperature range (0°C ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STAT1, STAT2. $\overline{ACPG}$ AND $\overline{USBPG}$, $\overline{PG}$ OPEN DRAIN (OD) OUTPUTS(14)						
V_{OL}	Low-level output saturation voltage	I_{OL} = 5 mA, An external pullup resistor ≥ 1 K required.			0.25	V
I_{LKG}	Input leakage current			1	5	µA
ISET2, CE, VBSEL INPUTS						
V_{IL}	Low-level input voltage		0		0.4	V
V_{IH}	High-level input voltage		1.4			V
I_{IL}	Low-level input current, CE		–1			µA
I_{IH}	High-level input current, CE				1	µA
I_{IL}	Low-level input current, ISET2	V_{ISET2} = 0 V	–20			µA
I_{IH}	High-level input current, ISET2	V_{ISET2} = V_{CC}			40	µA
I_{IL1}	Low-level input current	VBSEL = Low	6		1	µA
I_{IH1}	High-level input current	VBSEL = High			15	µA
$t_{(CE-HLDOFF)}$	Holdoff time, CE	CE going low only	4		6	ms
PSEL INPUT						
V_{IL}	Low-level input voltage	Falling Hi→Low; 280 K ± 10% applied when low. (bq24030/2A/5/8)	0.975	1	1.025	V
		(bq24032 only)	0		0.4	V
V_{IH}	High-level input voltage	Input R_{PSEL} sets external hysteresis (bq24030/2A/5/8)	V_{IL} + .01		V_{IL} + .024	V
		(bq24032 only)	1.4			V
I_{IL}	Low-level input current, PSEL		–1			µA
I_{IH}	High-level input current, PSEL					µA
TIMERS						
$K_{(TMR)}$	Timer set factor	$t_{(CHG)}$ = $K_{(TMR)}$ × $R_{(TMR)}$	0.313	0.360	0.414	s/Ω
$R_{(TMR)}$(15)	External resistor limits		30		100	kΩ
$t_{(PRECHG)}$	Precharge timer		0.09 × $t_{(CHG)}$	0.10 × $t_{(CHG)}$	0.11 × $t_{(CHG)}$	s
$I_{(FAULT)}$	Timer fault recovery pullup from OUT to BAT			1		kΩ
CHARGER SLEEP THRESHOLDS ($\overline{ACPG}$, $\overline{PG}$, and $\overline{USBPG}$ THRESHOLDS, LOW → POWER GOOD)						
$V_{(SLPENT)}$(16)	Sleep-mode entry threshold	$V_{(UVLO)}$≤ $V_{I(BAT)}$≤ $V_{O(BAT-REG)}$, No $t_{(BOOT-UP)}$ delay			V_{VCC} ≤ $V_{I(BAT)}$ +125 mV	V
$V_{(SLPEXIT)}$(16)	Sleep-mode exit threshold	$V_{(UVLO)}$≤ $V_{I(BAT)}$≤ $V_{O(BAT-REG)}$, No $t_{(BOOT-UP)}$ delay	V_{VCC} ≥ $V_{I(BAT)}$ +190 mV			V
$t_{(DEGL)}$	Deglitch time for sleep mode(17)	$R_{(TMR)}$ = 50 kΩ, $V_{(AC)}$ or $V_{(USB)}$ or decreasing below threshold, 100-ns fall time, 10-mv overdrive		22.5		ms
START-UP CONTROL and USB BOOT-UP						
$t_{(BOOT-UP)}$	Boot-up time	On the first application of USB input power or AC input with PSEL Low	120	150	180	ms

(14) See Charger Sleep mode for $\overline{ACPG}$ (V_{CC} = V_{AC}) and $\overline{USBPG}$ (V_{CC} = V_{USB}) specifications.
(15) To disable the safety timer and charge termination, tie TMR to the LDO pin.
(16) The IC is considered in sleep mode when both AC and USB are absent ($\overline{ACPG}$ = $\overline{USBPG}$ = OPEN DRAIN).
(17) Does not declare sleep mode until after the deglitch time and implement the needed power transfer immediately according to the switching specification.

ELECTRICAL CHARACTERISTICS (continued)

over junction temperature range (0°C ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

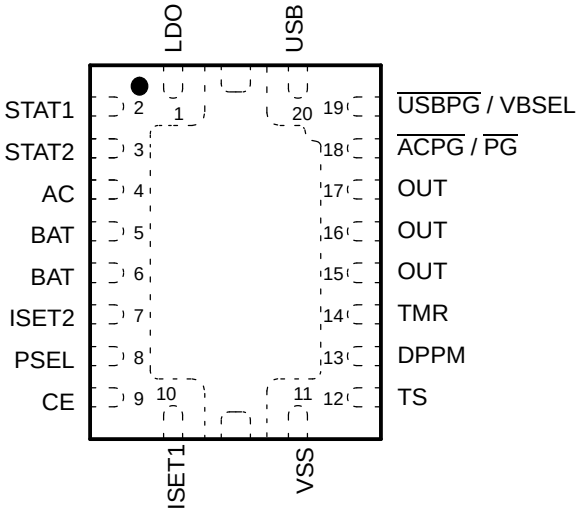
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING POWER SOURCE TIMING						
t_{SW-BAT}	Switching power source from inputs (AC or USB) to battery	Only AC power or USB power applied. Measure from: [xx$\overline{PG}$: Lo → Hi to I(xx) > 5 mA], xx = AC or USB I(OUT) = 100 mA, R_{TRM} = 50 K			50	µs
$t_{SW-AC/USB}$	Switching from AC to USB, or, USB to AC by input source removal. (18)	Measure from: I(AC) < 5 mA to I(USB) > 5 mA or I(USB) < 5 mA → I(AC) > 5 mA; I(OUT) = 100 mA, R_{TMR} = 50 K, ISET2 = hi, R_{OUT} > 15 Ω, V_{DPPM} = 2.5 V			100	
$t_{SW-PSEL}$	Switching from AC to USB, or USB to AC by toggling PSEL, bq24030/2/2A/5/8 only			50	100	
THERMAL SHUTDOWN REGULATION (19)						
$T_{(SHTDWN)}$	Temperature trip	T_J (Q1 and Q3 only)		155		°C
	Thermal hysteresis	T_J (Q1 and Q3 only)		30		
$T_{J(REG)}$	Temperature regulation limit	T_J (Q2)	115		135	
UVLO						
$V_{(UVLO)}$	Undervoltage lockout	Decreasing V_{CC}	2.45	2.50	2.65	V
	Hysteresis			27		mV

(18) The power handoff is implemented once the $\overline{PG}$ pin goes high (removed sources PG) which is when the removed source drops to the battery voltage. If the battery voltage is critically low, the system may lose power unless the system takes control of the PSEL pin and switches to the available power source prior to shutdown. The USB source often has less current available; so, the system may have to reduce its load when switching from AC to USB (bq24030/2/2A/5/8).

(19) Reaching thermal regulation reduces the charging current. Battery supplement current is not restricted by either thermal regulation or shutdown. Input power FETs turn off during thermal shutdown. The battery FET is only protected by a short-circuit limit which typically does not cause a thermal shutdown (input FETs turning off) by itself.

DEVICE INFORMATION

bq24030RHL – bq24038RHL
RHL PACKAGE
(TOP VIEW)

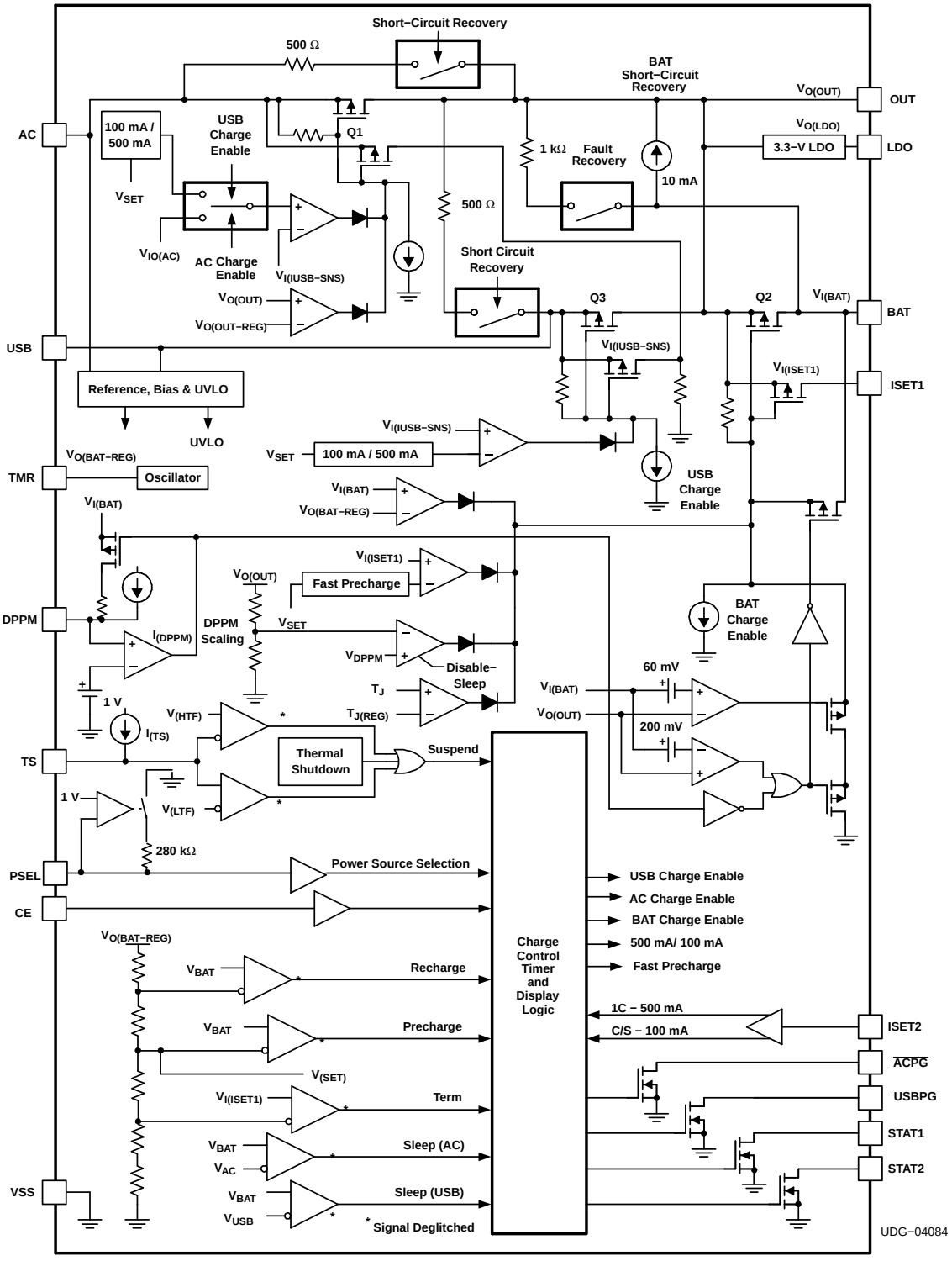


TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AC	4	I	Charge input voltage from AC adapter
$\overline{\text{ACPG}}$ (1)	18	O	AC power-good status output (open-drain)
BAT	5, 6	I/O	Battery input and output.
CE	9	I	Chip enable input (active high)
DPPM	13	I	Dynamic power-path management set point (account for scale factor)
ISET1	10	I/O	Charge current set point for AC input and precharge and termination set point for both AC and USB
ISET2	7	I	Charge current set point for USB port. (High = 500 mA, Low = 100 mA) For bq24032, see half-charge current mode using ISET2.
LDO	1	O	3.3-V LDO regulator
OUT	15, 16, 17	O	Output terminal to the system
$\overline{\text{PG}}$ (1)	18	O	AC or USB power-good status output (open-drain)
PSEL	8	I	Power source selection input (Low for USB, High for AC)
STAT1	2	O	Charge status output 1 (open-drain)
STAT2	3	O	Charge status output 2 (open-drain)
TMR	14	I/O	Timer program input programmed by resistor. Disable safety timer and termination by tying TMR to LDO.
TS	12	I/O	Temperature sense input
USB	20	I	USB charge input voltage
$\overline{\text{USBPG}}$ (2)	19	O	USB power-good status output (open-drain)
VBSEL (2)	19	I	Battery charge voltage selection
VSS	11	–	Ground input (the thermal pad on the underside of the package) There is an internal electrical connection between the exposed thermal pad and VSS pin of the device. The exposed thermal pad must be connected to the same potential as the VSS pin on the printed-circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

(1) Pin 18 is $\overline{\text{PG}}$ for bq24038 and $\overline{\text{ACPG}}$ for bq24030/2/2A/5.
(2) Pin 19 is VBSEL for bq24038 and $\overline{\text{USBPG}}$ for bq24030/2/2A/5.

FUNCTIONAL BLOCK DIAGRAM FOR bq24030/2/5 ONLY (1)



(1) For bq24038 see *bq24038 Differences* in the *Functional Descriptions* section.

FUNCTIONAL DESCRIPTIONS

CHARGE CONTROL

The bqTINY-III supports a precision Li-ion or Li-polymer charging system suitable for single-cell portable devices. See a typical charge profile, application circuit, and an operational flow chart in Figure 1 through Figure 4, respectively.

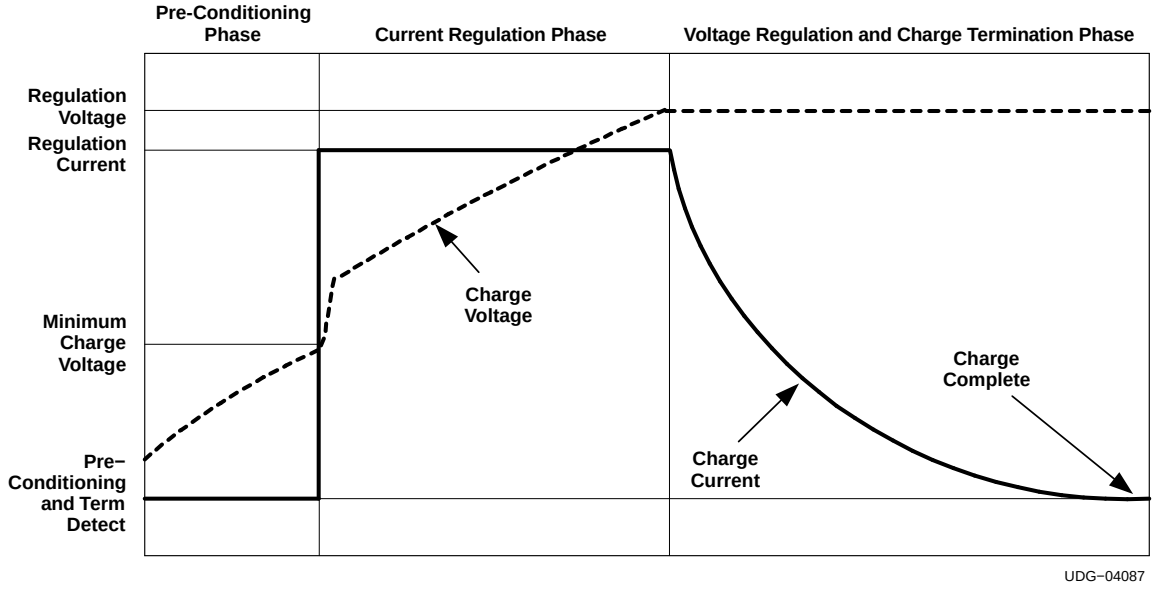


Figure 1. Charge Profile

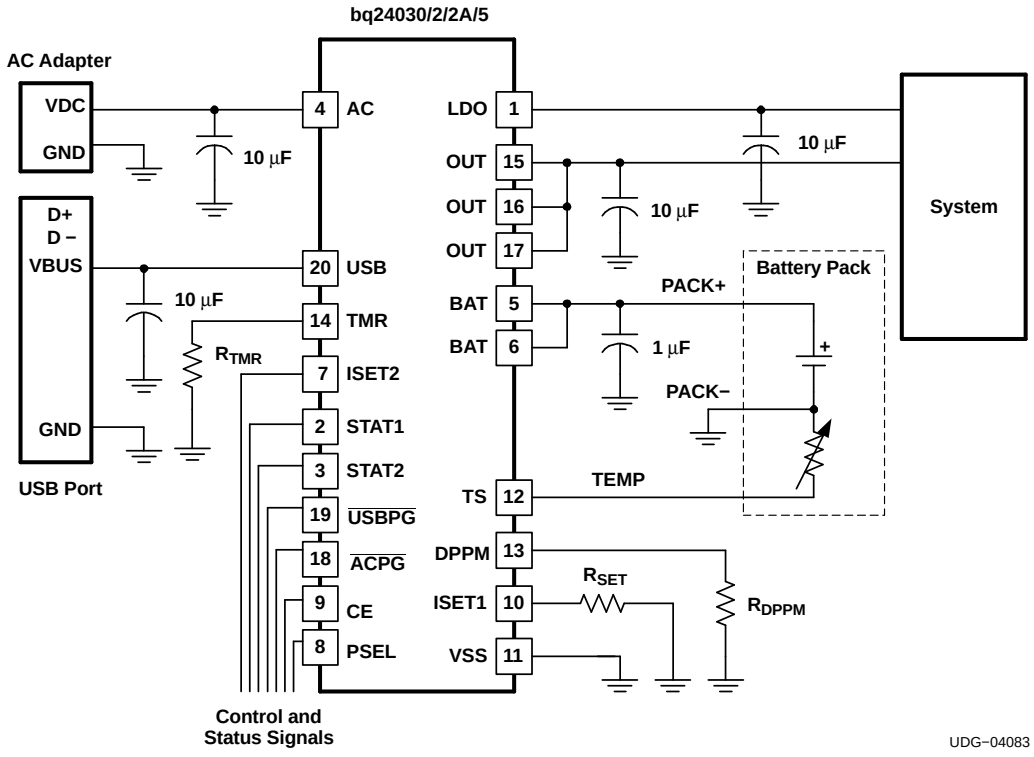


Figure 2. Typical Application Circuit

FUNCTIONAL DESCRIPTIONS (continued)

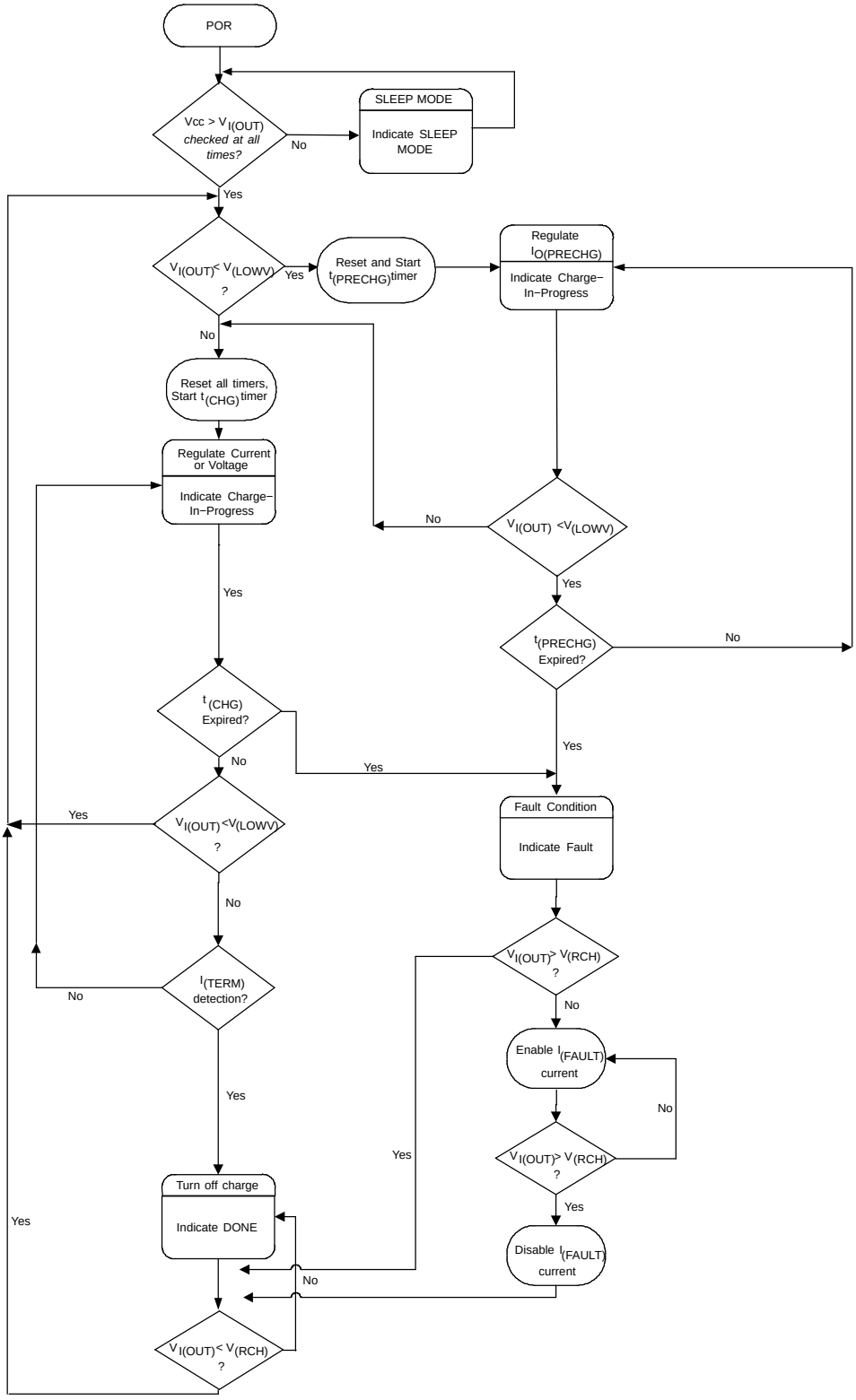


Figure 3. Charge Control Operational Flow Chart

FUNCTIONAL DESCRIPTIONS (continued)

bq24038 Differences

The bq24038 replaces $\overline{\text{USBPG}}$ with pin VBSEL, to enable user selection of the charge voltage. In addition, pin $\overline{\text{ACPG}}$ was modified to $\overline{\text{PG}}$. $\overline{\text{PG}}$ is active low when either ac power or USB power is detected.

Autonomous Power Source Selection, PSEL Control Pin

The PSEL pin selects the priority of the input sources (high = AC, low = USB), if that primary source is not available (based on $\overline{\text{ACPG}}$, $\overline{\text{USBPG}}$ signal), then it uses the secondary source. If neither input source is available, then the battery is selected as the source. With the PSEL input high, the bqTINY-III attempts to charge from the AC input. If AC input is not present, the USB is selected. If both inputs are available, the AC adapter has priority. With the PSEL input low, the bqTINY-III defaults to USB charging. If USB input is grounded, then the bqTINY-III charges from the AC input at the USB charge rate (as selected by ISET2). This feature can be used in system where AC and USB power source selection is done elsewhere. The PSEL function is summarized in Table 1.

Table 1. Power Source Selection Function Summary

PSEL STATE	AC	USB	CHARGE SOURCE	MAXIMUM CHARGE RATE(1)	SYSTEM POWER SOURCE	USB BOOT-UP FEATURE
Low	Present(2)	Absent	AC	ISET2	AC	Enabled
	Absent(3)	Present	USB	ISET2	USB	Enabled
	Present	Present	USB	ISET2	USB	Enabled
	Absent	Absent	N/A	N/A	Battery	Disabled
High	Present	Absent	AC	ISET1	AC	Disabled
	Absent	Present	USB	ISET2	USB	Disabled
	Present	Present	AC	ISET1	AC	Disabled
	Absent	Absent	N/A	N/A	Battery	Disabled

(1) Battery charge rate is always set by ISET1, but may be reduced by a limited input source (ISET2 USB mode) and I_{OUT} system load.
(2) *Present* is defined as input being at a higher voltage than the BAT voltage (sources power good is low).
(3) *AC Absent* is defined as AC input not present ($\overline{\text{ACPG}}$ is High) or Q1 turned off due to overvoltage in bq24035.

Boot-Up Sequence

In order to facilitate the system start-up and USB enumeration, the bqTINY-III offers a proprietary boot-up sequence. On the first application of power to the bqTINY-III, this feature enables the 100-mA USB charge rate for a period of approximately 150 ms, ($t_{(BOOT-UP)}$), ignoring the ISET2 and CE inputs setting. At the end of this period, the bqTINY-III implements CE and ISET2 inputs settings. Table 1 indicates when this feature is enabled. See Figure 13.

Power-Path Management

The bqTINY-III powers the system while independently charging the battery. This features reduces the charge and discharge cycles on the battery, allows for proper charge termination, and allows the system to run with an absent or defective battery pack. This feature gives the system priority on input power, allowing the system to power up with a deeply discharged battery pack. This feature works as follows (note that PSEL is assumed HIGH for this discussion).

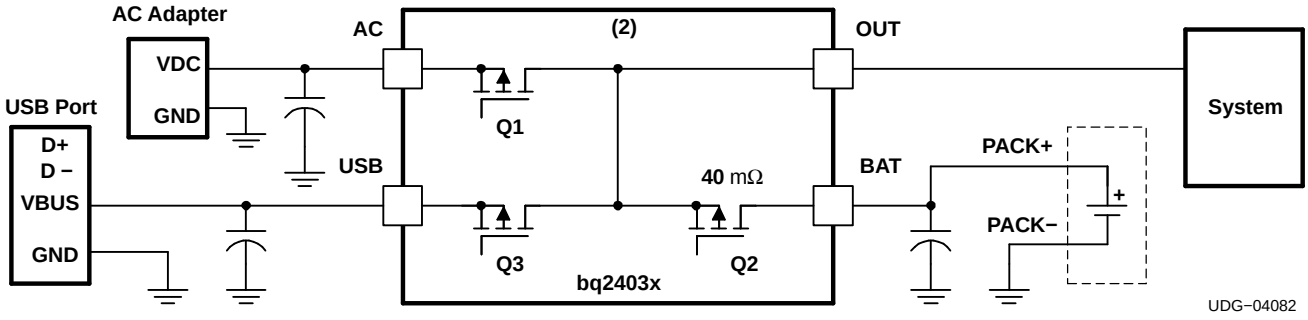


Figure 4. Power-Path Management

Case 1: AC Mode (PSEL = High)

System Power

In this case, the system load is powered directly from the AC adapter through the internal transistor Q1 (see Figure 4). For bq24030, Q1 acts as a switch as long as the AC input remains at or below 6 V ($V_{O(OUT-REG)}$). Once the AC voltage goes above 6 V, Q1 starts regulating the output voltage at 6 V. For bq24035, once the AC voltage goes above $V_{CUT-OFF}$ (~6.4 V), Q1 turns off. For bq24032/2A/8, the output is regulated at 4.4 V from the AC input. Note that switch Q3 is turned off for both devices. If the system load exceeds the capacity of the supply, the output voltage drops down to the battery's voltage.

Charge Control

When AC is present, the battery is charged through switch Q2 based on the charge rate set on the ISET1 input.

Dynamic Power-Path Management (DPPM)

This feature monitors the output voltage (system voltage) for input power loss due to brown outs, current limiting, or removal of the input supply. If the voltage on the OUT pin drops to a preset value, $V_{(DPPM)} \times SF$, due to a limited amount of input current, then the battery charging current is reduced until the output voltage stops dropping. The DPPM control tries to reach a steady-state condition where the system gets its needed current and the battery is charged with the remaining current. No active control limits the current to the system; therefore, if the system demands more current than the input can provide, the output voltage drops just below the battery voltage and Q2 turns on which supplements the input current to the system. DPPM has three main advantages.

1. This feature allows the designer to select a lower power wall adapter, if the average system load is moderate compared to its peak power. For example, if the peak system load is 1.75 A, average system load is 0.5 A and battery fast-charge current is 1.25 A, the total peak demand could be 3 A. With DPPM, a 2-A adaptor could be selected instead of a 3.25-A supply. During the system peak load of 1.75 A and charge load of 1.25 A, the smaller adaptor's voltage drops until the output voltage reaches the DPPM regulation voltage threshold. The charge current is reduced until there is no further drop on the output voltage. The system gets its 1.75-A charge and the battery charge current is reduced from 1.25 A to 0.25 A. When the peak system load drops to 0.5 A, the charge current returns to 1 A and the output voltage returns to its normal value.
2. Using DPPM provides a power savings compared to configurations without DPPM. Without DPPM, if the system current plus charge current exceed the supply's current limit, then the output is pulled down to the battery. Linear chargers dissipate the unused power $(V_{IN}-V_{OUT}) \times I_{LOAD}$. The current remains high (at current limit) and the voltage drop is large for maximum power dissipation. With DPPM, the voltage drop is less $(V_{IN}-V_{(DPPM-REG)})$ to the system which means better efficiency. The efficiency for charging the battery is the same for both cases. The advantages include less power dissipation, lower system temperature, and better overall efficiency.
3. The DPPM sustains the system voltage no matter what causes it to drop, if at all possible. It does this by reducing the noncritical charging load while maintaining the maximum power output of the adaptor.

   Note that the DPPM voltage, $V_{(DPPM)}$, is programmed as follows:

$$V_{(DPPM)} = I_{(DPPM)} \times R_{(DPPM)} \times SF \quad (1)$$

where

$R_{(DPPM)}$ is the external resistor connected between the DPPM and VSS pins.

$I_{(DPPM)}$ is the internal current source.

SF is the scale factor as specified in the specification table.

The safety timer is dynamically adjusted while in DPPM mode. The voltage on the ISET1 pin is directly proportional to the programmed charging current. When the programmed charging current is reduced, due to DPPM, the ISET1 and TMR voltages are reduced and the timer's clock is proportionally slowed, extending the safety time. In normal operation, V(TMR) = 2.5 V, when the clock is slowed the voltage V(TMR) us reduced, Wgeb V(TMR) = 1.25 V, the safety timer has a value close to 2 times the normal operation timer value. See Figure 5 through Figure 8.

Case 2: USB (PSEL = Low) bq24030/2/2A/8

System Power

In this case, the system load is powered directly from the USB port through the internal switch Q3 (see Figure 14). Note in this case, Q3 regulates the total current to the 100 mA or 500 mA level, as selected on the ISET2 input. Switch Q1 is turned off in this mode. If the system and battery load is less than the selected regulated limit, then Q3 is fully on and V_{OUT} is approximately ($V_{(USB)}$-$V_{(USB-DO)}$). The systems power management is responsible for keeping its system load below the USB current level selected (if the battery is critically low or missing). Otherwise, the output drops to the battery voltage; therefore, the system should have a low power mode for USB power application. The DPPM feature keeps the output from dropping below its programmed threshold, due to the battery charging current, by reducing the charging current.

Charge Control

When USB is present and selected, Q3 regulates the input current to the value selected by the ISET2 pin (0.1/0.5 A). The charge current to the battery is set by the ISET1 resistor (typically > 0.5 A). Because the charge current typically is programmed for more current than Q3 allows, the output voltage drops to the battery voltage or DPPM voltage, whichever is higher. If the DPPM threshold is reached first, the charge current is reduced until V_{OUT} stops dropping. If V_{OUT} drops to the battery voltage, the battery is able to supplement the input current to the system.

Dynamic Power-Path Management (DPPM)

The theory of operation is the same as described in CASE 1, except that Q3 restricts the amount of input current delivered to the output and battery instead of the input supply.

Note that the DPPM voltage, $V_{(DPPM)}$, is programmed as follows:

$$V_{(DPPM)} = I_{(DPPM)} \times R_{(DPPM)} \times SF \quad (2)$$

where

$R_{(DPPM)}$ is the external resistor connected between the DPPM and VSS pins.

$I_{(DPPM)}$ is the internal current source.

SF is the scale factor as specified in the specification table.

Feature Plots

Figure 5 illustrates DPPM and battery supplement modes as the output current (I_{OUT}) is increased; channel 1 (CH1) VAC = 5.4 V; channel 2 (CH2) V_{OUT}; channel 3 (CH3) I_{OUT} = 0 to 2.2 A to 0 A; channel 4 (CH4) V_{BAT} = 3.5 V; $I_{(PGM-CHG)}$ = 1 A. In typical operation, bq24032 (V_{OUT} = 4.4 V_{reg}), through an AC adaptor overload condition and recovery. The AC input is set for ~5.1 V (1.5 A current limit), $I_{(CHG)}$ = 1 A, $V_{(DPPM-SET)}$ = 3.7 V, $V_{(DPPM-OUT)}$ = 1.15 × $V_{(DPPM-SET)}$ = 4.26 V, V_{BAT} = 3.5 V, PSEL = H, and USB input is not connected. The output load is increased from 0 A to ~2.2 A and back to 0 A as shown in the bottom waveform. As the I_{OUT} load reaches 0.5 A, along with the 1-A charge current, the adaptor starts to current limit, the output voltage drops to the DPPM-OUT threshold of 4.26 V. This is DPPM mode. The AC input tracks the output voltage by the dropout voltage of the AC FET. The battery charge current is then adjusted back as necessary to keep the output voltage from falling any further.

Once the output load current exceeds the input current, the battery has to supplement the excess current and the output voltage falls just below the battery voltage by the dropout voltage of the battery FET. This is the battery supplement mode. When the output load current is reduced, the operation described is reversed as shown. If the DPPM-OUT voltage was set below the battery voltage, during input current limiting, the output falls directly to the battery's voltage.

Under USB operation, when the loads exceeds the programmed input current thresholds a similar pattern is observed. If the output load exceeds the available USB current, the output instantly goes into the battery supplement mode.

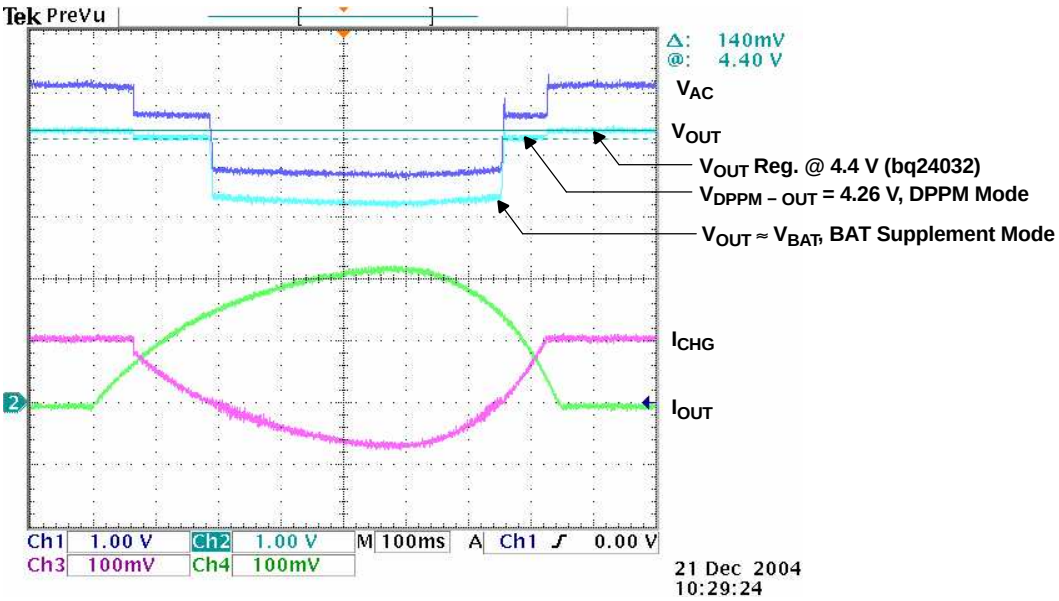


Figure 5. DPPM and Battery Supplement Modes

Figure 6 illustrates when PSEL is toggled low for 500 µs. Power transfers from AC to USB to AC; channel 1 (CH1) VAC = 5.4 V; channel 2 (CH2) $V_{(USB)}$ = 5 V; channel 3 (CH3) V_{OUT}; output current, I_{OUT} = 0.25 A; channel 4 (CH4) V_{BAT} = 3.5 V; and $I_{(PGM-CHG)}$ = 1 A. When the PSEL went low (1st div), the AC FET opened, and the output fell until the USB FET turned on. Turning off the active source before turning on the replacement source is referred to as *break-before-make* switching. The rate of discharge on the output is a function of system capacitance and load. Note the cable IR drop in the AC and USB inputs when they are under load. At the 4th division, the output has reached steady-state operation at the DPPM voltage level (charge current has been reduced due to the limited USB input current). At the 6th division, the PSEL goes high and the USB FET turns off followed by the AC FET turning on. The output returns to its regulated value, and the battery returns to its programmed current level.

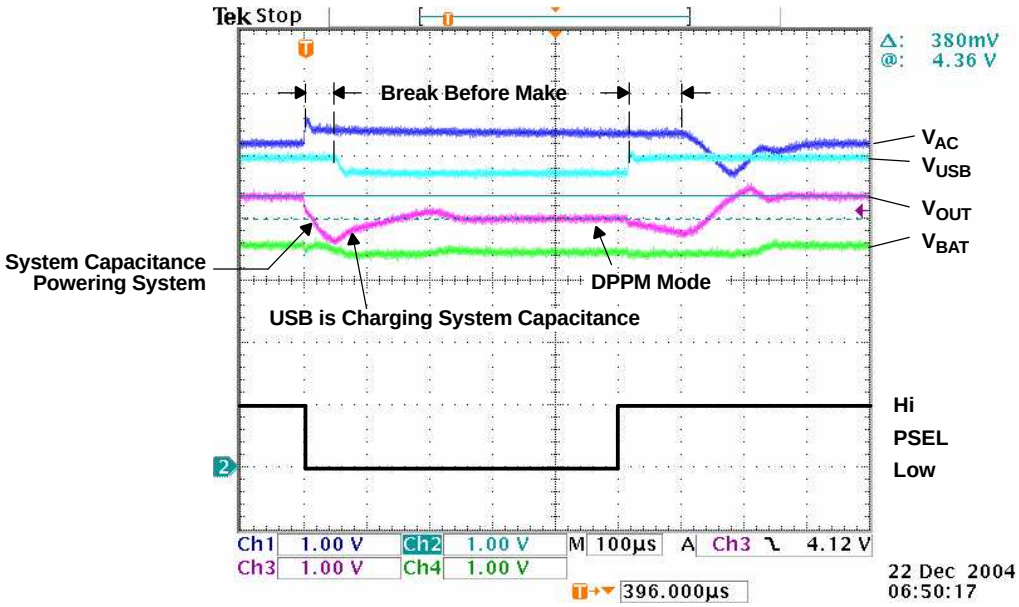


Figure 6. Toggle PSEL Low

Figure 7 illustrates when AC is removed, power transfers to USB; PSEL = H (AC primary source); channel 1 (CH1) VAC = 5.4 V; channel 2 (CH2) $V_{(USB)}$ = 5 V; channel 3 (CH3) V_{OUT}; output current, I_{OUT} = 0.25 A; channel 4 (CH4) V_{BAT} = 3.5 V; and $I_{(PGM-CHG)}$ = 1 A. The power transfer from AC to USB only takes place after the primary source (AC) is considered bad (too low, V_{AC}<=V_{BAT} + 125 mV) indicated by the $\overline{ACPG}$ FET turning off (open drain not shown). Thus, the output drops down to the battery voltage before the USB source is connected (6th div). The output starts to recover when the USB FET starts to limit the input current (7th div) and the output drops to the DPPM voltage threshold.

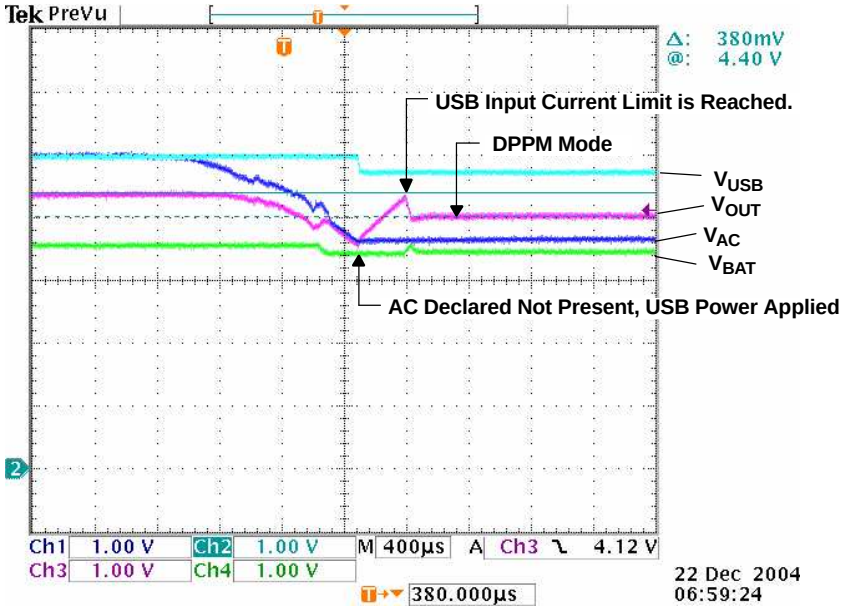


Figure 7. Remove AC – PWR XFER to USB

Figure 8 illustrates when AC (low battery) is removed, power transfers to USB; PSEL = H; channel 1 (CH1) VAC = 5.4 V; channel 2 (CH2) $V_{(USB)}$ = 5 V; channel 3 (CH3) V_{OUT}; output current, I_{OUT} = 0.25 A; channel 4 (CH4) V_{BAT} = 2.25 V; and $I_{(PGM-CHG)}$ = 1 A. This figure is the same as where the battery has more capacity. Note that the output drops to the battery voltage before switching to USB power. A resistor divider between AC and ground tied to PSEL can toggle the power transfer earlier if necessary.

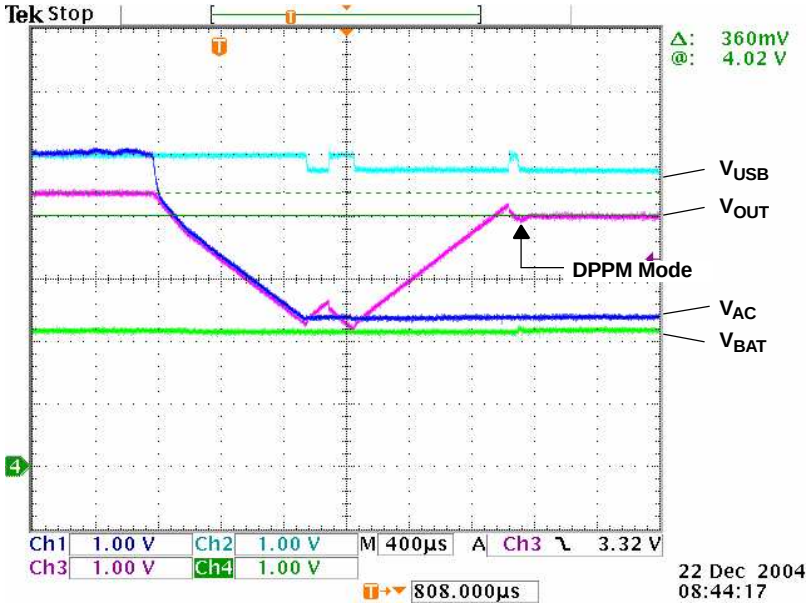


Figure 8. Remove AC (Low Battery) – PWR XFER to USB

Figure 9 illustrates when AC is applied, power transfers from USB to AC; PSEL = H; channel 1 (CH1) VAC = 5.4 V; channel 2 (CH2) $V_{(USB)}$ = 5 V; channel 3 (CH3) V_{OUT}; output current, I_{OUT} = 0.25 A; channel 4 (CH4) V_{BAT} = 3.5 V; and $I_{(PGM-CHG)}$ = 1 A. The charger is set for AC priority but is running off USB until AC is applied. When AC is applied (1st div) and the USB FET opens (2nd div), the AC FET closes (3rd div) and the output recovers from the DPPM threshold (8th div).

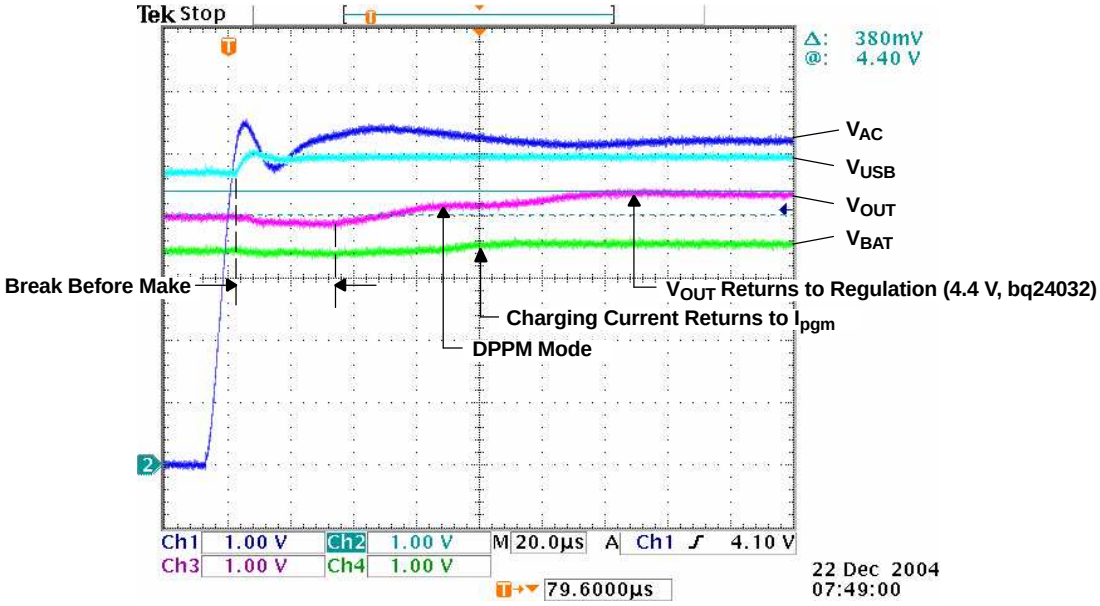


Figure 9. Apply AC – PWR XFER From USB to AC

Figure 10 illustrates when USB is removed, power transfers from USB to AC; PSEL = L; channel 1 (CH1) VAC =

5.4 V; channel 2 (CH2) $V_{(USB)}$ = 5 V; channel 3 (CH3) V_{OUT}; output current, I_{OUT} = 0.25 A; channel 4 (CH4) V_{BAT} = 3.5 V; and $I_{(PGM-CHG)}$ = 1 A. The USB source is removed (2nd div) and the output drops to the battery voltage (declares USB bad, 4th div) and switches to AC (in USB mode) and recovers similar to the figure that is switching to USB power. This power transfer occurred with PSEL low, which means that the AC input is regulated as if it were a USB.

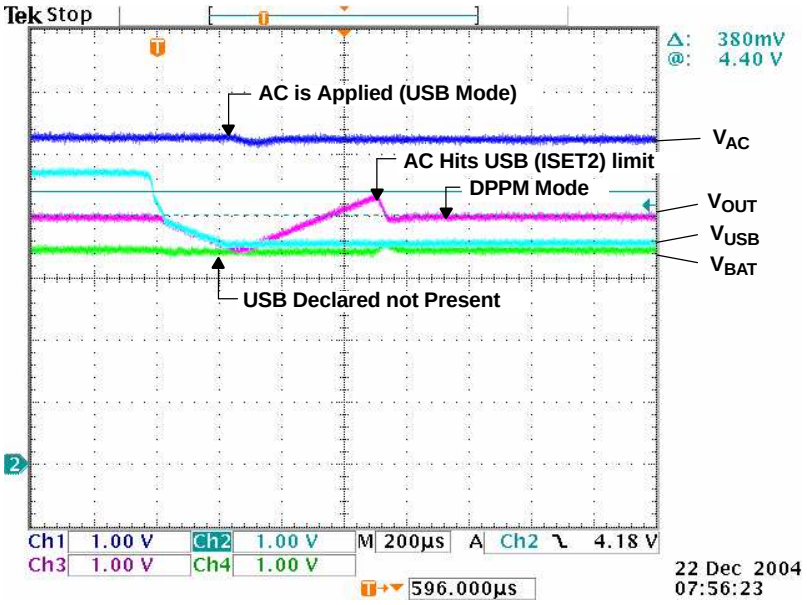


Figure 10. Remove USB – PWR XFER From USB to AC

Figure 11 illustrates when the battery is absent, power transfers to USB; PSEL = H; channel 1 (CH1) VAC = 5.4 V; channel 2 (CH2) $V_{(USB)}$ = 5 V; channel 3 (CH3) V_{OUT}; output current, I_{OUT} = 0.25 A; channel 4 (CH4) V_{BAT}; $I_{(PGM-CHG)}$ = 1 A. Note the saw-tooth waveform due to cycling between charge done and refresh (new charge).

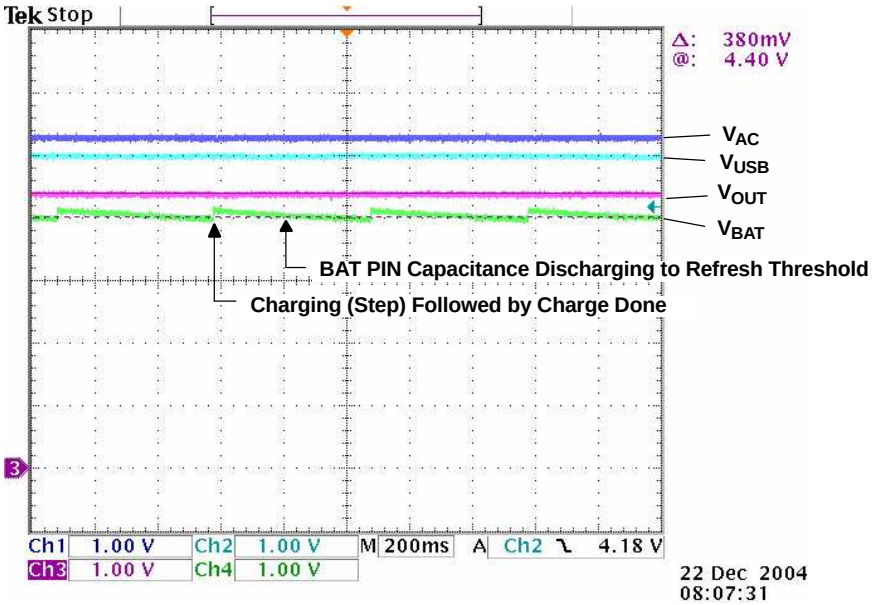


Figure 11. Battery Absent – PWR XFER to USB

Figure 12 illustrates when a battery is inserted for power up; channel 1 (CH1) VAC = 0 V; channel 2 (CH2) V_{USB} = 0 V; channel 3 (CH3) V_{OUT}; output current, I_{OUT} = 0.25 A for V_{OUT} > 2 V; channel 4 (CH4) V_{BAT} = 3.5 V; $C_{(DPPM)}$ = 0 pF. When there are no power sources and the battery is inserted, the output tracks the battery voltage if there is no load (<10 mA of load) on the output, as shown. If a load is present that keeps the output more than 200 mV below the battery, a short-circuit condition is declared. At this time, the load has to be removed to recover. A capacitor can be placed on the DPPM pin to delay implementing the short-circuit mode and get unrestricted (not limited) current.

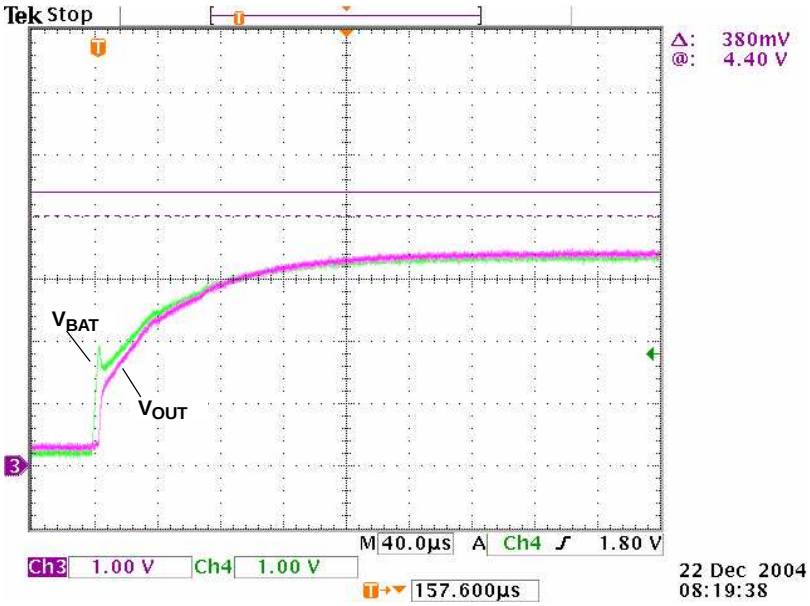


Figure 12. Insert Battery – Power-Up Output via BAT

Figure 13 illustrates USB bootup and power-up via USB; channel 1 (CH1) $V_{(USH)}$ = 0 to 5 V; channel 2 (CH2) USB input current (0.2 A/div); PSEL = Low; CE = High; ISET2 = High; V_{BAT} = 3.85 V; $V_{(DPPM)}$ = 3.0 V ($V_{(DPPM)}$ × 1.15 < V_{BAT}, otherwise DPPM mode increases time duration). When a USB source is applied (if AC is not present), the CE pin and ISET2 pin are ignored during the boot-up time and a maximum input current of 100 mA is made available to the OUT or BAT pins. After the boot-up time, the IC implements the CE and ISET2 pins as programmed.

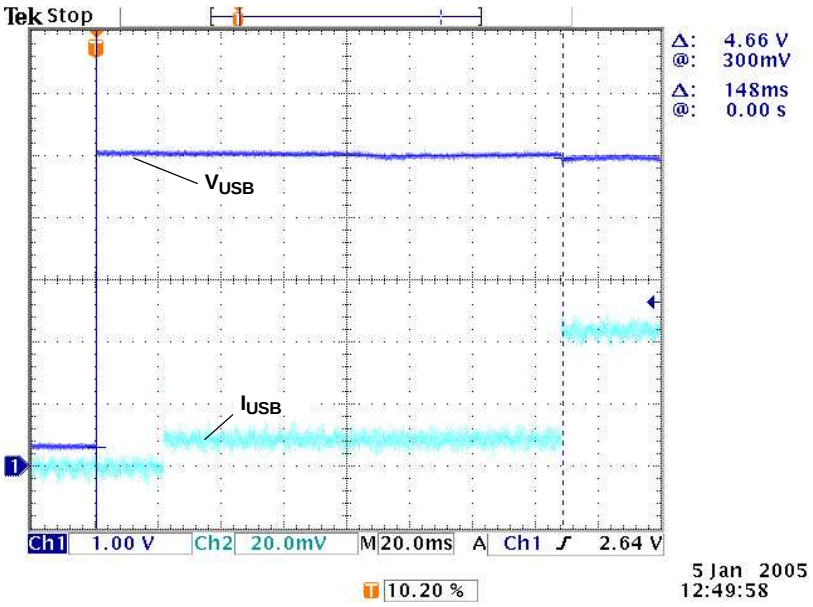


Figure 13. USB Boot-Up Power-Up

Battery Temperature Monitoring

The bqTINY-III continuously monitors battery temperature by measuring the voltage between the TS and VSS pins. An internal current source provides the bias for most-common 10 kΩ negative-temperature coefficient thermistors (NTC) (see Figure 14). The device compares the voltage on the TS pin against the internal $V_{(LTF)}$ and $V_{(HTF)}$ thresholds to determine if charging is allowed. Once a temperature outside the $V_{(LTF)}$ and $V_{(HTF)}$ thresholds is detected, the device immediately suspends the charge. The device suspends charge by turning off the power FET and holding the timer value (i.e., timers are not reset). Charge is resumed when the temperature returns to the normal range. The allowed temperature range for 103AT-type thermistor is 0°C to 45°C. However, the user may increase the range by adding two external resistors. See Figure 15.

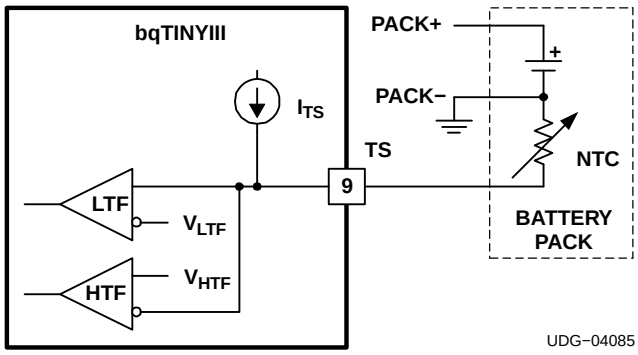


Figure 14. TS Pin Configuration

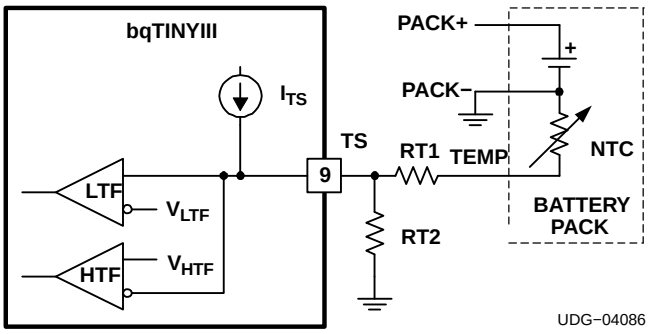


Figure 15. TS Pin Thresholds

Battery Pre-Conditioning

During a charge cycle, if the battery voltage is below the $V_{(LOWV)}$ threshold, the bqTINY-III applies a precharge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The resistor connected between the ISET1 and VSS, R_{SET}, determines the precharge rate. The $V_{(PRECHG)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{O\ (PRECHG)} = \frac{V_{(PRECHG)} \times K_{(SET)}}{R_{SET}} \quad (3)$$

The bqTINY-III activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the bqTINY-III turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. The timeout is extended if the charge current is reduced by DPPM. See the *Timer Fault Recovery* section for additional details.

Battery Charge Current

The bqTINY-III offers on-chip current regulation with programmable set point. The resistor connected between the ISET1 and VSS, $R_{SET,}$ determines the charge level. The charge level may be reduced to give the system priority on input current (see DPPM). The $V_{(SET)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O\ (OUT)} = \frac{V_{(SET)} \times K_{(SET)}}{R_{SET}} \quad (4)$$

When powered from a USB port, the input current available (0.1 A/0.5 A) is typically less than the programmed (ISET1) charging current, and therefore, the DPPM feature attempts to keep the output from being pulled down by reducing the charging current.

For the bq24032/2A/8 the charge level, during AC operation only (PSEL = High), can be changed by a factor of 2 by setting the ISET2 pin high (full charge) or low (half charge). The voltage on the ISET1 pin, VSET1, is divided by 2 when in the half constant current charge mode. Note that with PSEL low, the ISET2 pin controls only the 0.1 A/0.5 A USB current level.

See the section titled *Power-Path Management* for additional details.

Battery Voltage Regulation

The voltage regulation feedback is through the BAT pin. This input is tied directly to the positive side of the battery pack. The bqTINY-III monitors the battery-pack voltage between the BAT and VSS pins. When the battery voltage rises to the $V_{O(REG)}$ threshold, the voltage regulation phase begins and the charging current begins to taper down.

If the battery is absent, the BAT pin cycles between charge done ($V_{O(REG)}$) and charging (battery refresh threshold, ~4.1 V). See Figure 11.

See Figure 12 for power up by battery insertion.

As a safety backup, the bqTINY-III also monitors the charge time in the charge mode. If charge is not terminated within this time period, $t_{(CHG)}$, the bqTINY-III turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. See the DPPM operation under Case 1 for information on extending the safety timer during DPPM operation. See the*Timer Fault Recovery* section for additional details.

Power Handoff

The design goal of the IC is to keep the system powered at all times (OUT pin); first, by either AC or USB input—priority chosen by PSEL, and lastly by the battery. The input power source is only considered present if its power-good status is low. There is a break-before-make switching action when switching between AC to USB or USB to AC, for $t_{SW\text{-}AC/USB}$, where the system capacitance should hold up the system voltage. Note that the transfer of power occurs when the sources power-good pin goes high (open-drain output high = power not present), which is when the input source drops to the battery's voltage. If the battery is below a useable voltage, the system may reset. Typically, prior to losing the input power, the battery would have some useable capacity, and a system reset would be avoided. If the battery was dead or missing, the system would lose power unless the PSEL pin was used to transfer power prior to shutdown.

If this is a concern, there is a simple external solution. Externally toggling the PSEL (bq24030/2A/5/8) pin immediately starts the power-transfer process (does not wait for input to drop to the battery's voltage). This can

be implemented by a resistor divider between the AC input and ground with the PSEL pin tied between R1 (top resistor) and R2 (resistor to ground). The resistor values are chosen such that the divider voltage will be at 1 V (PSEL threshold) when the AC has dropped to its critical voltage (user defined). An internal ~280-kΩ resistor is applied when PSEL < 1 V, to provide hysteresis. Choose R2 between 10 kΩ and 60 kΩ and $V_{(ac\text{-}critical)}$ between 3.5 V and 4.5 V. R1 can be found using the following equation:

R1 = R2 ($V_{(ac\text{-}critical)}$ – 1 V); $V_{(ac\text{-}reset)}$ = 1 + R1 (R2+280 k)/(280 k × R2);

Example: If R2 = 30 kΩ and $V_{(ac\text{-}critical)}$ = 4 V; R1 = 30 kΩ(4 V – 1 V) = 90 kΩ, $V_{(ac\text{-}reset)}$ = 1+ 90k (30 k+280 k)/(280 k×30 k) = 4.32 V. Therefore, for a 90 kΩ/30 kΩ divider, the bias on PSEL would switch power from AC to USB ($\overline{USBPG}$ = L) when the VAC dropped to 4 V (independent of V_{BAT}) and switches back when the VAC recovers to 4.32 V. See Figure 6 through Figure 10.

Temperature Regulation and Thermal Protection

In order to maximize charge rate, the bqTINY-III features a junction temperature regulation loop. If the power dissipation of the IC results in a junction temperature greater than the $T_{J(REG)}$ threshold, the bqTINY-III throttles back on the charge current in order to maintain a junction temperature around the $T_{J(REG)}$ threshold. To avoid false termination, the termination detect function is disabled while in this mode.

The bqTINY-III also monitors the junction temperature, T_J, of the die and disconnects the OUT pin from AC or USB inputs if T_J exceeds $T_{(SHTDWN)}$. This operation continues until T_J falls below $T_{(SHTDWN)}$ by the hysteresis level specified in the specification table.

The battery supplement mode has no thermal protection. The Q2 FET continues to connect the battery to the output (system), if input power is not sufficient; however, a short-circuit protection circuit limits the battery discharge current such that the maximum power dissipation of the part is not exceeded under typical design conditions.

Charge Timer Operation

As a safety backup, the bqTINY-III monitors the charge time in the charge mode. If the termination threshold is not detected within the time period, $t_{(CHG)}$, the bqTINY-III turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. The resistor connected between the TMR and VSS, R_{TMR}, determines the timer period. The $K_{(TMR)}$ parameter is specified in the specifications table. In order to disable the charge timer, eliminate R_{TMR}, connect the TMR pin directly to the LDO pin. Note that this action eliminates all safety timers, disables termination, and also clears any timer fault (does not apply to the bq24032). TMR pin should not be left floating.

$$t_{(CHG)} = K_{(TMR)} \times R_{(TMR)} \quad (5)$$

While in the thermal regulation mode or DPPM mode, the bqTINY-III dynamically adjusts the timer period in order to provide the additional time needed to fully charge the battery. This proprietary feature is designed to prevent against early or false termination. The maximum charge time in this mode, $t_{(CHG\text{-}TREG)}$, is calculated by Equation 6.

$$t_{(CHG-TREG)} = \frac{t_{(CHG)} \times V_{(SET)}}{V_{(SET-REG)}} \quad (6)$$

Note that because this adjustment is dynamic and changes as the ambient temperature changes and the charge level changes, the timer clock is adjusted. It is difficult to estimate a total safety time without integrating the above equation over the charge cycle. Therefore, understanding the theory that the safety time is adjusted inversely proportionately with the charge current and the battery is a current-hour rating, the safety time dynamically adjusts appropriately.

The $V_{(SET)}$ parameter is specified in the specifications table. $V_{(SET\text{-}TREG)}$ is the voltage on the ISET pin during the thermal regulation or DPPM mode and is a function of charge current. (Note that charge current is dynamically adjusted during the thermal regulation or DPPM mode.)

$$V_{(SET-TREG)} = \frac{I_{(OUT)} \times R_{(SET)}}{K_{(SET)}} \quad (7)$$

All deglitch times also adjusted proportionally to $t_{(CHG\text{-}TREG)}$.

Charge Termination and Recharge

The bqTINY-III monitors the voltage on the ISET1 pin, during voltage regulation, to determine when termination should occur (C/10 – 250 mV, C/25 – 100 mV). Once the termination threshold, $I_{(TERM)}$, is detected the bqTINY-III terminates charge. The resistor connected between the ISET1 and VSS, R_{SET}, programs the fast charge current level (C level, V_{ISET1} = 2.5 V) and thus the C/10 and C/25 current termination threshold levels (does not apply to the bq24032). The $V_{(TERM)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{(TERM)} = \frac{V_{(TERM)} \times K_{(SET)}}{R_{SET}} \quad (8)$$

After charge termination, the bqTINY-III re-starts the charge once the voltage on the OUT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times.

LDO Regulator

The bqTINY-III provides a 3.3-V LDO regulator. This regulator is typically used to power USB transceiver or drivers in portable applications. Note that this LDO is only enabled when either AC or USB inputs are present. If the CE pin is low (chip disabled) and AC or USB is present, the LDO is powered by the battery. This is to ensure low input current when the chip is disabled.

Sleep and Standby Modes

The bqTINY-III charger circuitry enters the low-power sleep mode if both AC and USB are removed from the circuit. This feature prevents draining the battery into the bqTINY-III during the absence of input supplies. Note that in sleep mode, Q2 remains on (i.e., battery connected to the OUT pin) in order for the battery to continue supplying power to the system.

The bqTINY-III enters the low-power standby mode if while AC or USB is present, the CE input is low. In this suspend mode, internal power FETs Q1 and Q3 (see the block diagram) are turned off, the BAT input is used to power the system through OUT pin, and the LDO remains on (powered from output). This feature is designed to limit the power drawn from the input supplies (such as USB suspend mode).

Charge Status Outputs

The open-drain (OD) STAT1 and STAT2 outputs indicate various charger operations as shown in Table 2. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off. Note that this assumes CE = High.

Table 2. Status Pins Summary

CHARGE STATE	STAT1	STAT2
Precharge in progress	ON	ON
Fast charge in progress	ON	OFF
Charge done	OFF	ON
Charge suspend (temperature), timer fault, and sleep mode	OFF	OFF

$\overline{\text{ACPG}}$, $\overline{\text{USBPG}}$ Outputs (Power Good), bq24030/2/2A/5

The two open-drain pins, $\overline{\text{ACPG}}$, $\overline{\text{USBPG}}$ (AC and USB power good), indicate when the AC adapter or USB port is present and above the battery voltage. The corresponding output turns ON (low) when exiting sleep mode (input voltage above battery voltage). This output is turned off in the sleep mode (open drain). The $\overline{\text{ACPG}}$, $\overline{\text{USBPG}}$ pins can be used to drive an LED or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off.

$\overline{\text{PG}}$ Output (Power Good), bq24038

The open-drain pin $\overline{\text{PG}}$ indicates when either the AC adapter or USB port is present and above the battery voltage. This output is turned off in sleep mode (open drain). The $\overline{\text{PG}}$ pin can be used to drive a LED or communicate with the host processor.

CE Input (Chip Enable)

The CE (chip enable) digital input is used to disable or enable the IC. A high-level signal on this pin enables the chip, and a low-level signal disables the device and initiates the standby mode. The bqTINY-III enters the low-power standby mode when the CE input is low with either AC or USB present. In this suspend mode, internal power FETs Q1 and Q3 (see block diagram) are turned off; the battery (BAT pin) is used to power the system via Q2 and the OUT pin which also powers the LDO. This feature is designed to limit the power drawn from the input supplies (such as USB suspend mode).

VBSEL INput (Battery Voltage Selection), bq24038

The VBSEL (battery voltage select) digital input pin can be used to set the charge voltage to 4.2 V typical (VBSEL = low) or 4.36 V typical (VBSEL = high). If VBSEL is left open, an internal current source pulldown ensures that the charge voltage is set to 4.2 V typical.

Charge Disable Functions

The DPPM input can be used to disable the charge process. This can be accomplished by floating the DPPM mode. Note that this applies to both AC and USB charging.

Timer Fault Recovery

As shown in Figure 3, bqTINY-III provides a recovery method to deal with timer fault conditions. The following summarizes this method:

Condition 1: Charge voltage above recharge threshold ($V_{(RCH)}$) and timeout fault occurs.

Recovery Method: bqTINY-III waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge, or battery removal. Once the battery falls below the recharge threshold, the bqTINY-III clears the fault and starts a new charge cycle. A POR or CE toggle also clears the fault.

Condition 2: Charge voltage below recharge threshold ($V_{(RCH)}$) and timeout fault occurs.

Recovery Method: Under this scenario, the bqTINY-III applies the $I_{(FAULT)}$ current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the bqTINY-III disables the $I_{(FAULT)}$ current and executes the recovery method described for condition 1. Once the battery falls below the recharge threshold, the bqTINY-III clears the fault and starts a new charge cycle. A POR or CE toggle also clears the fault.

Short-Circuit Recovery

The output can experience two types of short-circuit protection, one associated with the input and one with the battery.

If the output drops below ~1 V, an input short-circuit condition is declared and the input FETs (AC and USB) are turned off. To recover from this state, a 500-Ω pullup resistor from each input is applied (switched) to the output. To recover, the load on the output has to be reduced {Rload > 1 V × 500 Ω/ (Vin–Vout)} such that the pullup resistor is able to lift the output voltage above 1 V, for the input FETs to be turned back on.

If the output drops 200 mV below the battery voltage, the battery FET is considered in short circuit and the battery FET turns off. To recover from this state, there is a 10-mA current source from the battery to the output. Once the output load is reduced, such that the 10-mA current source can pick up the output within 200 mV of the battery, the FET turns back on.

If the *short* is removed, and the minimum system load is still too large [R<(VBat-200 nV) / 10 mA], the short-circuit protection can be temporarily defeated. The battery short-circuit protection can be disabled (recommended only for a short time) if the voltage on the DPPM pin is less than 1 V. Pulsing this pin below 1 V, for a few microseconds, should be enough to recover.

This short-circuit disable feature was implemented mainly for power up when inserting a battery. Because the BAT input voltage rises much faster than the OUT voltage (Vout<Vbat-200 mV), with most any capacitive load on the output, the part can get stuck in short-circuit mode. Placing a capacitor between the DPPM pin and ground slows the V_{DPPM} rise time, during power up, and delays the short-circuit protection. Too large a capacitance on this pin (too much of a delay) could allow too-high currents if the output was shorted to ground. The recommended capacitance is 1 nF to 10 nF. The V_{DPPM} rise time is a function of the 100-µA DPPM current source, the DPPM resistor, and the capacitor added.

APPLICATION INFORMATION

Selecting the Input and Output Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor on each input (AC and USB). A 0.1-µF ceramic capacitor, placed in close proximity to AC and USB to VSS pins, works well. In some applications depending on the power supply characteristics and cable length, it may be necessary to add an additional 10-µF ceramic capacitor to each input.

The bqTINY-III only requires a small output capacitor for loop stability. A 0.1-µF ceramic capacitor placed between the OUT and VSS pin is typically sufficient.

The integrated LDO requires a maximum of 1-µF ceramic capacitor on its output. The output does not require a capacitor for a steady-state load but a 0.1-µF minimum capacitance is recommended.

It is recommended to install a minimum of 33-µF capacitor between the BAT pin and VSS (in parallel with the battery). This ensures proper hot plug power up with a no-load condition (no system load or battery attached).

Thermal Considerations

The bqTINY-III is packaged in a thermally enhanced MLP package. The package includes a QFN thermal pad to provide an effective thermal contact between the device and the printed-circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled *QFN/SON PCB Attachment* (SLUA271). The power pad should be tied to the VSS plane. The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient).

The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_J - T_A}{P} \tag{9}$$

where

T_J = chip junction temperature

T_A = ambient temperature

P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- whether or not the device is board mounted
- trace size, composition, thickness, and geometry
- orientation of the device (horizontal or vertical)
- volume of the ambient air surrounding the device under test and airflow
- whether other surfaces are in close proximity to the device being tested

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal power FET. It can be calculated from Equation 10:

$$P = \left[\left(V_{IN} - V_{OUT}\right) \times \left(I_{OUT} + I_{BAT}\right)\right] + \left[\left(V_{OUT} - V_{BAT}\right) \times \left(I_{BAT}\right)\right] \tag{10}$$

Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See Figure 1. Typically the Li-ion battery's voltage quickly (< 2 V minutes) ramps to approximately 3.5 V, when entering fast charge (1-C charge rate and battery above 3 V). Therefore, it is customary to perform the steady-state thermal design using 3.5 V as the minimum battery voltage because the system board and charging device does not have time to reach a maximum temperature due to the thermal mass of the assembly during the early stages of fast charge. This theory is easily verified by performing a charge cycle on a discharged battery while monitoring the battery voltage and chargers power pad temperature.

APPLICATION INFORMATION (continued)

PCB Layout Considerations

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from input terminals to VSS and the output filter capacitors from OUT to VSS should be placed as close as possible to the bqTINY-II, with short trace runs to both signal and VSS pins.
- All low-current VSS connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high-current charge paths into AC and USB and from the BAT and OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bqTINY-III is packaged in a thermally enhanced MLP package. The package includes a QFN thermal pad to provide an effective thermal contact between the device and the printed-circuit board. Full PCB design guidelines for this package are provided in the application note entitled *QFN/SON PCB Attachment* (SLUA271).

THERMAL PAD MECHANICAL DATA

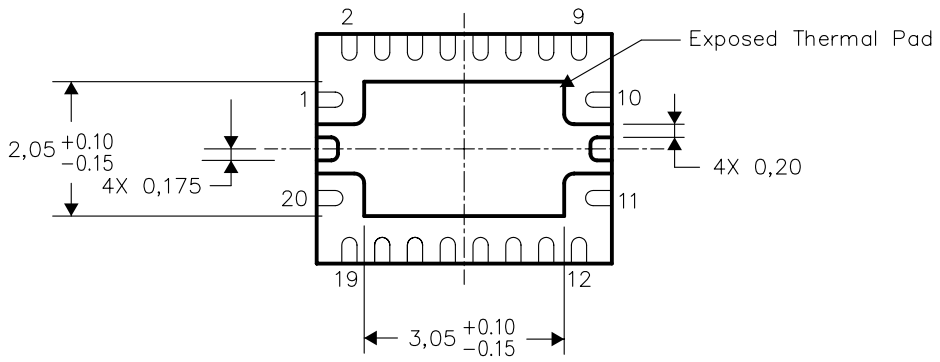
RHL (R–PQFP–N20)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ24030RHLR	ACTIVE	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24030RHLRG4	ACTIVE	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24032ARHLR	ACTIVE	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24032ARHLRG4	ACTIVE	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24032ARHLT	ACTIVE	QFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24032ARHLTG4	ACTIVE	QFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24032RHLR	NRND	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24032RHLRG4	NRND	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24035RHLR	ACTIVE	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24035RHLRG4	ACTIVE	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24038RHLR	ACTIVE	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24038RHLRG4	ACTIVE	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24038RHLT	ACTIVE	QFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24038RHLTG4	ACTIVE	QFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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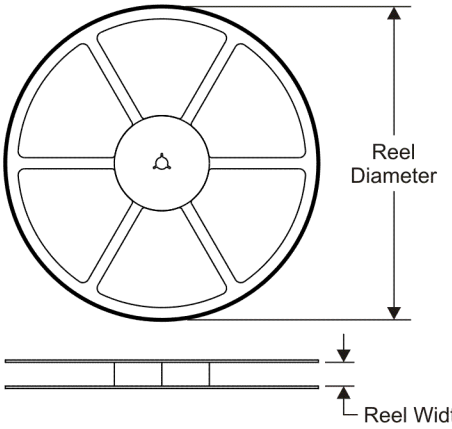
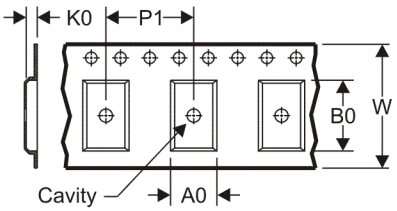
TAPE AND REEL INFORMATION

REEL DIMENSIONS

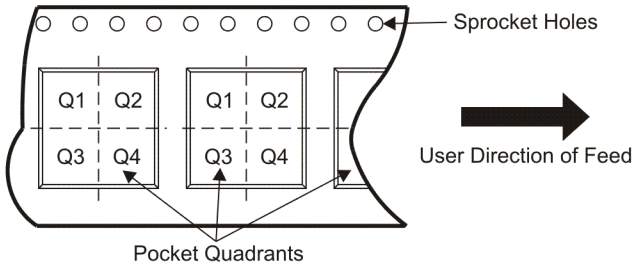


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

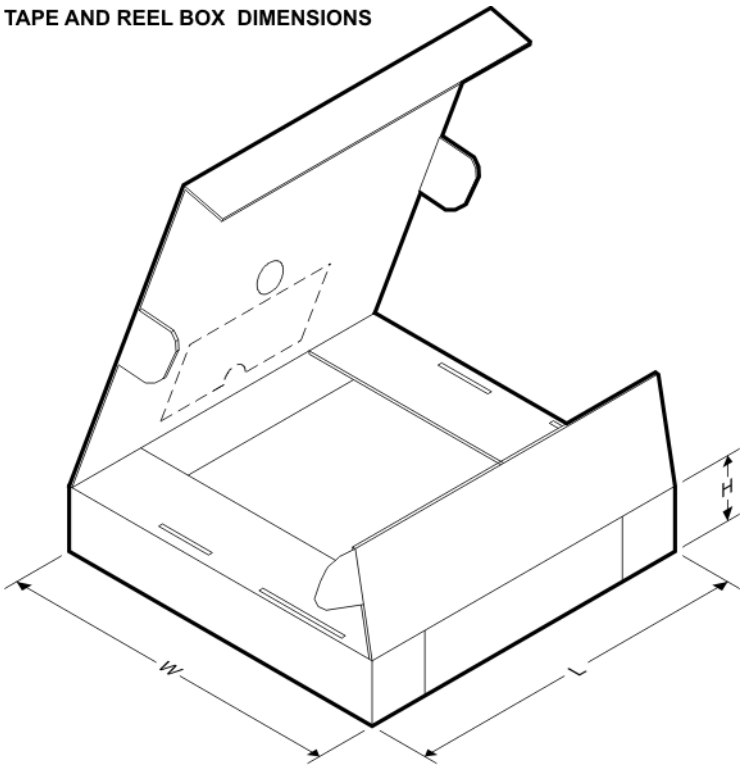
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24030RHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.3	8.0	12.0	Q1
BQ24030RHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24032ARHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.3	8.0	12.0	Q1
BQ24032ARHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24032ARHLT	QFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24032ARHLT	QFN	RHL	20	250	180.0	12.4	3.8	4.8	1.3	8.0	12.0	Q1
BQ24032RHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.3	8.0	12.0	Q1
BQ24032RHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24035RHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.3	8.0	12.0	Q1
BQ24035RHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24038RHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.3	8.0	12.0	Q1
BQ24038RHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24038RHLT	QFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24038RHLT	QFN	RHL	20	250	330.0	12.4	3.8	4.8	1.3	8.0	12.0	Q1

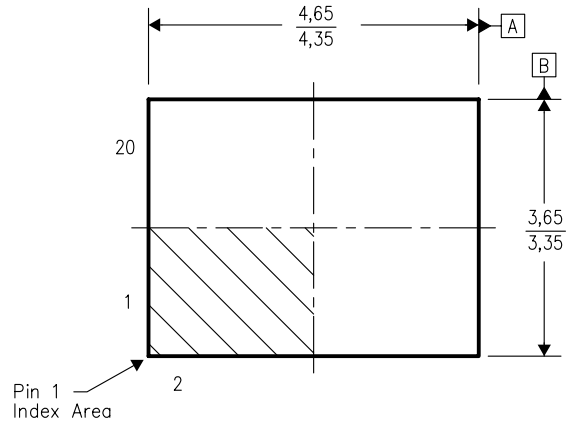
TAPE AND REEL BOX DIMENSIONS

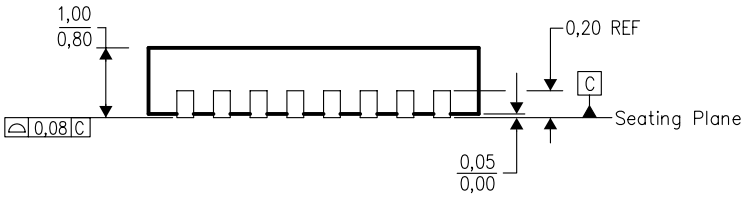


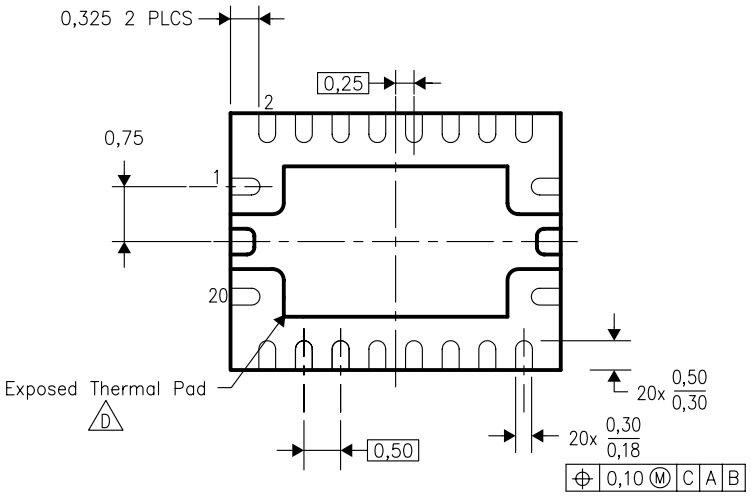
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24030RHLR	QFN	RHL	20	3000	333.2	345.9	28.6
BQ24030RHLR	QFN	RHL	20	3000	346.0	346.0	29.0
BQ24032ARHLR	QFN	RHL	20	3000	370.0	355.0	55.0
BQ24032ARHLR	QFN	RHL	20	3000	346.0	346.0	29.0
BQ24032ARHLT	QFN	RHL	20	250	190.5	212.7	31.8
BQ24032ARHLT	QFN	RHL	20	250	195.0	200.0	45.0
BQ24032RHLR	QFN	RHL	20	3000	370.0	355.0	55.0
BQ24032RHLR	QFN	RHL	20	3000	346.0	346.0	29.0
BQ24035RHLR	QFN	RHL	20	3000	370.0	355.0	55.0
BQ24035RHLR	QFN	RHL	20	3000	346.0	346.0	29.0
BQ24038RHLR	QFN	RHL	20	3000	370.0	355.0	55.0
BQ24038RHLR	QFN	RHL	20	3000	346.0	346.0	29.0
BQ24038RHLT	QFN	RHL	20	250	190.5	212.7	31.8
BQ24038RHLT	QFN	RHL	20	250	370.0	355.0	55.0

RHL (R–PQFP–N20) PLASTIC QUAD FLATPACK







4205346–2/C 12/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

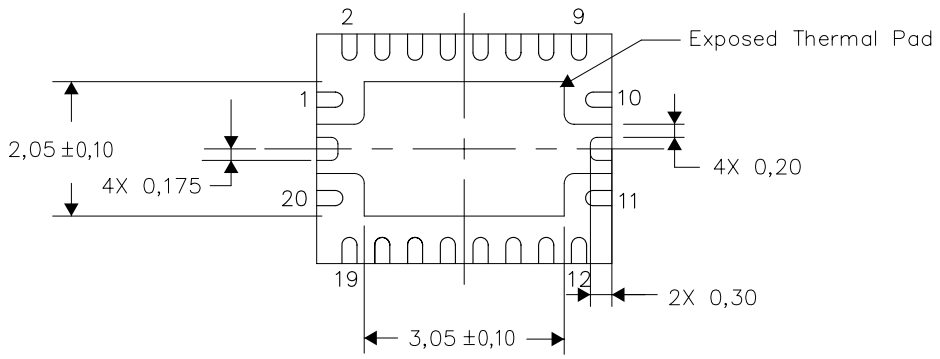
RHL (R–PVQFN–N20)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

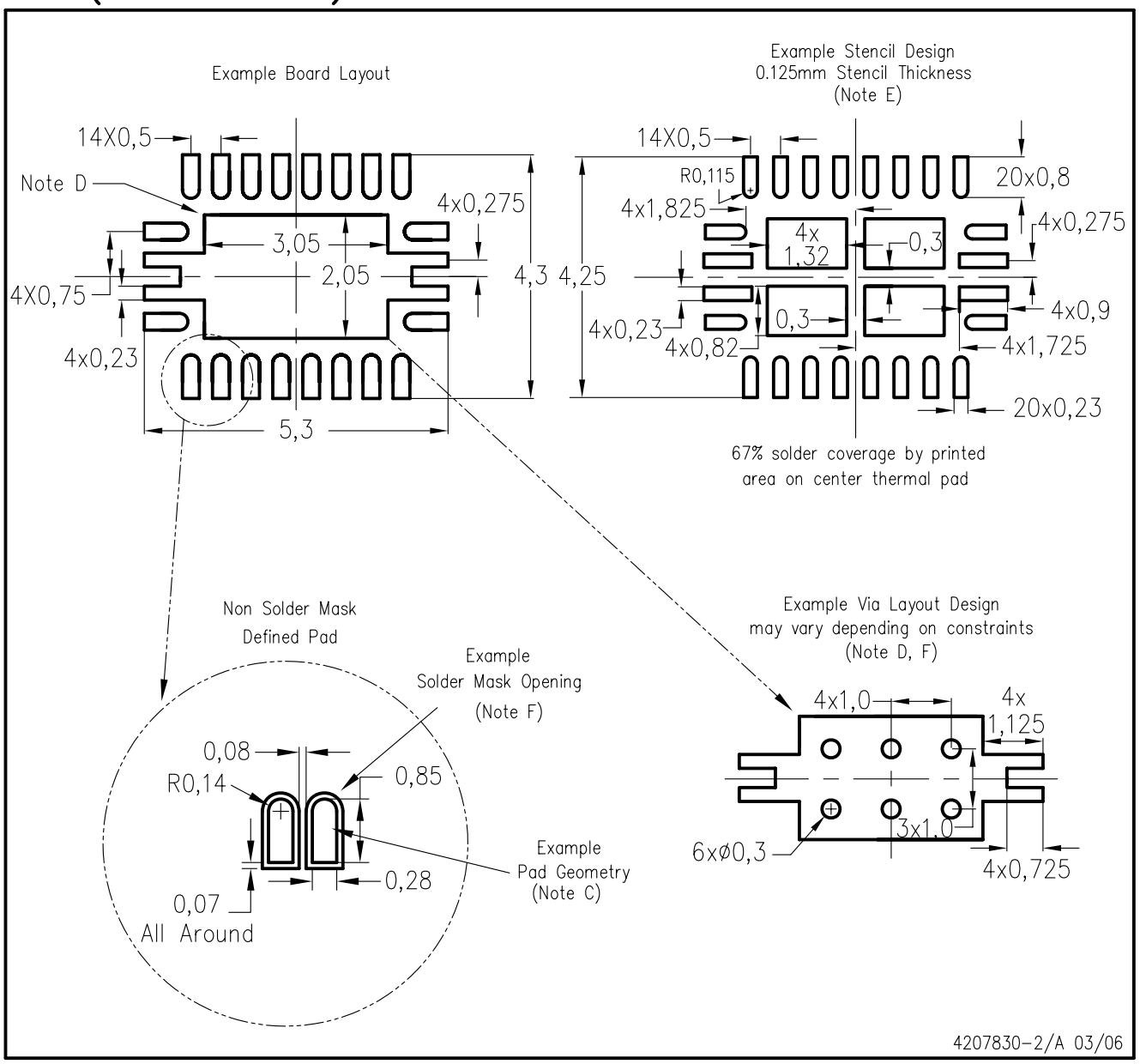


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHL (R–PQFP–N20)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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