

NDS9435

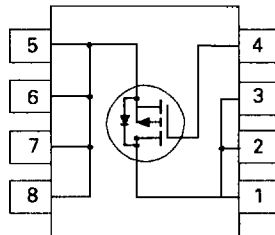
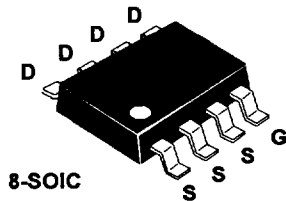
Single P-Channel Enhancement Mode Field Effect Transistor

General Description

These P-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -4.6A, -30V. $R_{DS(ON)} = 0.07\Omega @ V_{GS} = -10V$.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDS9435	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1 \text{ M}\Omega$)	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_b	Drain Current - Continuous $T_A = 25^\circ\text{C}$	± 4.6	A
	- Continuous $T_A = 70^\circ\text{C}$	± 4.1	
	- Pulsed $T_A = 25^\circ\text{C}$	± 15	
P_D	Maximum Power Dissipation	2.5 (Note 1)	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50 (Note 1)	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	25 (Note 1)	$^\circ\text{C/W}$

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_b = -250\ \mu\text{A}$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$T_J = 55^\circ\text{C}$			-10	μA
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_b = -250\ \mu\text{A}$	-1	-2	-3	V
		$T_J = 125^\circ\text{C}$	-0.85	-1.7	-2.6	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_b = -4.6\text{ A}$		0.054	0.07	Ω
		$T_J = 125^\circ\text{C}$		0.075	0.105	
		$V_{GS} = -6\text{ V}, I_b = -4.1\text{ A}$		0.068	0.09	
		$V_{GS} = -4.5\text{ V}, I_b = -2\text{ A}$		0.083	0.13	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	-15			A
		$V_{GS} = -4.5, V_{DS} = -5\text{ V}$	-4			
g_{FS}	Forward Transconductance	$V_{DS} = -15\text{ V}, I_b = -4.6\text{ A}$		8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1570		pF
C_{oss}	Output Capacitance			620		
C_{riss}	Reverse Transfer Capacitance			220		
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -15\text{ V}, I_b = -1\text{ A},$ $V_{GEN} = -10\text{ V}, R_{GEN} = 6\ \Omega$		11	30	ns
t_r	Turn - On Rise Time			18	60	
$t_{D(off)}$	Turn - Off Delay Time			63	120	
t_f	Turn - Off Fall Time			27	100	
Q_g	Total Gate Charge	$V_{DS} = -10\text{ V},$ $I_b = -4.6\text{ A}, V_{GS} = -10\text{ V}$		38	40	nC
Q_{gs}	Gate-Source Charge			3		
Q_{gd}	Gate-Drain Charge			12		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.2	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -4.6\text{ A}$ (Note 2)		-1	-1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_F = -4.6\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$		80	100	ns
Notes:						
1. $R_{\theta(jc)}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta(jc)}$ is $25^\circ\text{C}/\text{W}$ in this case but depends on the specific circuit board thermal design.						
2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.						

Typical Electrical Characteristics

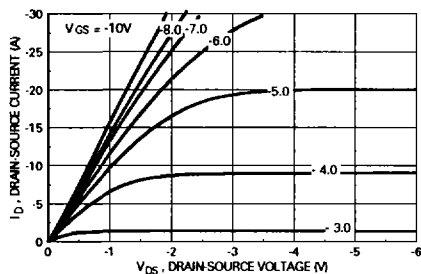


Figure 1. On-Region Characteristics.

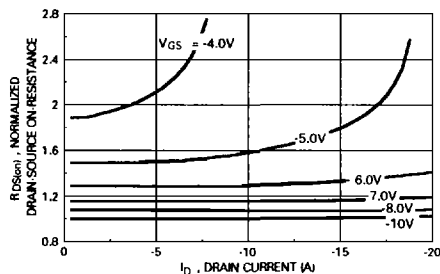


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

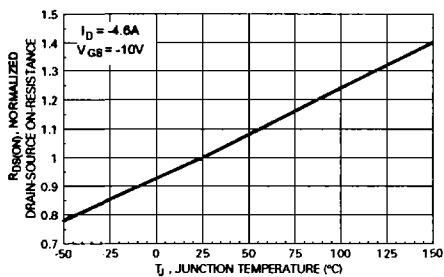


Figure 3. On-Resistance Variation with Temperature.

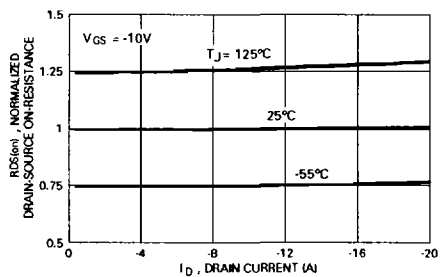


Figure 4. On-Resistance Variation with Drain Current and Temperature.

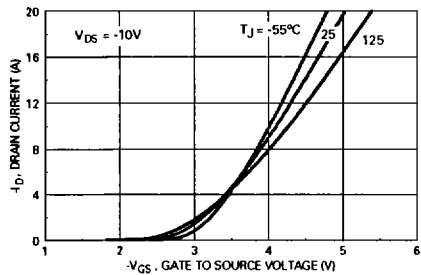


Figure 5. Transfer Characteristics.

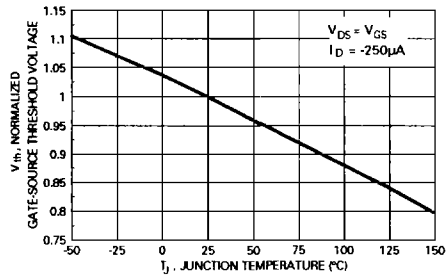


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

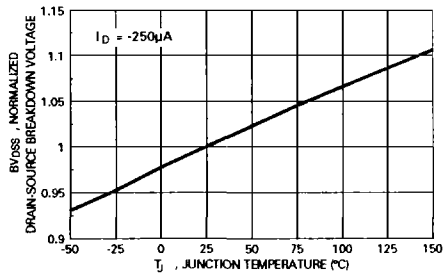


Figure 7. Breakdown Voltage Variation with Temperature.

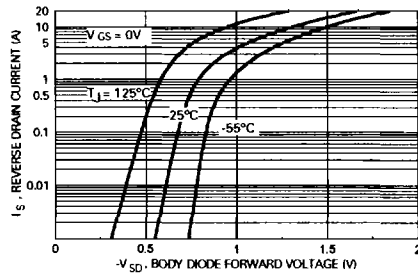


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.

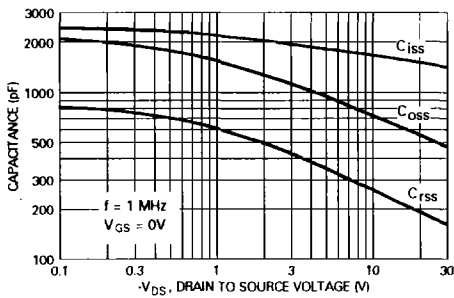


Figure 9. Capacitance Characteristics.

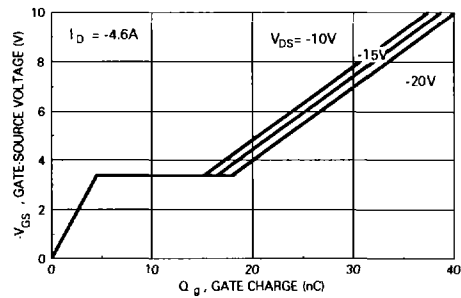


Figure 10. Gate Charge Characteristics.

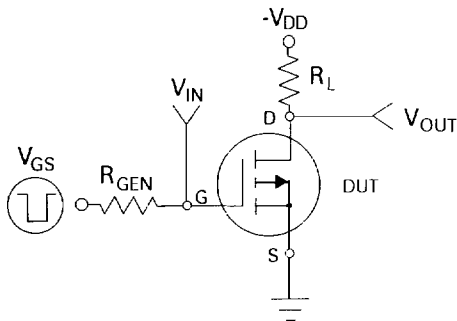


Figure 11. Switching Test Circuit.

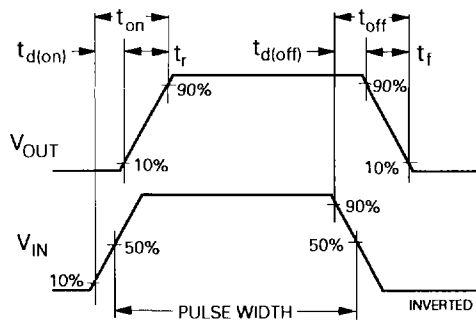


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)

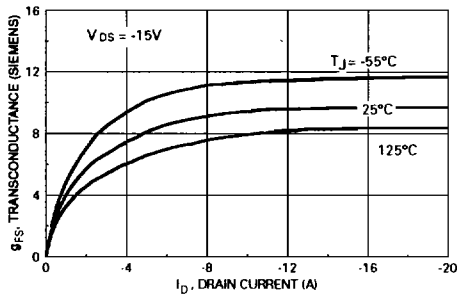


Figure 13. Transconductance Variation with Drain Current and Temperature.

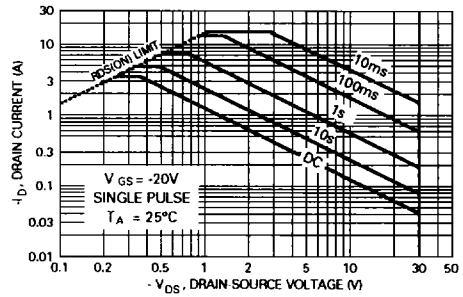


Figure 14. Maximum Safe Operating Area.

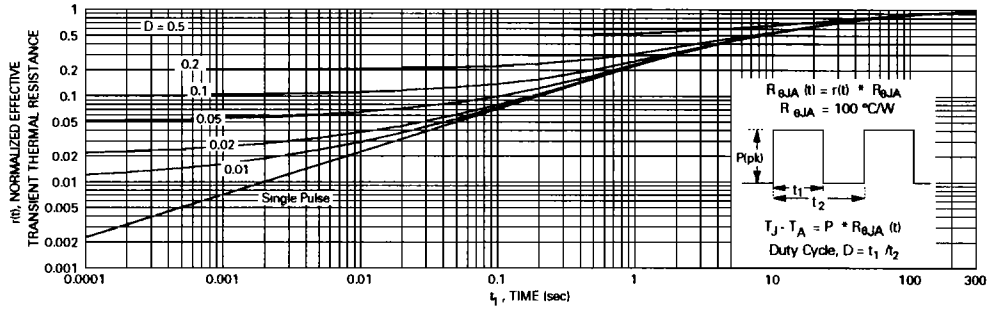


Figure 15. Transient Thermal Response Curve.

Note: Characterization performed using a circuit board with 75°C/W typical thermal resistance.