HARRIS SEMICONDUCTOR

ICM7218

8-Digit LED μP Compatible Multiplexed Display Decoder Driver

GENERAL DESCRIPTION

The ICM7218 series of universal LED driver systems provide, in a single package, all the circuitry necessary to interface most common microprocessors or digital systems to an LED display. Included on chip are an 8-byte static display memory, 2 types of 7-segment decoders, multiplex scan circuitry, and high current digit and segment drivers for either common-cathode or common-anode displays.

The ICM7218A and ICM7218B feature 2 control lines ($\overline{\text{WRITE}}$ and MODE) which write either 4 bits of control information (DATA COMING, $\overline{\text{SHUTDOWN}}$,$\overline{\text{DECODE}}$, and HEXA/$\overline{\text{CODE B}}$) or 8 bits of display input data. Display data is automatically sequenced into the 8-byte internal memory on successive positive going $\overline{\text{WRITE}}$ pulses. Data may be displayed either directly or decoded in Hexadecimal or Code B formats.

The ICM7218C and ICM7218D feature 2 control lines ($\overline{\text{WRITE}}$ and HEXA/CODE B/$\overline{\text{SHUTDOWN}}$), 4 separate display data input lines, and 3 digit address lines. Display data is written into the internal memory by setting up a digit address and strobing the $\overline{\text{WRITE}}$ line low. Only Hexadecimal and Code B formats are available for display outputs.

FEATURES

- **Microprocessor Compatible**
- **Total Circuit Integration On Chip Includes:**
  - **a) Digit and Segment Drivers**
  - **b) All Multiplex Scan Circuitry**
  - **c) 8 Byte Static Display Memory**
  - **d) 7 Segment Hexadecimal and Code B Decoders**
- **Output Drive Suitable for LED Displays Directly**
- **Common Anode and Common Cathode Versions**
- **Single 5 Volt Supply Required**
- **Data Retention to 2 Volts Supply**
- **Shutdown Feature — Turns Off Display and Puts Chip Into Low Power Dissipation Mode**
- **Sequential and Random Access Versions**
- **Decimal Point Drive On Each Digit**

ORDERING INFORMATION

Part Number	Temperature Range	Package	Display Type
ICM7218AIJI	−40°C to +85°C	28-PIN CERDIP	Common Anode
ICM7218BIJI	−40°C to +85°C	28-PIN CERDIP	Common Cathode
ICM7218CIJI	−40°C to +85°C	28-PIN CERDIP	Common Anode
ICM7218DIJI	−40°C to +85°C	28-PIN CERDIP	Common Cathode

NOTE: All typical values have been characterized but are not tested

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6V
Digit Output Current 300mA
Segment Output Current 50mA
Input Voltage
(any terminal) .... V_{SS} $-0.3V$ to $V_{DD} + 0.3V$
(Note 1)

Power Dissipation (28 Pin CERDIP) .... 1 W (Note 2)
Operating Temperature Range .... −40°C to +85°C
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (Soldering, 10sec) .... 300°C

NOTE 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that no inputs from sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7218 should be turned on first.

2: These limits refer to the package and will not be obtained during normal operation. Derate above 50°C by 25mW per °C.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

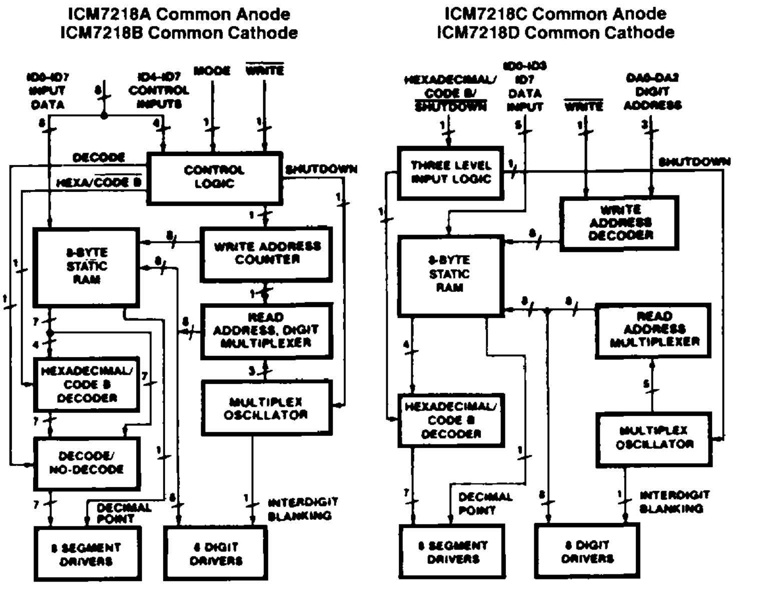

Figure 1: Functional Diagrams

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NOTE: All typical values have been characterized but are not tested

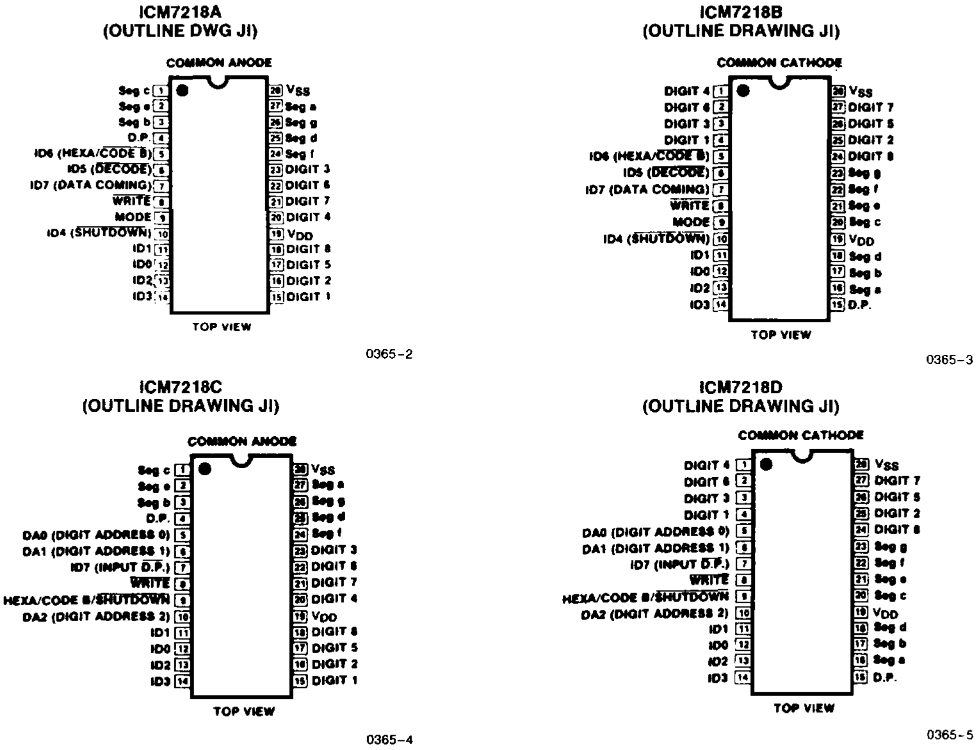

Figure 2: Pin Configurations

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS $V_{DD} = 5V$, $V_{SS} = 0V$, $T_A = 25°C$, Display Diode drop = 1.7V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SUPPLY}	Supply Voltage Range	Operating Power Down Mode	4 2		6 6	V V
I_Q	Quiescent Supply Current	Shutdown (Note 3)	6	10	300	μA
I_{DD}	Operating Supply Current	Common Anode SEGS On / SEGS Off; Common Cathode SEGS On / SEGS Off — Outputs Open Circuit Note 4			2.5 500 700 500	mA μA μA μA
I_{DIG}	Digit Drive Current	Common Anode $V_{out} = V_{DD} - 2.0V$ Common Cathode $V_{out} = V_{SS} + 1.0V$	140 50	200 100		mA mA
I_{DLK}	Digit Leakage Current	Shutdown Mode Common Anode $V_{out} = 2V$ Common Cathode $V_{out} = 5V$			100 100	μA μA
I_{SEG}	Peak Segment Drive Current	Common Anode $V_{out} = V_{SS} + 1.0V$ Common Cathode $V_{out} = V_{DD} - 2.0V$	20 −10	40 −20		mA mA
I_{SLK}	Segment Leakage Current	Shutdown Mode Common Anode $V_{out} = V_{DD}$ Common Cathode $V_{out} = V_{SS}$			100 100	μA μA
f_{MUX}	Display Scan Rate	Per Digit		250		Hz
 V_{IH} V_{IF} V_{IL} Z_{IN}	Three Level Input: Pin 9 ICM7218C/D Logical "1" Input Voltage Floating Input Logical "0" Input Voltage Three Level Input Impedance	 Hexadecimal Code B Shutdown Note 3	 4.5 2.0	 100	 3.0 0.4	 V V V kΩ
V_{IH} V_{IL}	Logical "1" Input Voltage Logical "0" Input Voltage		3.5		 0.8	V V
t_{WL}	Write Pulse Width (Low)	7218A, B	550	400		ns
t_{WL}	Write Pulse Width (Low)	7218C, D	400	250		ns
t_{MH}	Mode Hold Time	7218A, B	150			ns
t_{MS}	Mode Set Up Time	7218A, B	500			ns
t_{DS}	Data Set Up Time		500			ns
t_{DH}	Data Hold Time	7218 A, B 7218 C, D	50 125			ns ns
t_{AS} t_{AH}	Digit Address Set Up Time Digital Address Hold Time	ICM7218C, D ICM7218C, D	500 0			ns ns
Z_{IN}	Data Input Impedance	5-10 pF Gate Capacitance		10^{10}		Ohms

NOTE: All typical values have been characterized but are not tested.

TABLE 1: INPUT DEFINITIONS ICM7218A and B

Input		Terminal	Logic Level	Function
$\overline{\text{WRITE}}$		8	High Low	Input Not Loaded Input Loaded
MODE		9	High Low	Load Control bits on Write Pulse Load Input Data on Write Pulse
ID4 $\overline{\text{SHUTDOWN}}$	MODE High	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Display Disabled)
ID5 ($\overline{\text{DECODE}}$)	MODE High	6	High Low	No Decode Decode
ID6 (HEXA/$\overline{\text{CODE B}}$)	MODE High	5	High Low	Hexadecimal Decoding Code B Decoding
ID7 (DATA COMING)	MODE High	7	High Low	Data Coming No Data Coming } Control Word
ID0-ID7	MODE Low	11,12,13,14, 5,6,10,7		Display Data Inputs (Notes 4, 5)

TABLE 2: INPUT DEFINITIONS ICM7218C and D

Input	Terminal	Logic Level	Function
$\overline{\text{WRITE}}$	8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
HEXA/CODE B/$\overline{\text{SHUTDOWN}}$	9 (Note 3)	High Floating Low	Hexadecimal Decoding Code B Decoding Shutdown (Oscillator, Decoder and Display Disabled)
DA0 – DA2	10,6,5		Digit Address Inputs
ID0 – ID3 ID (INPUT $\overline{\text{D.P.}}$)	14,13,11,12 7		Display Data Inputs Decimal Point Input

NOTE 3: In the ICM7218C and D (random access versions) the HEXA/CODE B/$\overline{\text{SHUTDOWN}}$ Input (Pin 9) has internal biasing resistors to hold it at $V_{DD}/2$ when Pin 9 is open circuited. These resistors consume power and result in a quiescent supply current (I_Q) of typically 50μA.
The ICM7218A, B, and E devices do not have these biasing resistors and thus are not subject to this condition.

4: ID0-ID3 = Don't care when writing control data
ID4-ID6 = Don't care when writing Hex/Code B data
ID7 = Decimal Point data
(The display blanks on ICM7218A/B versions when writing in data)

5: In the No Decode format, "Ones" represents "on" segments for all inputs except for the Decimal Point, where "Zero" represents an "on" segment, (i.e. segments are positive true, decimal point is negative true).

6: Common Anode segment drivers and Common Cathode Digit Drivers have 20kΩ pullup resistors.

NOTE: All typical values have been characterized but are not tested.

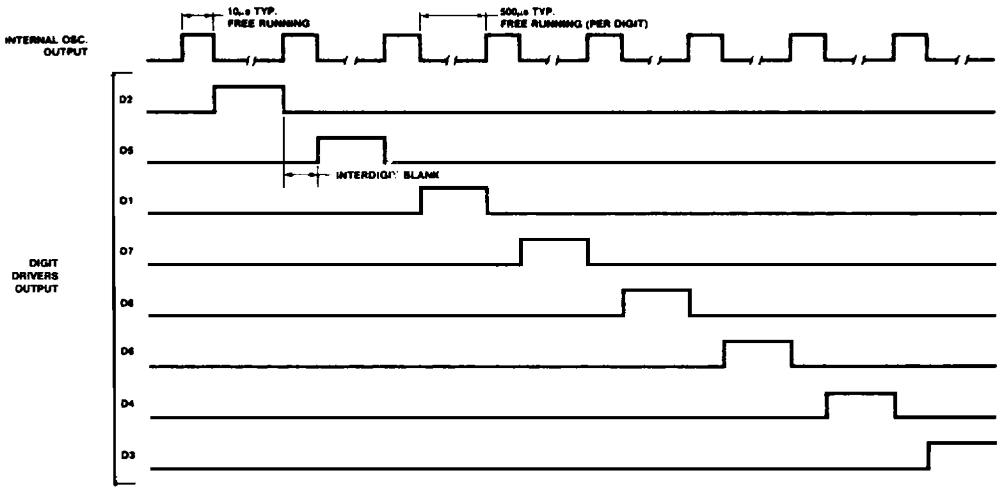

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Figure 3: Multiplex Timing (Common Cathode Version)

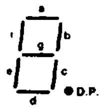

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Figure 4: Segment Assignments

DETAILED DESCRIPTION

DECODE Operation

For the ICM7218A/B products, there are 3 input data formats possible; either direct segment and decimal point information (8 bits per digit) or two Binary code plus decimal point information (Hexadecimal/Code B formats with 5 bits per digit).

NOTE: All typical values have been characterized but are not tested.

The 7 segment decoder on chip is disabled when direct segment information is to be written. In this format, the inputs directly control the outputs as follows:

Input Data: ID7 ID6 ID5 ID4 ID3 ID2 ID1 ID0

Output Segments: $\overline{\text{D.P.}}$ a b c e g f d

Here, "Ones" represent "on" segments for all inputs except the Decimal Point. For the Decimal Point "zero" represents an "on" segment.

HEXAdecimal/CODE B Decoding

For all products, a choice of either HEXA or Code B decoding may be made, HEXA decoding provides 7 segment numeric plus six alpha characters while Code B provides a negative sign (−), a blank (for leading zero blanking), certain useful alpha characters and all numeric formats.

The four bit binary code is set up on inputs ID3-ID0, and decimal point data is set up on ID7.

Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
HEXA CODE	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F
CODE B	0	1	2	3	4	5	6	7	8	9	-	E	H	L	P	(BLANK)

$\overline{\text{SHUTDOWN}}$

$\overline{\text{SHUTDOWN}}$ performs several functions: it puts the device into a very low dissipation mode (typically 10μA at V_{DD} = 5V), turns off both the digit and segment drivers, and stops the multiplex scan oscillator (this is the only way the scan oscillator can be disabled). However, it is still possible to input data to the memory during shutdown — only the display output sections of the device are disabled in this mode.

Powerdown

In the Shutdown Mode, the supply voltage may be reduced to 2 volts without data in memory being lost. However, data should not be written into memory if the supply voltage is less than 4 volts.

Output Drive

The common anode output drive is approximately 200 mA per digit at a 12% duty cycle. With segment peak drive current of 40mA typically, this results in 5mA average drive. The common cathode drive capability is approximately one half that of the common anode drive. If high impedance LED displays are used, the drive current will be correspondingly less.

Inter Digit Blanking

A blanking time of approximately 10μs occurs between digit strobes. This ensures that the segment information is correct before the next digit drive, thereby avoiding display ghosting.

Driving Larger Displays

If a higher average drive current per digit is required, it is possible to connect digit drive outputs together. For example, by paralleling pairs of digit drives together to drive a 4 digit display, 5mA average segment drive current can be obtained.

Power Dissipation Considerations

Assuming common anode drive at V_{DD} = 5 volts and all digits on with an average of 5 segments driven per digit, the average current would be approximately 200mA. Assuming a 1.8 volt drop across the LED display, there will be a 3.2 volt drop across the ICM7218. The device power dissipation will therefore be 640mW, rising to about 900mW, for all '8' 's displayed. **Caution: Position device in system such that air can flow freely to provide maximum cooling. The common cathode dissipation is approximately one half that of the common anode dissipation.**

Sequential Addressing Considerations (ICM7218A/B)

The control instructions are read from the input bus lines if MODE is high and $\overline{\text{WRITE}}$ low. The instructions occur on 4 lines and are — $\overline{\text{DECODE}}$/no Decode, type of Decode (if desired), $\overline{\text{SHUTDOWN}}$/no Shutdown and DATA COMING/not Coming. After the control word has been written (with the Data Coming instruction), display data can be written into memory with each successive negative going $\overline{\text{WRITE}}$ pulse. After all 8 digit memory locations have been written to, additional transitions of the $\overline{\text{WRITE}}$ input are ignored until a new control word is written. It is not possible to change one individual digit without refreshing the data for all the other digits.

Random Access Input Drive Considerations (ICM7218C/D)

Control instructions are provided to the ICM7218C/D by a single three level input terminal (Pin 9), which operates independently of the $\overline{\text{WRITE}}$ pulse.

Data can be written into memory on the ICM7218C/D by setting up a 3 bit binary code (one of eight) on the digit address inputs and applying a low level to the $\overline{\text{WRITE}}$ pin. For example, it is possible to change only digit 7 without altering the data for the other digits. (See Figure 7).

Supply Capacitor

A 0.1μF plus a 47μF capacitor is recommended between V_{DD} and V_{SS} to bypass display multiplexed noise.

NOTE: All typical values have been characterized but are not tested.

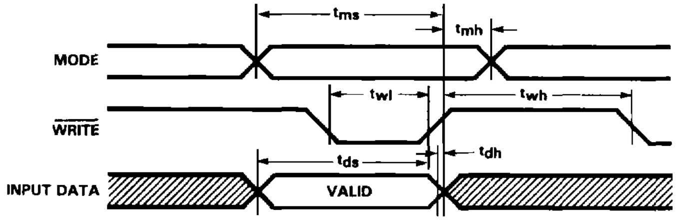


Figure 5: Timing Diagram for ICM7218A/B

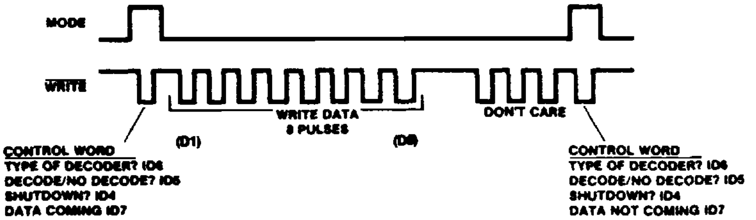


Figure 6: Load Sequence ICM7218A/B

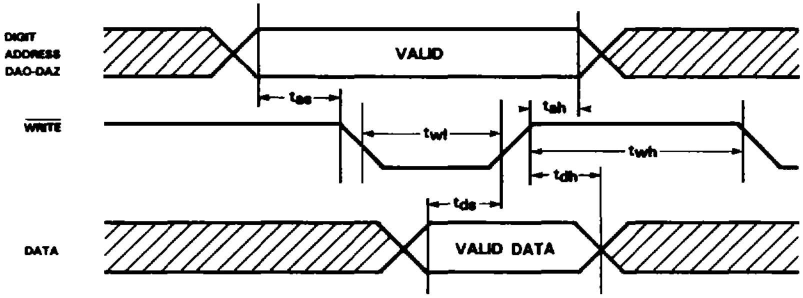


Figure 7: Timing Diagram for ICM7218C/D

NOTE: All typical values have been characterized but are not tested.

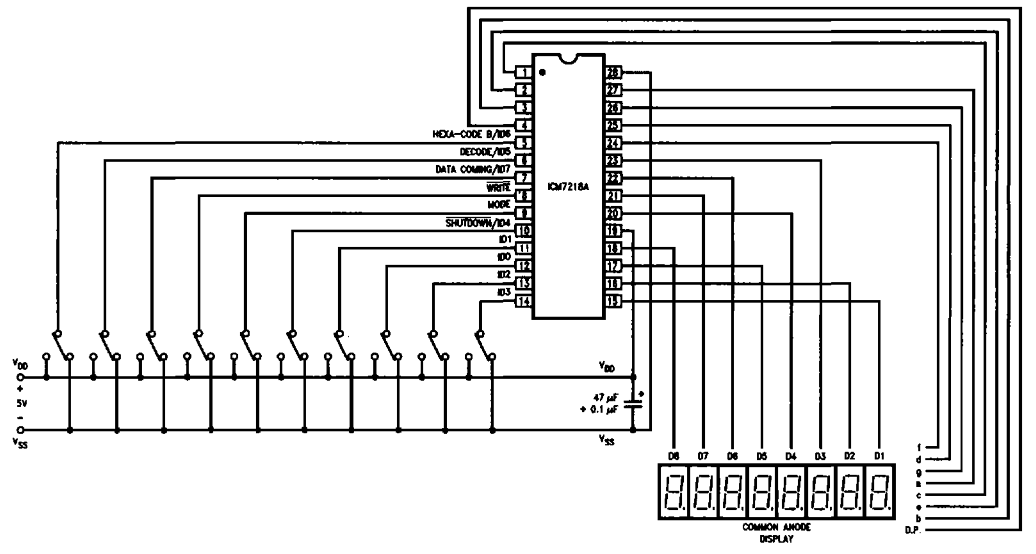


Figure 8: Functional Test Circuit (# 1)

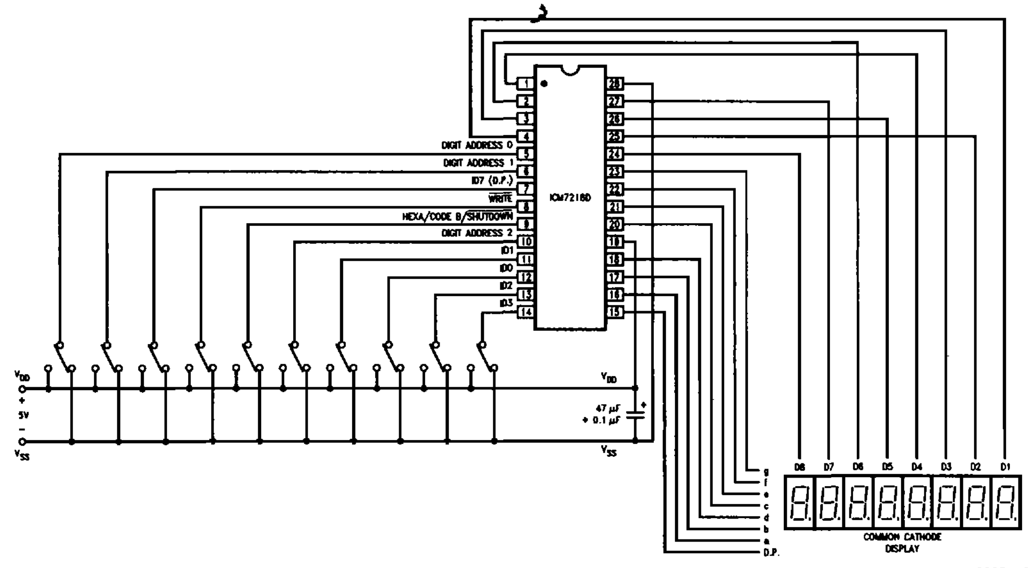
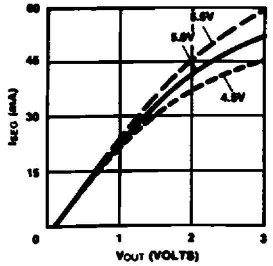


Figure 9: Functional Test Circuit (# 2)

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

COMMON ANODE SEG. DRIVER
I_{SEG} vs. V_{OUT} AT 25°C



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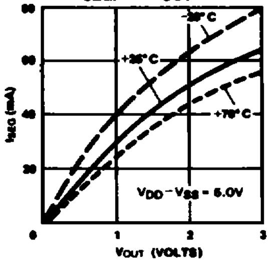
COMMON ANODE SEG. DRIVER
$I_{SEG.}$ vs. V_{OUT}



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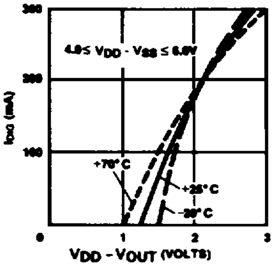
COMMON ANODE DIGIT DRIVER
I_{DIG} vs. $(V_{DD} - V_{OUT})$



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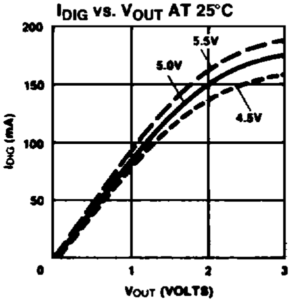
COMMON CATHODE DIGIT DRIVER
I_{DIG} vs. V_{OUT} AT 25°C



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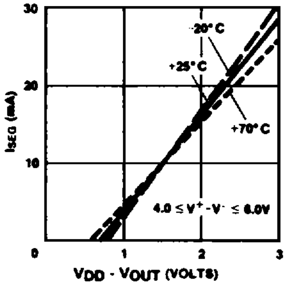
COMMON CATHODE SEG. DRIVER
I_{SEG} vs. $(V_{DD} - V_{OUT})$



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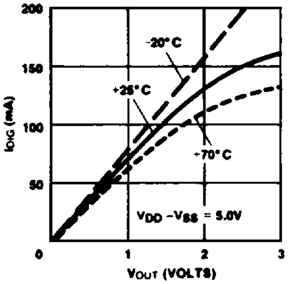
COMMON CATHODE DIGIT DRIVER
I_{DIG} vs. V_{OUT}



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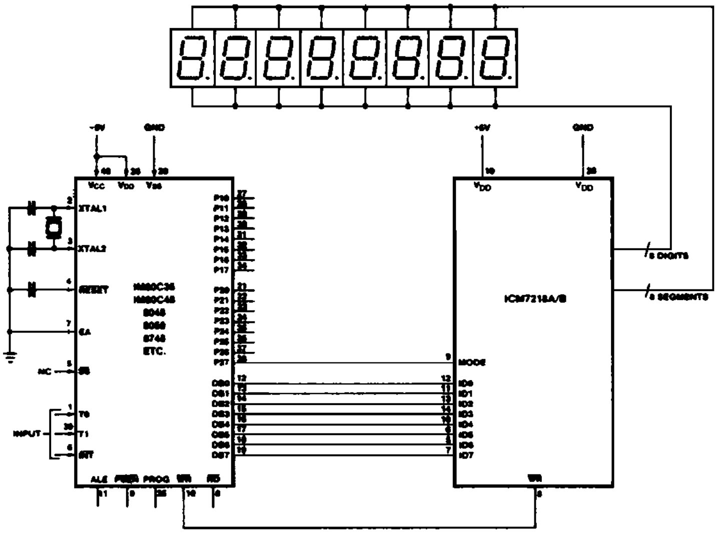

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Figure 10: 8 Digit Microprocessor Display

NOTE: All typical values have been characterized but are not tested.

APPLICATION EXAMPLES

8 DIGIT MICROPROCESSOR DISPLAY APPLICATION

Figure 10 shows a display interface using the ICM7218A/B with an 8048 family microcontroller. The 8 bit data bus (DB0/DB7-ID0/ID7) transfers control and data information to the 7218 display interface on successive $\overline{\text{WRITE}}$ pulses. The MODE input to the 7218 is connected to one of the I/O port pins on the microcontroller. When MODE is high a control word is transferred; when MODE is low data is transfered. Sequential locations in the 8-byte static memory are automatically loaded on each successive $\overline{\text{WRITE}}$ pulse. After eight $\overline{\text{WRITE}}$ pulses have occurred, further pulses are ignored until a new control word is transferred. (See Figure 6). This also allows writing to other peripheral devices without disturbing the ICM7218A/B.

16 DIGIT MICROPROCESSOR DISPLAY

In this application (see Figure 11), both ICM7218's are addressed simultaneously with a 3 bit word, DA2-DA0. Display data from the 8048 I/O bus (DB7-DB0) is transferred to both ICM7218's simultaneously.

The display digits from both ICM7218's are interleaved to allow adjacent pairs of digits to be loaded simultaneously from a single 8 bit data bus.

Decimal point information is supplied to the ICM7218's from the processor on port lines P26 and P27.

NO DECODE APPLICATION

The ICM7218 can also be used as a microprocessor based LED status panel driver. The microprocessor selected control word must include "No Decode" and "Data Coming". The processor writes "Ones" and "Zeroes" into the ICM7218 which in turn directly drives appropriate discrete LEDs. LED indicators can be red or green (8 segments $\times$ 8 digits $=$ 64 dots $\div$ 2 per red or green $=$ 32 channels).

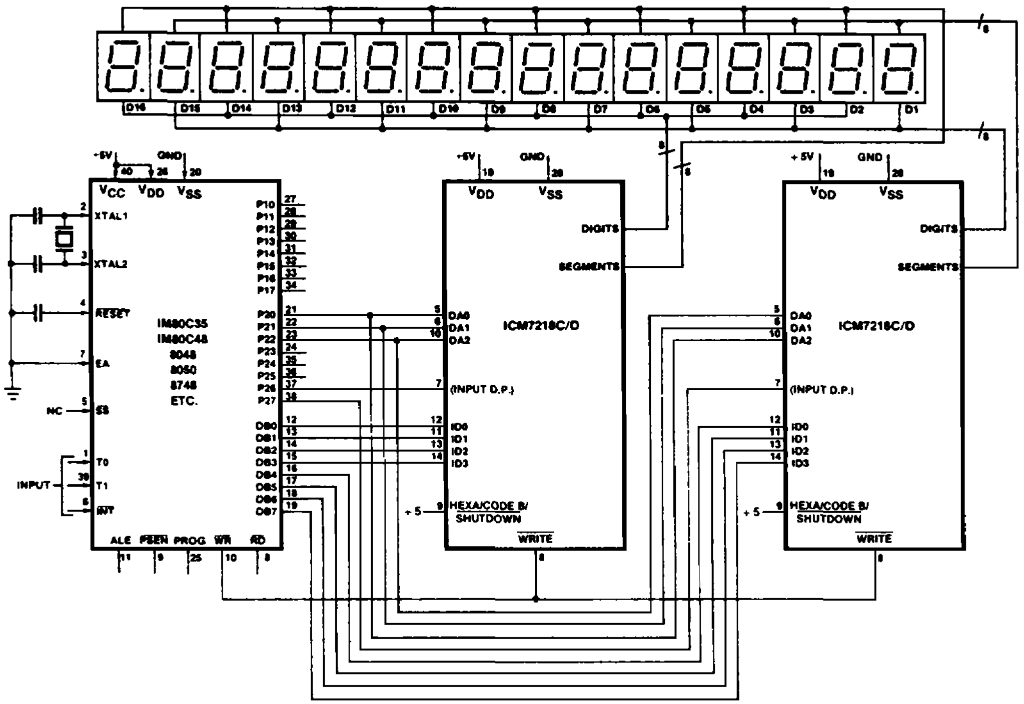

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Figure 11: 16 Digit Display

NOTE: All typical values have been characterized but are not tested.