National Semiconductor

MICROCIRCUIT DATA SHEET

MNDM54LS374-X REV 0A0

Original Creation Date: 08/20/97
Last Update Date: 07/10/02
Last Major Revision Date: 08/20/97

OCTAL D -TYPE FLIP-FLOP with TRI-STATE OUTPUTS

General Description

The 'LS374 is a high-speed, low power octal D - type flip-flop featuring separate D - type inputs for each flip-flop and tri-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (/OE) are common to all flip-flops.

Industry Part Number

54LS374

Prime Die

L374

NS Part Numbers

DM54LS374E/883
DM54LS374J-MLS
DM54LS374J/883
DM54LS374W/883

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Edge-triggered D - type inputs
- Buffered Positive Edge-triggered Clock
- Tri-state outputs for Bus-oriented applications

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Junction Temperature under Bias	-55C to +175C
Vcc Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage	-0.5V to +10.0V
Current Applied to Output in LOW State (Max)	twice the rated Iol(mA)

Note 1: Absolute Maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55 C to +125 C
Supply Voltage	
Military	+4.5V to +5.5V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp range: -55C to 125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input High Current	VCC=5.5V, VM=2.7V, VINH=4.5V	1, 3	INPUTS		20	uA	1, 2, 3
IBVI	Input High Current	VCC=5.5V, VM=10.0V, VINH=4.5V	1, 3	INPUTS		100	uA	1, 2, 3
IIL	Input LOW Current	VCC=5.5V, VM=0.4V, VINH=4.5V	1, 3	INPUTS	-30	-400	uA	1, 2, 3
IIL 2	Input LOW Current	VCC=5.5V, VM=0.4V, VINH=4.5V	1, 3	$\overline{OE}$, CP	-0.5	-400	uA	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, VIL=0.7V, IOL=12.0mA, VINH=4.5V	1, 3	OUTPUTS		0.4	V	1, 2, 3
VOH	Output HIGH Voltage	VCC= 4.5V, VIH=2.0V, IOH=-3.0mA, VINL=0.0V	1, 3	OUTPUTS	2.4		V	1, 2, 3
VOH 2	Output HIGH Voltage	VCC= 4.5V, VIH=2.0V, IOH=-12.0mA, VINL=0.0V, VIL=0.7V	1, 3	OUTPUTS	2		V	1, 2, 3
IOS	Short Circuit Current	VCC=5.5V, VINH=4.5V, VINL=0.0V, VOUT=0.0V	1, 3	OUTPUTS	-50	-225	mA	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IM=-18mA, VINH=4.5V	1, 3	INPUTS		-1.5	V	1, 2, 3
ICCZ	Supply Current	VCC=5.5V, VINH=4.5V	1, 3	VCC		45	mA	1, 2, 3
IOZH	Output Current	VCC=5.5V, VM=2.7V, VINL=0.0V, VINH=4.5V, VIH=2.0V	1, 3	OUTPUTS		20	uA	1, 2, 3
IOZL	Output Current	VCC=5.5V, VM=0.4V, VINH=4.5V, VIH=2.0V	1, 3	OUTPUTS		-20	uA	1, 2, 3

Electrical Characteristics

AC PARAMETERS - Standard Load

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Temp range: +25C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH	Propagation Delay	VCC=5.0V, CL=50pF	5	CP to On		28	ns	9
tpHL	Propagation Delay	VCC=5.0V, CL=50pF	5	CP to On		34	ns	9
tpZH	Output Enable	VCC=5.0V, CL=50pF, RL=667 ohms, R=5k ohms	5	$\overline{OE}$ to On		28	ns	9
tpZL	Output Enable	VCC=5.0V,CL=50pF, RL=667 ohms, R=5k ohms	5	$\overline{OE}$ to On		28	ns	9
tpHZ	Output Disable	VCC=5.0V, CL=5pF, RL=667 ohms, R=5k ohms	5	$\overline{OE}$ to On		20	ns	9
tpLZ	Output Disable	VCC=5.0V, CL=5pF, RL=667 ohms, R=5k ohms	5	$\overline{OE}$ to On		25	ns	9
ts(H/L)	Setup Time	VCC=5.0V	5	Dn to CP	20		ns	9
th(H/L)	Hold Time	VCC=5.0V	5	Dn to CP	5		ns	9
tw(H/L)	Pulse Width	VCC=5.0V	5	CP	15		ns	9
fMAX	Maximum Clock Frequency	VCC=5.0V	5	CP	35		MHZ	9

Electrical Characteristics

AC PARAMETERS - Alternate Load

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pF, RL=110 ohms, R=2.4kohms::Temp range: -55C to +125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH	Propagation Delay	VCC=5.0V	2, 4	CP to On	2	28	ns	9
			2, 4	CP to On	2	41	ns	10, 11
tpHL	Propagation Delay	VCC=5.0V	2, 4	CP to On	2	34	ns	9
			2, 4	CP to On	2	49	ns	10, 11
tpZH	Output Enable	VCC=5.0V	2, 4	$\overline{OE}$ to On	2	28	ns	9
			2, 4	$\overline{OE}$ to On	2	48	ns	10, 11
tpZL	Output Enable	VCC=5.0V	2, 4	$\overline{OE}$ to On	2	28	ns	9
			2, 4	$\overline{OE}$ to On	2	39	ns	10, 11
tpHZ	Output Disable	VCC=5.0V	2, 4	$\overline{OE}$ to On	2	33	ns	9
			2, 4	$\overline{OE}$ to On	2	46	ns	10, 11
tpLZ	Output Disable	VCC=5.0V	2, 4	$\overline{OE}$ to On	2	34	ns	9
			2, 4	$\overline{OE}$ to On	2	58	ns	10, 11
Ts (H/L)	Set-up time	VCC=5.0V	2, 4	Dn to CP	20		ns	9
			2, 4	Dn to CP	25		ns	10, 11
Th (H/L)	Hold time	VCC=5.0V	2, 4	Dn to CP	5		ns	9
			2, 4	Dn to CP	10		ns	10, 11
Tw (H/L)	Pulse width	VCC=5.0V	2, 4	CP	15		ns	9
			2, 4	CP	20		ns	10, 11
Fmax	Maximum clock frequency	VCC=5.0V	2, 4	CP	35		MHZ	9
			2, 4	CP	30		MHZ	10, 11

Note 1: Screen tested 100% on each device at +25C, +125C & -55C temperature, subgroups A1, 2, 3, 7 & 8.
Note 2: Screen tested 100% on each device at +25C temperature only, subgroup A9.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C & -55C temperature, subgroups A1, 2, 3, 7 & 8.

(Continued)

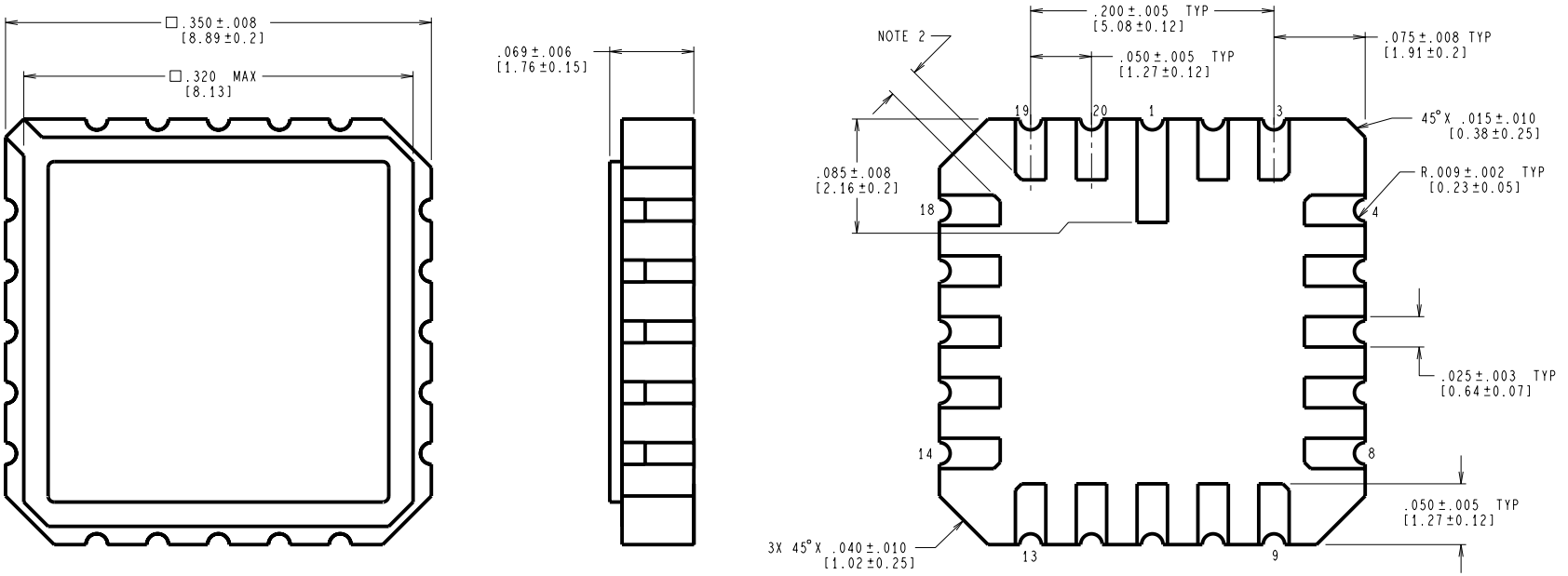
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C subgroup A9, and periodically at +125C & -55C, subgroups 10 & 11.
Note 5: GUARANTEED, NOT TESTED. (Design characterization data)
Note 6: NATIONAL TESTS TRI-STATE PROPAGATION DELAYS USING AN EQUIVALENT LOAD WITH CORRELATED LIMITS.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
W20ARF	CERPACK (W), 20 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

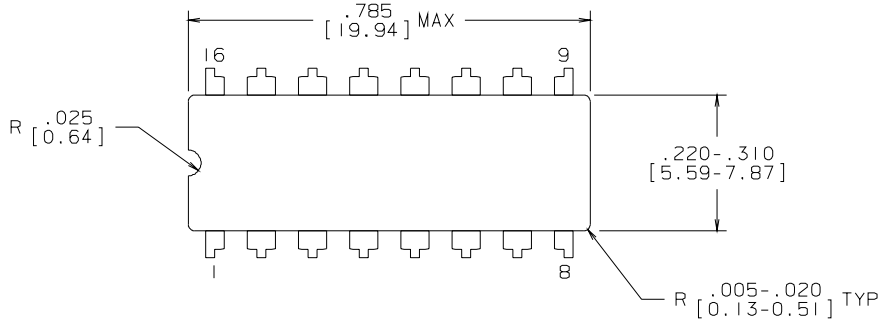
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

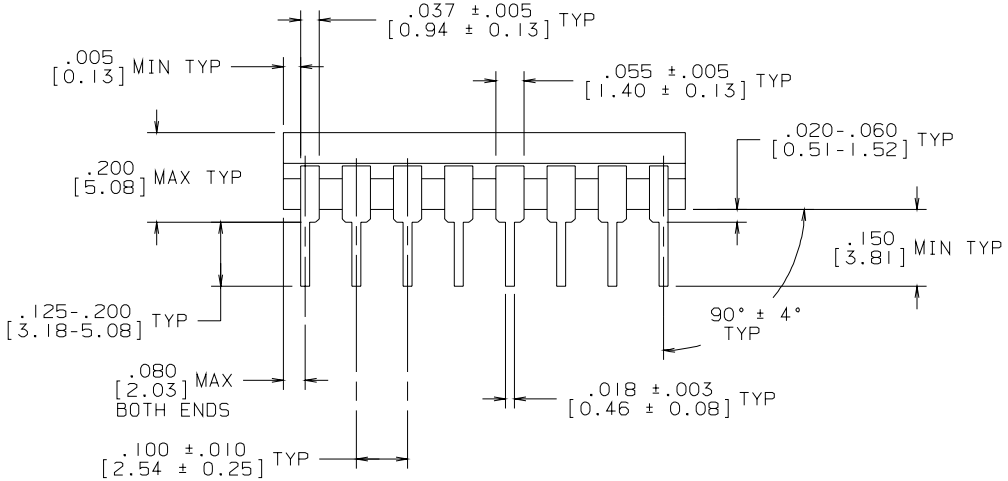
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

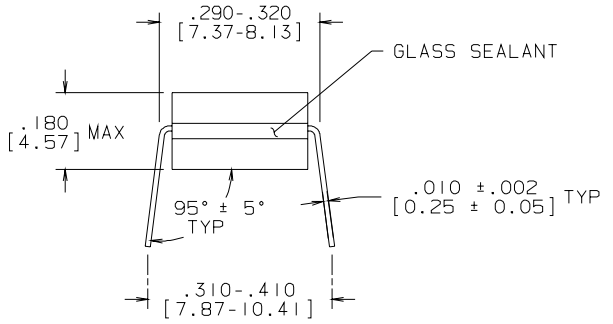
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 16 LEAD

PROJECTION

INCH [MM]

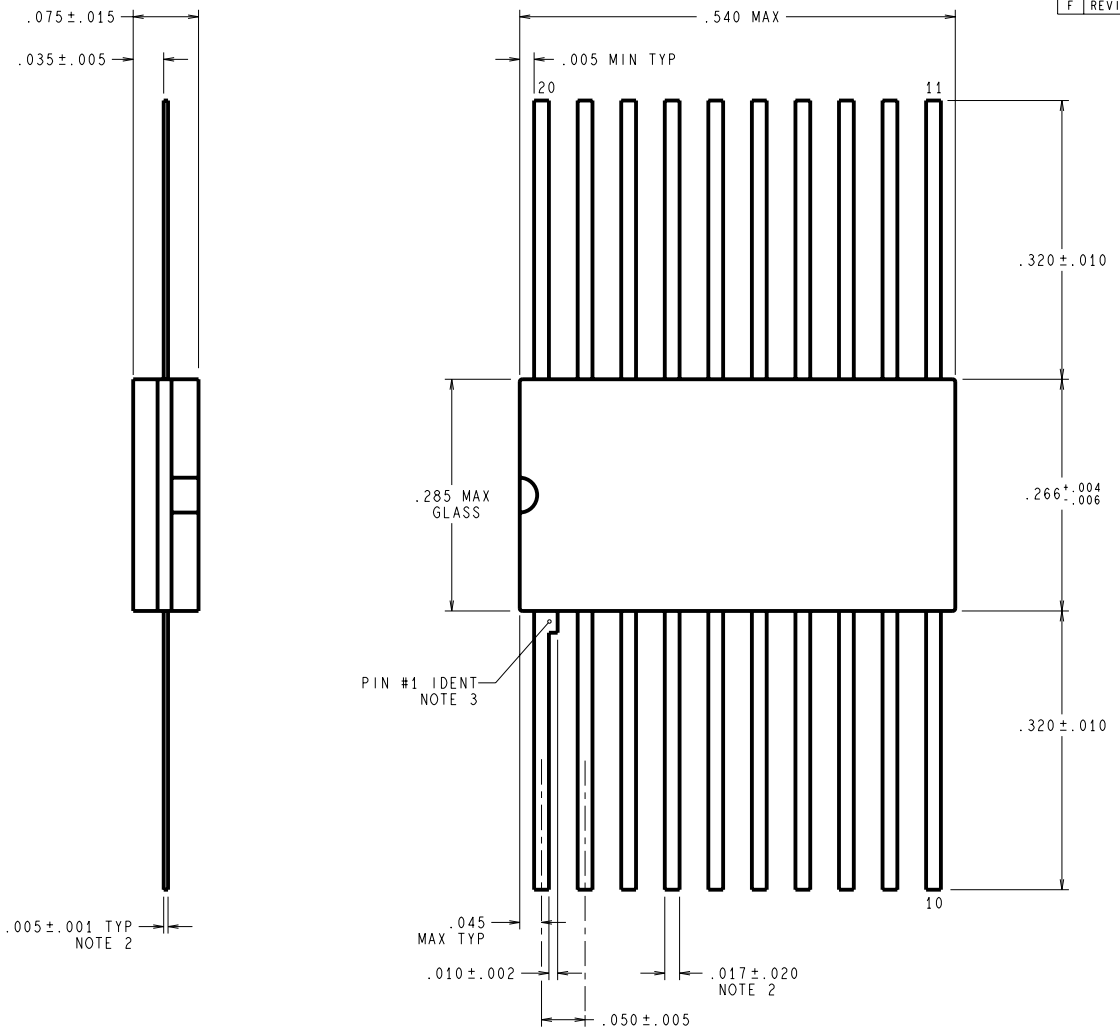
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J16A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE AND REDRAW PER NEW STANDARD.	10512	07/28/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. NO JEDEC REGISTRATION AS OF 02/70/94.

MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 20 LEAD

PROJECTION — INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W20A	F

DO NOT SCALE DRAWING — SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0002477	07/10/02	Rose Malone	Initial MDS Release: MNDM54LS374-X, Rev. 0A0. Conversion from Table 1 Data Sheet: 54LS374, Rev. C0.2