

## 1. Overview

The M32C/83 group microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/83 group is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It incorporates a multiplier and DMAC adequate for office automation, communication devices and industrial equipments and other high-speed processing applications.

### 1.1 Applications

Audio, cameras, office equipment, communications equipment, portable equipment, etc.

## 1.2 Performance Outline

Tables 1.1 and 1.2 list performance outlines of the M32C/83 group.

**Table 1.1 M32C/83 Group Performance (144-Pin Package)**

Item		Performance
CPU	Basic instructions	108 instructions
	Shortest instruction execution time	31.3 ns (f(BCLK)=32 MHz, Vcc=4.2 V to 5.5 V) <sup>(1)</sup> 50 ns (f(BCLK)=20 MHz, Vcc=3.0 V to 5.5 V)
	Operation mode	Single-chip mode, Memory expansion mode and Microprocessor mode
	Address space	16 Mbytes
	Memory capacity	See Table 1.3
Peripheral function	Port	123 I/O pins and 1 input pin
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function: 16 bits x 12 channels Waveform generating function: 16 bits x 28 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus <sup>(2)</sup> , 8-bit or 16-bit clock synchronous serial I/O)
	Serial I/O	5 channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus <sup>(2)</sup> , I <sup>2</sup> C bus <sup>(3)</sup>
	CAN module	1 channel Supporting CAN 2.0B specification
	A/D converter	10-bit A/D converter: 2 circuits, 34 channels
	D/A converter	8 bits x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt factors Immediate transfer, Calculation transfer and Chain transfer functions
	DRAMC	CAS-before-RAS refresh, Self-refresh, EDO, FP
	CRC calculation circuit	CRC-CCITT
	XY converter	16 bits x 16 bits
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	42 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock generating circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (* )Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally
	Oscillation stop detect function	Main clock oscillation stop detect function
	Electric characteristics	Supply voltage
Power consumption		41 mA (Vcc=5 V, f(BCLK)=32 MHz) 38 mA (Vcc=5 V, f(BCLK)=30 MHz) 26 mA (Vcc=3.3 V, f(BCLK)=20 MHz) 470 μA (Vcc=5 V, f(XCIN)=32 kHz, in wait mode) 340 μA (Vcc=3.3 V, f(XCIN)=32 kHz, through VDC in wait mode) 5.0 μA (Vcc=3.3 V, f(XCIN)=32 kHz, not through VDC in wait mode) 0.4 μA (Vcc=5 V, f(XCIN)=32 kHz, in stop mode) 0.4 μA (Vcc=3.3 V, f(XCIN)=32 kHz, in stop mode)
Flash memory	Program/erase supply voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V
	Program and erase endurance	100 cycles
Operating ambient temperature		-20 to 85°C, -40 to 85°C (optional)
Package		144-pin plastic molded LQFP

NOTES:

- Contact Renesas Technology Sales Co., Ltd. to use this microcomputer with an operating frequency higher than 30 MHz.
- IEBus is a trademark of NEC Electronics Corporation.
- I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.

All options are on a request basis.

**Table 1.2 M32C/83 Group Performance (100-Pin Package)**

Item		Performance
CPU	Basic instructions	108 instructions
	Shortest instruction execution time	31.3 ns (f(BCLK)=32 MHz, V <sub>CC</sub> =4.2 V to 5.5 V) <sup>(1)</sup> 50 ns (f(BCLK)=20 MHz, V <sub>CC</sub> =3.0 V to 5.5 V)
	Operation mode	Single-chip mode, Memory expansion mode and Microprocessor mode
	Address space	16 Mbytes
	Memory capacity	See Table 1.3
Peripheral function	Port	87 I/O pins and 1 input pin
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function: 16 bits x 5 channels Waveform generating function: 16 bits x 10 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus <sup>(2)</sup> , 8-bit or 16-bit clock synchronous serial I/O)
	Serial I/O	5 channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus <sup>(2)</sup> , I <sup>2</sup> C bus <sup>(3)</sup>
	CAN module	1 channel Supporting CAN 2.0B specification
	A/D converter	10-bit A/D converter: 2 circuits, 26 channels
	D/A converter	8 bits x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt factors Immediate transfer, Calculation transfer and Chain transfer functions
	DRAMC	CAS-before-RAS refresh, Self-refresh, EDO, FP
	CRC calculation circuit	CRC-CCITT
	XY converter	16 bits x 16 bits
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	42 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock generating circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (* )Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally
	Oscillation stop detect function	Main clock oscillation stop detect function
	Electric characteristics	Supply voltage
Power consumption		41 mA (V <sub>CC</sub> =5 V, f(BCLK)=32 MHz) 38 mA (V <sub>CC</sub> =5 V, f(BCLK)=30 MHz) 26 mA (V <sub>CC</sub> =3.3 V, f(BCLK)=20 MHz) 470 μA (V <sub>CC</sub> =5 V, f(XCIN)=32 kHz, in wait mode) 340 μA (V <sub>CC</sub> =3.3 V, f(XCIN)=32 kHz, through VDC in wait mode) 5.0 μA (V <sub>CC</sub> =3.3 V, f(XCIN)=32 kHz, not through VDC in wait mode) 0.4 μA (V <sub>CC</sub> =5 V, f(XCIN)=32 kHz, in stop mode) 0.4 μA (V <sub>CC</sub> =3.3 V, f(XCIN)=32 kHz, in stop mode)
Flash memory	Program/erase supply voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V
	Program and erase endurance	100 cycles
Operating ambient temperature		-20 to 85°C, -40 to 85°C (option)
Package		100-pin plastic molded LQFP/QFP

## NOTES:

1. Contact Renesas Technology Sales Co., Ltd. to use this microcomputer with an operating frequency higher than 30 MHz.
2. IEBus is a trademark of NEC Electronics Corporation.
3. I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.

All options are on a request basis.

### 1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/83 group microcomputer.

The M32C/83 group microcomputer contains ROM and RAM as memory to store instructions and data, CPU to execute calculations and peripheral functions such as interrupt, timer, serial I/O, DMAC, CRC calculation circuit, A/D converter, D/A converter, DRAMC, intelligent I/O and ports.

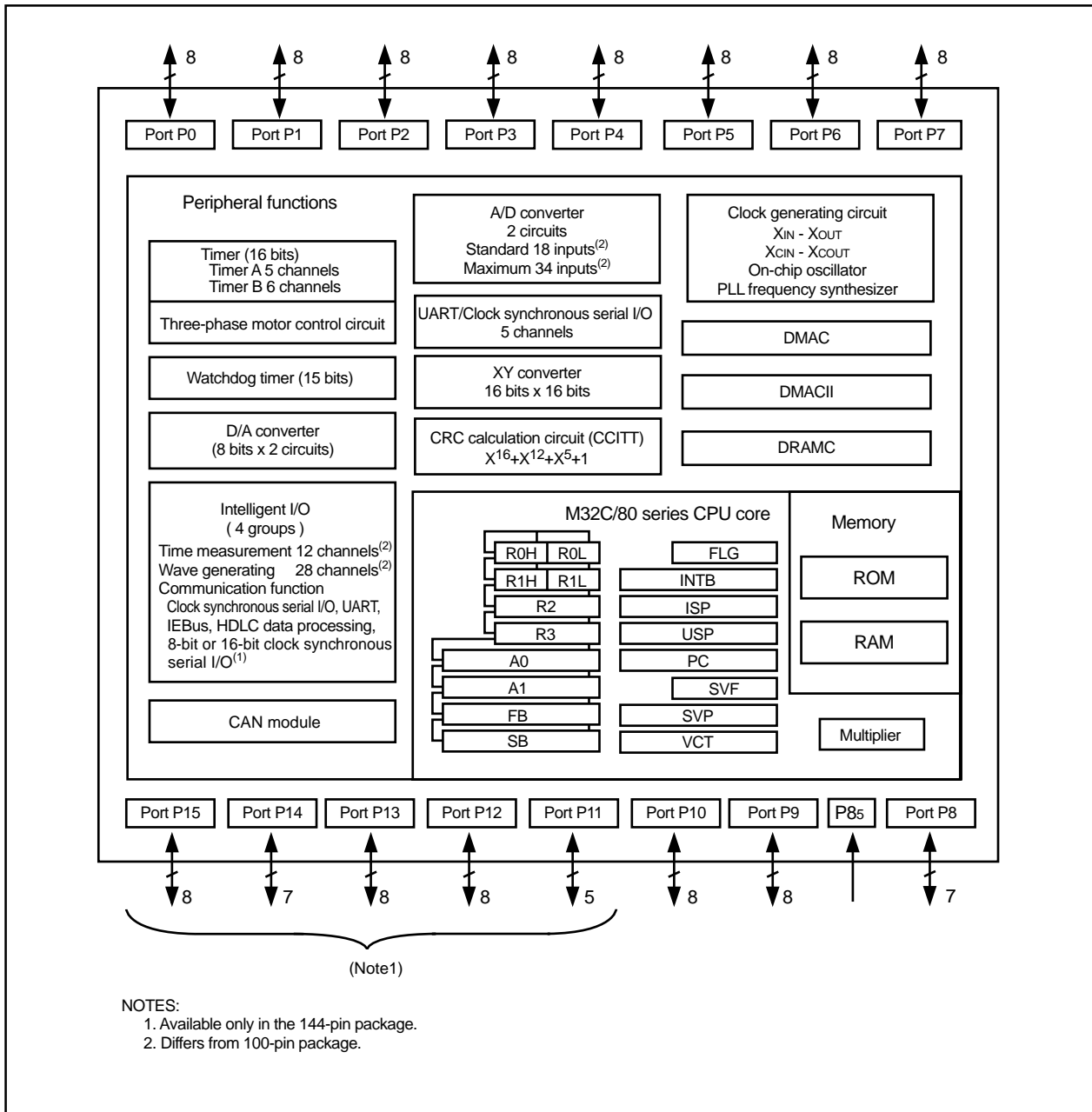


Figure 1.1 M32C/83 Group Block Diagram

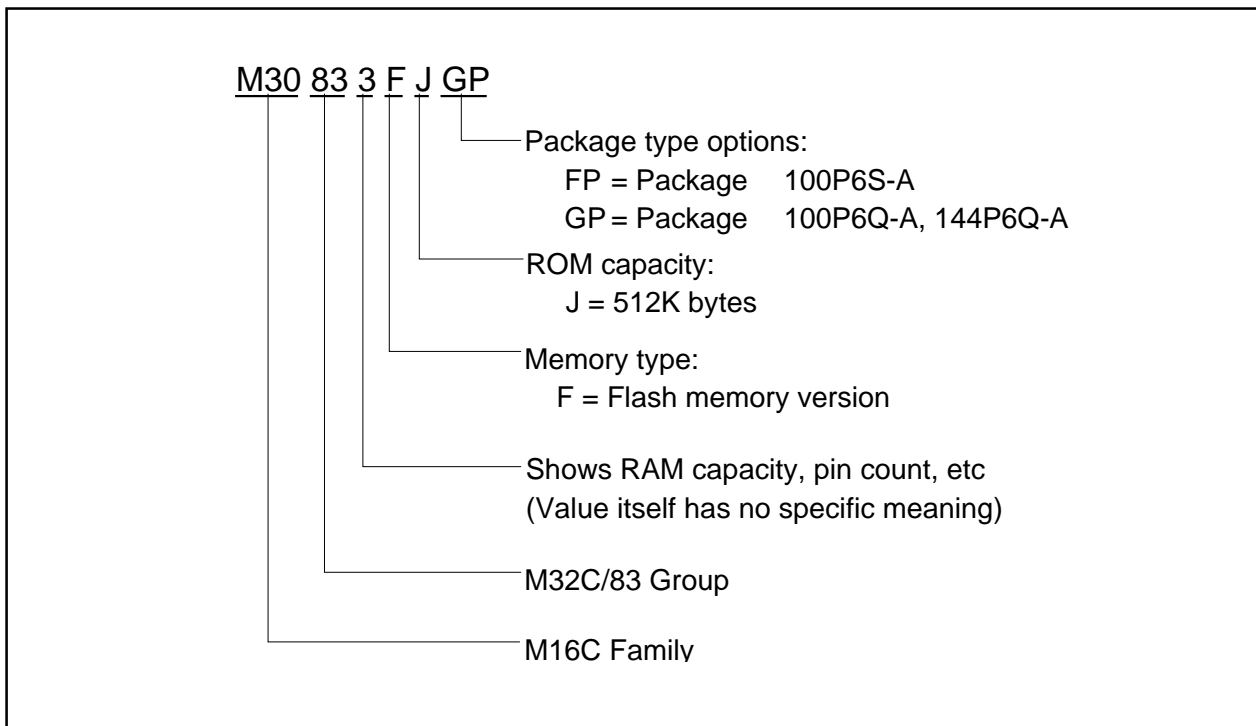
### 1.4 Product Information

Renesas plans to release the following products in the M32C/83 group:

- (1) Support for the flash memory version
- (2) ROM/RAM capacity
- (3) Package
  - 100P6S-A : Plastic molded QFP
  - 100P6Q-A : Plastic molded LQFP
  - 144P6Q-A : Plastic molded LQFP

**Table 1.3 M32C/83 Group**

Type number	ROM capacity	RAM capacity	Package type	Remarks
M30835FJGP	512K	31K	144P6Q-A	Flash memory
M30833FJGP			100P6Q-A	
M30833FJFP			100P6S-A	



**Figure 1.2 Product Numbering System**

### 1.5 Pin Assignments

Figures 1.3 to 1.5 show pin assignments (top view).

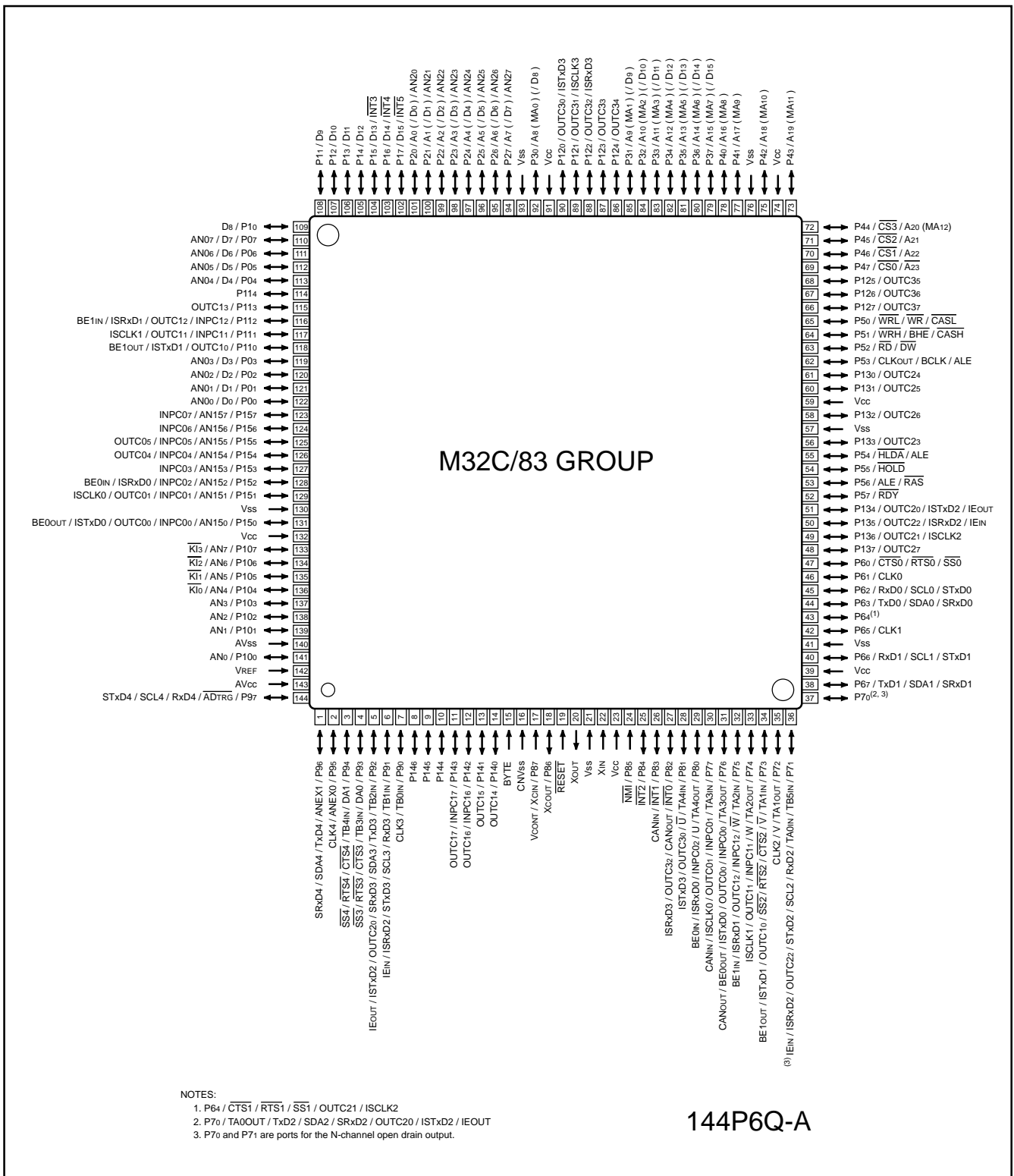


Figure 1.3 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
1		P96			TxD4/SDA4/SRx4D4		ANEX1	
2		P95			CLK4		ANEX0	
3		P94		TB4IN	CTS4/RTS4/SS4		DA1	
4		P93		TB3IN	CTS3/RTS3/SS3		DA0	
5		P92		TB2IN	TxD3/SDA3/SRx4D3	OUTC20/IEOUT/ISTxD2		
6		P91		TB1IN	RxD3/SCL3/STxD3	IEIN/ISRxD2		
7		P90		TB0IN	CLK3			
8		P146						
9		P145						
10		P144						
11		P143				INPC17/OUTC17		
12		P142				INPC16/OUTC16		
13		P141				OUTC15		
14		P140				OUTC14		
15	BYTE							
16	CNVSS							
17	X <sub>CIN</sub> /V <sub>CONT</sub>	P87						
18	X <sub>COUT</sub>	P86						
19	RESET							
20	X <sub>OUT</sub>							
21	V <sub>SS</sub>							
22	X <sub>IN</sub>							
23	V <sub>CC</sub>							
24		P85	NMI					
25		P84	INT2					
26		P83	INT1		CAN <sub>IN</sub>			
27		P82	INT0		CAN <sub>OUT</sub>	OUTC32/ISRxD3		
28		P81		TA4 <sub>IN</sub> /U		OUTC30/ISTxD3		
29		P80		TA4 <sub>OUT</sub> /U		INPC02/ISRxD0/BE0 <sub>IN</sub>		
30		P77		TA3 <sub>IN</sub>	CAN <sub>IN</sub>	INPC01/OUTC01/ISCLK0		
31		P76		TA3 <sub>OUT</sub>	CAN <sub>OUT</sub>	INPC00/OUTC00/ISTxD0/BE0 <sub>OUT</sub>		
32		P75		TA2 <sub>IN</sub> /W		INPC12/OUTC12/ISRxD1/BE1 <sub>IN</sub>		
33		P74		TA2 <sub>OUT</sub> /W		INPC11/OUTC11/ISCLK1		
34		P73		TA1 <sub>IN</sub> /V	CTS2/RTS2/SS2	OUTC10/ISTxD1/BE1 <sub>OUT</sub>		
35		P72		TA1 <sub>OUT</sub> /V	CLK2			
36		P71		TB5 <sub>IN</sub> /TA0 <sub>IN</sub>	RxD2/SCL2/STxD2	OUTC22/ISRxD2/IE <sub>IN</sub>		
37		P70		TA0 <sub>OUT</sub>	TxD2/SDA2/SRx4D2	OUTC20/ISTxD2/IE <sub>OUT</sub>		
38		P67			TxD1/SDA1/SRx4D1			
39	V <sub>CC</sub>							
40		P66			RxD1/SCL1/STxD1			
41	V <sub>SS</sub>							
42		P65			CLK1			
43		P64			CTS1/RTS1/SS1	OUTC21/ISCLK2		
44		P63			TxD0/SDA0/SRx4D0			
45		P62			RxD0/SCL0/STxD0			
46		P61			CLK0			
47		P60			CTS0/RTS0/SS0			
48		P137				OUTC27		

**Table 1.4 Pin Characteristics for 144-Pin Package (Continued)**

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
49		P136				OUTC21/ISCLK2		
50		P135				OUTC22/ISRxD2/IEIN		
51		P134				OUTC20/ISTxD2/IEOUT		
52		P57						RDY
53		P56						ALE/RAS
54		P55						HOLD
55		P54						HLDA/ALE
56		P133				OUTC23		
57	Vss							
58		P132				OUTC26		
59	Vcc							
60		P131				OUTC25		
61		P130				OUTC24		
62		P53						CLKOUT/BCLK/ALE
63		P52						RD/DW
64		P51						WRH/BHE/CASH
65		P50						WRL/WR/CASL
66		P127				OUTC37		
67		P126				OUTC36		
68		P125				OUTC35		
69		P47						CS0/A23
70		P46						CS1/A22
71		P45						CS2/A21
72		P44						CS3/A20(MA12)
73		P43						A19(MA11)
74	Vcc							
75		P42						A18(MA10)
76	Vss							
77		P41						A17(MA9)
78		P40						A16(MA8)
79		P37						A15(MA7)/(D15)
80		P36						A14(MA6)/(D14)
81		P35						A13(MA5)/(D13)
82		P34						A12(MA4)/(D12)
83		P33						A11(MA3)/(D11)
84		P32						A10(MA2)/(D10)
85		P31						A9(MA1)/(D9)
86		P124				OUTC34		
87		P123				OUTC33		
88		P122				OUTC32/ISRxD3		
89		P121				OUTC31/ISCLK3		
90		P120				OUTC30/ISTxD3		
91	Vcc							
92		P30						A8(MA0)/(D8)
93	Vss							
94		P27					AN27	A7/(D7)
95		P26					AN26	A6/(D6)
96		P25					AN25	A5/(D5)



Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
97		P24					AN24	A4(/D4)
98		P23					AN23	A3(/D3)
99		P22					AN22	A2(/D2)
100		P21					AN21	A1(/D1)
101		P20					AN20	A0(/D0)
102		P17	$\overline{\text{INT5}}$					D15
103		P16	$\overline{\text{INT4}}$					D14
104		P15	$\overline{\text{INT3}}$					D13
105		P14						D12
106		P13						D11
107		P12						D10
108		P11						D9
109		P10						D8
110		P07					AN07	D7
111		P06					AN06	D6
112		P05					AN05	D5
113		P04					AN04	D4
114		P114						
115		P113				OUTC13		
116		P112				INPC12/OUTC12/ISRxD1/BE1IN		
117		P111				INPC11/OUTC11/ISCLK1		
118		P110				OUTC10/ISTxD1/BE1OUT		
119		P03					AN03	D3
120		P02					AN02	D2
121		P01					AN01	D1
122		P00					AN00	D0
123		P157				INPC07	AN157	
124		P156				INPC06	AN156	
125		P155				INPC05/OUTC05	AN155	
126		P154				INPC04/OUTC04	AN154	
127		P153				INPC03	AN153	
128		P152				INPC02/ISRxD0/BE0IN	AN152	
129		P151				INPC01/OUTC01/ISCLK0	AN151	
130	Vss							
131		P150				INPC00/OUTC00/ISTxD0/BE0OUT	AN150	
132	Vcc							
133		P107	$\overline{\text{KI3}}$				AN7	
134		P106	$\overline{\text{KI2}}$				AN6	
135		P105	$\overline{\text{KI1}}$				AN5	
136		P104	$\overline{\text{KI0}}$				AN4	
137		P103					AN3	
138		P102					AN2	
139		P101					AN1	
140	AVss							
141		P100					AN0	
142	VREF							
143	AVcc							
144		P97			RxD4/SCL4/STxD4		$\overline{\text{ADTRG}}$	

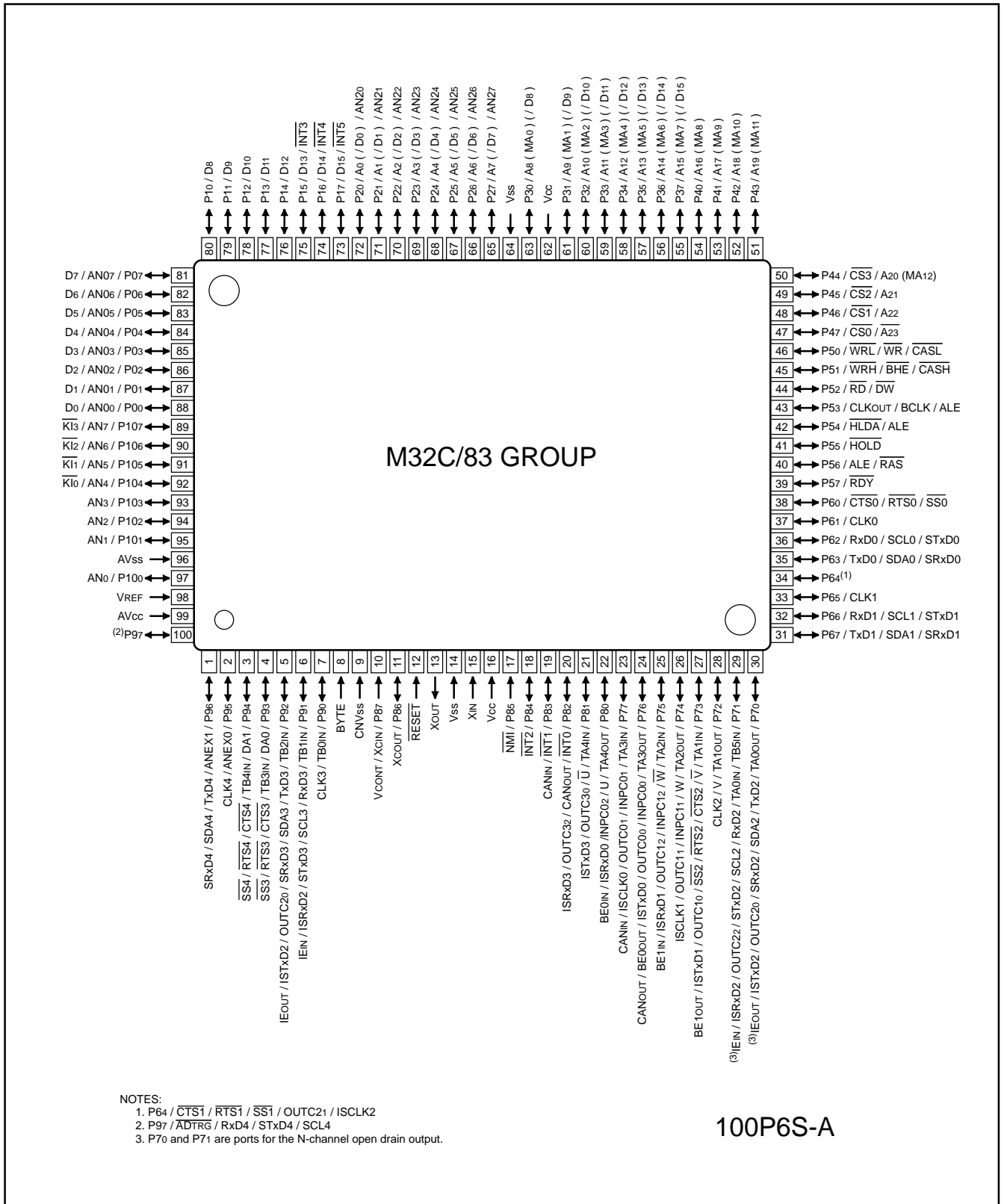


Figure 1.4 Pin assignment for 100-Pin Package

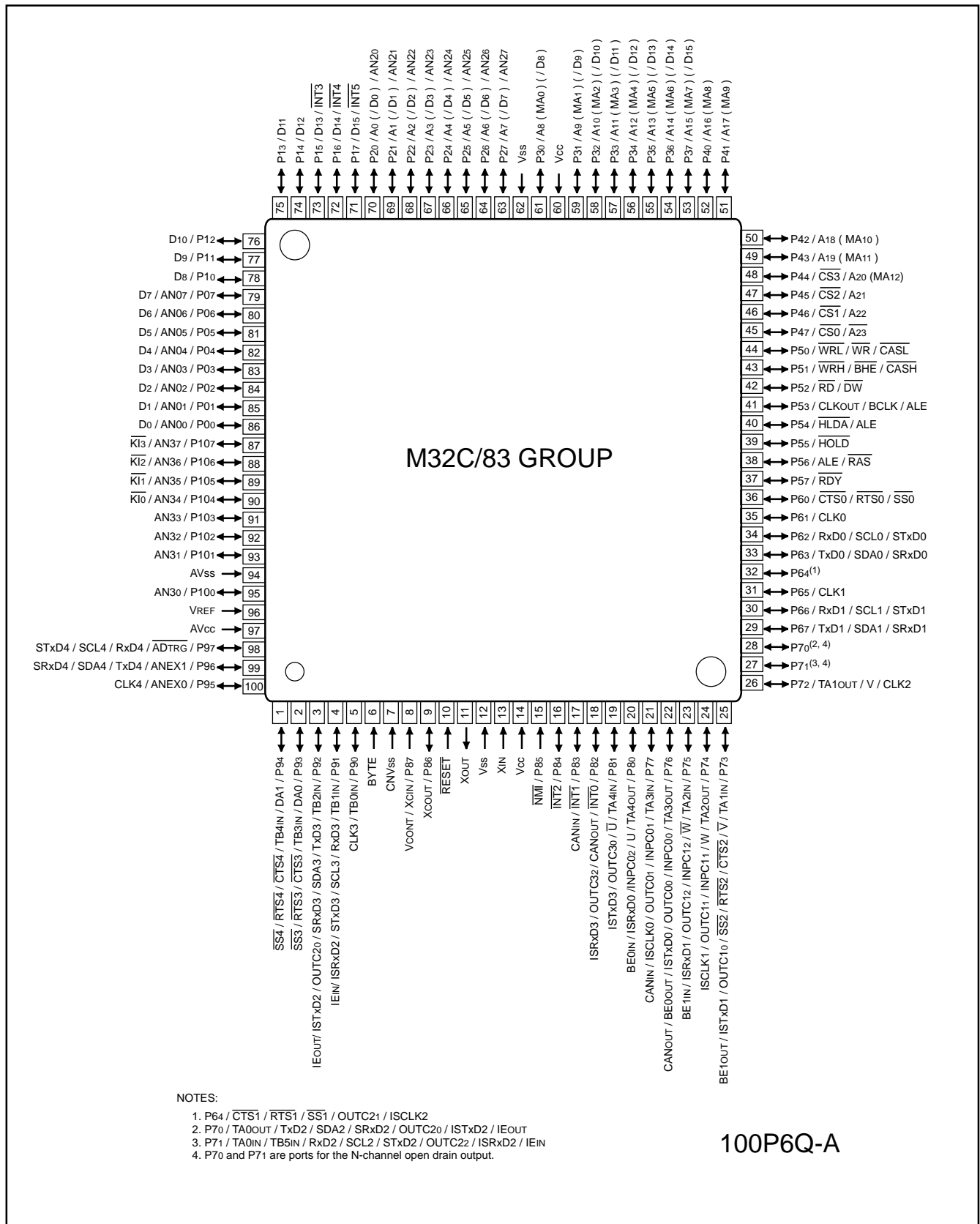


Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No		Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
FP	GP								
1	99		P96			TxD4/SDA4/SRx4D4		ANEX1	
2	100		P95			CLK4		ANEX0	
3	1		P94		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P93		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P92		TB2IN	TxD3/SDA3/SRx3D3	OUTC20/IEOUT/ISTxD2		
6	4		P91		TB1IN	RxD3/SCL3/STxD3	IEIN/ISRxD2		
7	5		P90		TB0IN	CLK3			
8	6	BYTE							
9	7	CNVss							
10	8	Xcin/Vcont	P87						
11	9	Xcout	P86						
12	10	RESET							
13	11	Xout							
14	12	Vss							
15	13	Xin							
16	14	Vcc							
17	15		P85	NMI					
18	16		P84	INT2					
19	17		P83	INT1		CANin			
20	18		P82	INT0		CANout	OUTC32/ISRxD3		
21	19		P81		TA4in/U		OUTC30/ISTxD3		
22	20		P80		TA4out/U		INPC02/ISRxD0/BE0in		
23	21		P77		TA3in	CANin	INPC01/OUTC01/ISCLK0		
24	22		P76		TA3out	CANout	INPC00/OUTC00/ISTxD0/BE0out		
25	23		P75		TA2in/W		INPC12/OUTC12/ISRxD1/BE1in		
26	24		P74		TA2out/W		INPC11/OUTC11/ISCLK1		
27	25		P73		TA1in/V	CTS2/RTS2/SS2	OUTC10/ISTxD1/BE1out		
28	26		P72		TA1out/V	CLK2			
29	27		P71		TB5in/TA0in	RxD2/SCL2/STxD2	OUTC22/ISRxD2/IEin		
30	28		P70		TA0out	TxD2/SDA2/SRx2D2	OUTC20/ISTxD2/IEout		
31	29		P67			TxD1/SDA1/SRx1D1			
32	30		P66			RxD1/SCL1/STxD1			
33	31		P65			CLK1			
34	32		P64			CTS1/RTS1/SS1	OUTC21/ISCLK2		
35	33		P63			TxD0/SDA0/SRx0D0			
36	34		P62			RxD0/SCL0/STxD0			
37	35		P61			CLK0			
38	36		P60			CTS0/RTS0/SS0			
39	37		P57						RDY
40	38		P56						ALE/RAS
41	39		P55						HOLD
42	40		P54						HLD/ALE
43	41		P53						CLKout/BCLK/ALE
44	42		P52						RD/DW
45	43		P51						WRH/BHE/CASH
46	44		P50						WRL/WR/CASL
47	45		P47						CS0/A23
48	46		P46						CS1/A22
49	47		P45						CS2/A21
50	48		P44						CS3/A20(MA12)

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package pin No		Control pin	Port	Interrupt pin	Timer pin	UART/CAN pin	Intelligent I/O pin	Analog pin	Bus control pin
FP	GP								
51	49		P4 <sub>3</sub>						A19(MA11)
52	50		P4 <sub>2</sub>						A18(MA10)
53	51		P4 <sub>1</sub>						A17(MA9)
54	52		P4 <sub>0</sub>						A16(MA8)
55	53		P3 <sub>7</sub>						A15(MA7)/(D15)
56	54		P3 <sub>6</sub>						A14(MA6)/(D14)
57	55		P3 <sub>5</sub>						A13(MA5)/(D13)
58	56		P3 <sub>4</sub>						A12(MA4)/(D12)
59	57		P3 <sub>3</sub>						A11(MA3)/(D11)
60	58		P3 <sub>2</sub>						A10(MA2)/(D10)
61	59		P3 <sub>1</sub>						A9(MA1)/(D9)
62	60	Vcc							
63	61		P3 <sub>0</sub>						A8(MA0)/(D8)
64	62	Vss							
65	63		P2 <sub>7</sub>				AN2 <sub>7</sub>		A7(/D7)
66	64		P2 <sub>6</sub>				AN2 <sub>6</sub>		A6(/D6)
67	65		P2 <sub>5</sub>				AN2 <sub>5</sub>		A5(/D5)
68	66		P2 <sub>4</sub>				AN2 <sub>4</sub>		A4(/D4)
69	67		P2 <sub>3</sub>				AN2 <sub>3</sub>		A3(/D3)
70	68		P2 <sub>2</sub>				AN2 <sub>2</sub>		A2(/D2)
71	69		P2 <sub>1</sub>				AN2 <sub>1</sub>		A1(/D1)
72	70		P2 <sub>0</sub>				AN2 <sub>0</sub>		A0(/D0)
73	71		P1 <sub>7</sub>	INT5					D15
74	72		P1 <sub>6</sub>	INT4					D14
75	73		P1 <sub>5</sub>	INT3					D13
76	74		P1 <sub>4</sub>						D12
77	75		P1 <sub>3</sub>						D11
78	76		P1 <sub>2</sub>						D10
79	77		P1 <sub>1</sub>						D9
80	78		P1 <sub>0</sub>						D8
81	79		P0 <sub>7</sub>				AN0 <sub>7</sub>		D7
82	80		P0 <sub>6</sub>				AN0 <sub>6</sub>		D6
83	81		P0 <sub>5</sub>				AN0 <sub>5</sub>		D5
84	82		P0 <sub>4</sub>				AN0 <sub>4</sub>		D4
85	83		P0 <sub>3</sub>				AN0 <sub>3</sub>		D3
86	84		P0 <sub>2</sub>				AN0 <sub>2</sub>		D2
87	85		P0 <sub>1</sub>				AN0 <sub>1</sub>		D1
88	86		P0 <sub>0</sub>				AN0 <sub>0</sub>		D0
89	87		P10 <sub>7</sub>	KI <sub>3</sub>			AN7		
90	88		P10 <sub>6</sub>	KI <sub>2</sub>			AN6		
91	89		P10 <sub>5</sub>	KI <sub>1</sub>			AN5		
92	90		P10 <sub>4</sub>	KI <sub>0</sub>			AN4		
93	91		P10 <sub>3</sub>				AN3		
94	92		P10 <sub>2</sub>				AN2		
95	93		P10 <sub>1</sub>				AN1		
96	94	AVss							
97	95		P10 <sub>0</sub>				AN0		
98	96	VREF							
99	97	AVcc							
100	98		P9 <sub>7</sub>			RxD4/SCL4/STxD4		ADTRG	

## 1.6 Pin Description

**Table 1.6 Pin Description (100-Pin and 144-Pin Packages)**

Symbol	Function	I/O type	Description
Vcc	Power supply input	I	Apply 3.0 to 5.5 V to the Vcc pins.
Vss		I	Apply 0 V to the Vss pin.
CNVss	CNVss	I	Switches processor mode. Connect this pin to Vss to start up in single-chip mode (memory expansion mode). Connect this pin to Vcc to start up in microprocessor mode.
RESET	Reset input	I	The microcomputer is in a reset state when applying "L" to the RESET pin.
XIN	Clock input	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To use an external clock, input the clock to XIN and leave XOUT open.
XOUT	Clock output	O	
BYTE	Input to switch external data bus width	I	Switches the data bus in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when the BYTE pin is held "H". Set to either. Connect this pin to Vss when an external bus is not used.
AVcc	Analog power supply input	I	Applies power supply for the A/D converter and D/A converter. Connect this pin to Vcc.
AVss	Analog power supply input	I	Applies power supply for the A/D converter and D/A converter. Connect this pin to Vss.
VREF	Reference voltage input	I	Applies reference voltage for the A/D converter.
P00 to P07	I/O port P0	I/O	8-bit I/O ports in CMOS having a direction register to select input or output. Each pin is set as an input port or output port. An input port in single-chip mode can be set for a pull-up or for no pull-up in 4-bit unit by program. When these pins are used as bus control pins in memory expansion mode and microprocessor mode, internal pull-up resistor cannot be selected. Ports used as input ports can be set for a pull-up or for no pull-up in the modes above.
D0 to D7	Data bus	I/O	Inputs and outputs data (D0 to D7) when these pins are set as the separate bus.
AN00 to AN07	Analog input pin	I	Analog input pins for the A/D converter
P10 to P17	I/O port P1	I/O	8-bit I/O ports having equivalent functions to P0
INT3 to INT5	INT interrupt input pin	I	Input pins for the INT interrupt
D8 to D15	Data bus	I/O	Inputs and outputs data (D8 to D15) when these pins are set as the separate bus.
P20 to P27	I/O port P2	I/O	8-bit I/O ports having equivalent functions to P0
A0 to A7	Address bus	O	Outputs 8 low-order address bits (A0 to A7).
A0/D0 to A7/D7	Address bus/data bus	I/O	Inputs and outputs data (D0 to D7) and outputs 8 low-order address bits (A0 to A7) by time-sharing when these pins are set as the multiplexed bus.
AN20 to AN27	Analog input pin	I	Analog input pins for A/D converter
P30 to P37	I/O port P3	I/O	8-bit I/O ports having equivalent functions to P0
A8 to A15	Address bus	O	Outputs 8 middle-order address bits (A8 to A15).
A8/D8 to A15/D15	Address bus/data bus	I/O	Inputs and outputs data (D8 to D15) and outputs 8 middle-order address bits (A8 to A15) by time-sharing when external 16-bit data bus is set as the multiplexed bus.
MA0 to MA7	Address bus	O	Outputs row addresses and column addresses by time-sharing when accessing the DRAM area.

I : Input    O : Output    I/O : Input and output

**Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)**

Symbol	Function	I/O type	Description
P40 to P47	I/O port P4	I/O	8-bit I/O ports having equivalent functions to P0
A16 to A22, A23	Address bus	O	Outputs 8 high-order address bits (A16 to A22, A23). The highest-order bit (A23) inverted is also output.
CS0 to CS3	Chip-select	O	Outputs CS0 to CS3 signals. CS0 to CS3 are chip-select signals specifying an external space.
MA8 to MA12	Address bus	O	Outputs row addresses and column addresses by time-sharing when accessing the DRAM area.
P50 to P57	I/O port P5	I/O	8-bit I/O ports having equivalent functions to P0
CLKOUT	Clock output	O	Outputs the main clock divided by 8 or divided by 32 or the clock having the same frequency as the sub clock from P53.
WRL WR WRH BHE RD BCLK HLDA HOLD ALE RDY	Bus control pin	O O O O O O O I O I	Outputs WRL, WRH, (WR, BHE), RD, BCLK, HLDA and ALE signals. WRL and WRH or BHE and WR can be switched by program. ■ WRL, WRH and RD are selected The WRL signal becomes "L" by writing data to an even address in an external memory space. The WRH signal becomes "L" by writing data to an odd address in an external memory space. The RD pin signal becomes "L" by reading data in an external memory space. ■ WR, BHE and RD are selected The WR signal becomes "L" by writing data to an external memory space. The RD signal becomes "L" by reading data in an external memory space. The BHE signal becomes "L" by accessing an odd address. Select WR, BHE and RD for an external 8-bit data bus. While the HOLD pin is held "L", the microcomputer is placed in a hold state. In a hold state, HLDA outputs a "L" signal. ALE is a signal latching the address. While the RDY pin is held "L", the microcomputer is placed in a wait state.
DW CASL CASH RAS	DRAM bus control pin	O O O O	The DW signal becomes "L" by writing data to the DRAM area. CASL and CASH are signals indicating a timing to latch column addresses. The CASL signal becomes "L" by accessing an even address. The CASH signal becomes "L" by accessing an odd address. RAS is a signal latching row addresses.
P60 to P67	I/O port P6	I/O	8-bit I/O ports having equivalent functions to P0
CTS0, CTS1 RTS0, RTS1 SS0, SS1 CLK0, CLK1 RxD0, RxD1 SCL0, SCL1 STxD0, STxD1 TxD0, TxD1 SDA0, SDA1 SRxD0, SRxD1	UART pin	I O I I/O I I/O O O I/O I	I/O pins for UART0 (P60 to P63) and UART1 (P64 to P67)
ISCLK2 OUTC21	Intelligent I/O pin	I/O O	ISCLK2 inputs and outputs the clock for the intelligent I/O communication function. OUTC21 outputs the clock for the waveform generating function.

I : Input    O : Output    I/O : Input and output

**Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)**

Symbol	Function	I/O type	Description				
P70 to P77	I/O port P7	I/O	8-bit I/O ports having equivalent functions to P0 (P70 and P71 are ports for the N-channel open drain output.)				
TA0OUT to TA3OUT TA0IN to TA3IN	Timer A pin	I/O I	I/O pins for timer A0 to A3				
TB5IN	Timer B pin	I	Input pin for timer B5				
V, $\bar{V}$	Three-phase motor control output pin	O	V-phase output pin				
W, $\bar{W}$		O	W-phase output pin				
CTS2 RTS2 SS2 CLK2 RxD2 SCL2 STxD2 TxD2 SDA2 SRxD2	UART pin	I O I I/O I I/O O O I/O I	I/O pins for UART2				
INPC00, INPC01 INPC11, INPC12 OUTC00, OUTC01 OUTC10 to OUTC12 OUTC20, OUTC22 ISCLK0, ISCLK1 ISTxD0 to ISTxD2 ISRxD1, ISRxD2 IEOUT IEIN BE0OUT BE1OUT BE1IN		Intelligent I/O pin	I O O I/O O I O O I O O I	INPC00, INPC01, INPC11 and INPC12 are input pins for the time measurement function. OUTC00, OUTC01, OUTC10 to OUTC12, OUTC20 and OUTC22 are output pins for the waveform generating function. ISCLK0 and ISCLK1 input and output the clock for the intelligent I/O communication function. ISRxD1, ISRxD2, BE1IN and IEIN input received data for the intelligent I/O communication function. ISTxD0 to ISTxD2, IEOUT, BE0OUT and BE1OUT output transmit data for the intelligent I/O communication function.			
CAN0OUT CAN0IN					CAN pin	O I	I/O pins for the CAN communication function

I : Input    O : Output    I/O : Input and output



**Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)**

Symbol	Function	I/O type	Description
P80 to P84, P86, P87	I/O port P8	I/O	I/O ports having equivalent functions to P0
XCIN XCOUT	Sub clock	I O	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT.
VCONT	Low-pass filter connect pin for PLL frequency synthesizer pin		Connects the low-pass filter to the VCONT pin when using the PLL frequency synthesizer. Connect P86 to VSS to stabilize the PLL frequency.
TA4OUT TA4IN	Timer A pin	O I	I/O pins for timer A4
U, Ū	Three-phase motor control output pin	O	U-phase output pins
INT0 to INT2	INT interrupt input pin	I	Input pins for the INT interrupt
INPC02 ISRxD0 BE0IN OUTC30 ISTxD3 OUTC32 ISRxD3	Intelligent I/O pin	I I I O O O I	INPC02 is an input pin for the time measurement function. OUTC30 and OUTC32 are output pins for the waveform generating function. ISRxD0 and BE0IN input received data for the intelligent I/O communication function. ISTxD3 outputs transmit data for the intelligent I/O communication function. ISRxD3 inputs received data for the intelligent I/O communication function.
CANOUT CANIN	CAN pin	O I	I/O pins for the CAN communication function
P85/NMI	NMI interrupt input pin	I	Input pin for the NMI interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I : Input    O : Output    I/O : Input and output

**Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)**

Symbol	Function	I/O type	Description		
P90 to P97	I/O port P9	I/O	8-bit I/O ports having equivalent functions P0. The PRCR register prevents PD9 and PS3 registers from rewriting.		
TB0IN to TB4IN	Timer B pin	I	Input pins for timers B0 to B4		
CTS3, CTS4	UART pin	I	I/O pins for UART3 (P90 to P93) and UART4 (P94 to P97)		
RTS3, RTS4		O			
SS3, SS4		I			
CLK3, CLK4		I/O			
RxD3, RxD4		I			
SCL3, SCL4		I/O			
STxD3, STxD4		O			
TxD3, TxD4		O			
SDA3, SDA4		I/O			
SRxD3, SRxD4		I			
DA0, DA1		D/A output pin		O	Output pins for the D/A converter
ANEX0,		A/D related pin		I/O	ANEX0 is an extended analog I/O pin for the A/D converter.
ANEX1,	I		ANEX1 is an extended analog input pin for the A/D converter.		
ADTRG	I		ADTRG is an A/D trigger input pin.		
OUTC20	Intelligent I/O pin	O	OUTC20 is an output pin for the waveform generating function.		
ISTxD2		O	ISTxD2 and IEOUT output transmit data for the intelligent I/O communication function.		
IEOUT		O			
IEIN		I	ISRxD2 and IEIN input received data for the intelligent I/O communication function.		
ISRxD2		I			
P100 to P107	I/O port P10	I/O	8-bit I/O ports having equivalent functions to P0		
KI0 to KI3	Key input interrupt pin	I	Input pins for the key input interrupt		
AN0 to AN7	Analog input pin	I	Analog input pins for the A/D converter		

I : Input    O : Output    I/O : Input and output

**Table 1.6 Pin Description (144-Pin Package only) (Continued)**

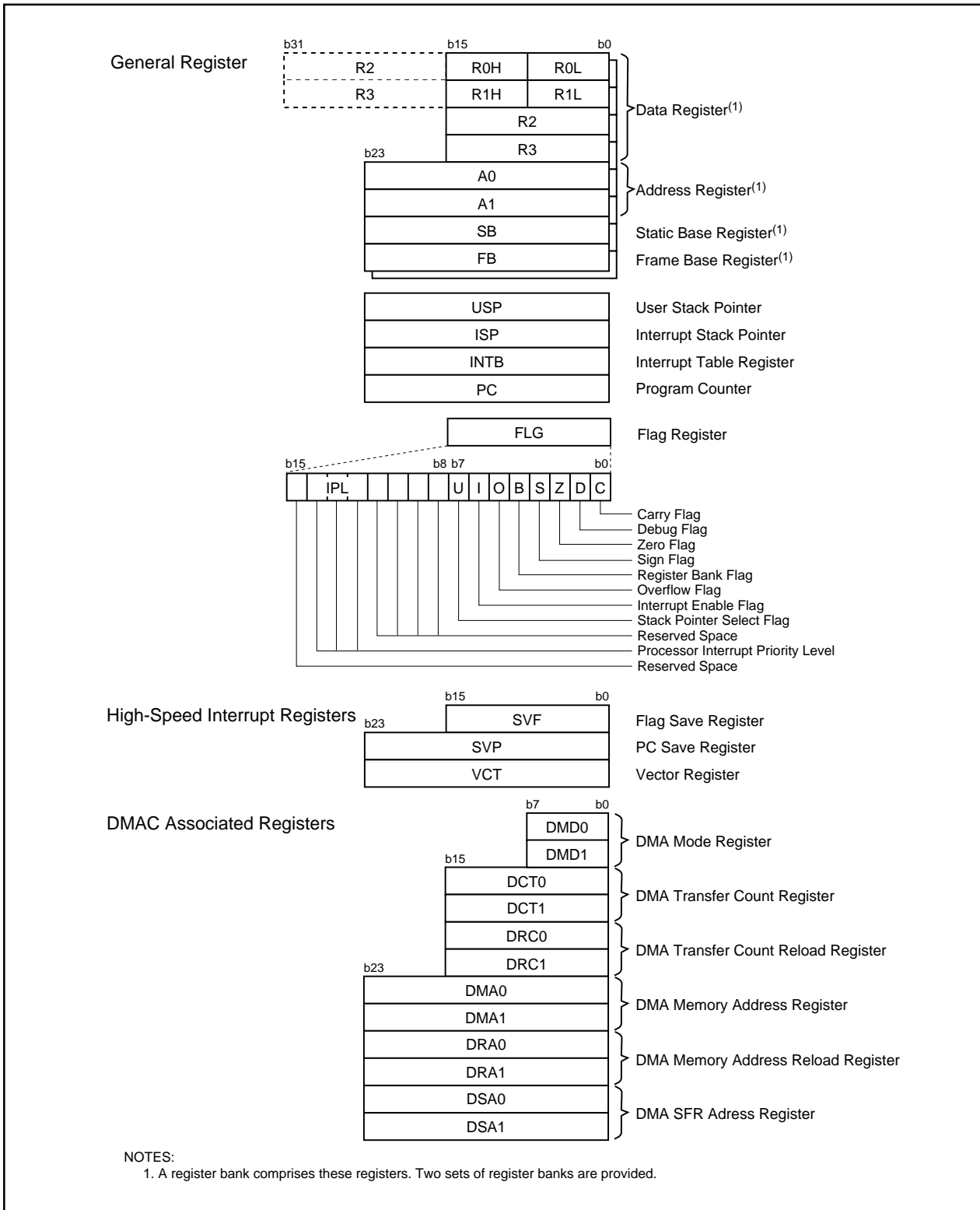
Symbol	Function	I/O type	Description
P11 <sub>0</sub> to P11 <sub>4</sub>	I/O port P11	I/O	5-bit I/O ports having equivalent functions to P0.
INPC <sub>11</sub> , INPC <sub>12</sub>	Intelligent I/O pin	I	INPC <sub>11</sub> and INPC <sub>12</sub> are input pins for the time measurement function. OUTC <sub>10</sub> to OUTC <sub>13</sub> are output pins for the waveform generating function. ISCLK <sub>1</sub> inputs and outputs the clock for the intelligent I/O communication function. ISRxD <sub>1</sub> and BE1 <sub>IN</sub> input received data for the intelligent I/O communication function. ISTxD <sub>1</sub> and BE1 <sub>OUT</sub> output transmit data for the intelligent I/O communication function.
OUTC <sub>10</sub> to OUTC <sub>13</sub>		O	
ISCLK <sub>1</sub>		I/O	
ISRxD <sub>1</sub>		I	
BE1 <sub>IN</sub>		I	
ISTxD <sub>1</sub>		O	
BE1 <sub>OUT</sub>		O	
P12 <sub>0</sub> to P12 <sub>7</sub>	I/O port P12	I/O	8-bit I/O ports having equivalent functions to P0
OUTC <sub>30</sub> to OUTC <sub>37</sub>	Intelligent I/O pin	O	OUTC <sub>30</sub> to OUTC <sub>37</sub> are output pins for the waveform generating function. ISCLK <sub>3</sub> inputs and outputs the clock for the intelligent I/O communication function. ISRxD <sub>3</sub> inputs received data for the intelligent I/O communication function. ISTxD <sub>3</sub> outputs transmit data for the intelligent I/O communication function.
ISCLK <sub>3</sub>		I/O	
ISRxD <sub>3</sub>		I	
ISTxD <sub>3</sub>		O	
P13 <sub>0</sub> to P13 <sub>7</sub>	I/O port P13	I/O	8-bit I/O ports having equivalent functions to P0
OUTC <sub>20</sub> to OUTC <sub>27</sub>	Intelligent I/O pin	O	OUTC <sub>20</sub> to OUTC <sub>27</sub> are output pins for the waveform generating function. ISCLK <sub>2</sub> inputs and outputs the clock for the intelligent I/O communication function. ISRxD <sub>2</sub> and IE <sub>IN</sub> input received data for the intelligent I/O communication function. ISTxD <sub>2</sub> and IE <sub>OUT</sub> output transmit data for the intelligent I/O communication function.
ISCLK <sub>2</sub>		I/O	
ISRxD <sub>2</sub>		I	
IE <sub>IN</sub>		I	
ISTxD <sub>2</sub>		O	
IE <sub>OUT</sub>		O	
P14 <sub>0</sub> to P14 <sub>6</sub>	I/O port P14	I/O	7-bit I/O ports having equivalent functions to P0
INPC <sub>16</sub> , INPC <sub>17</sub>	Intelligent I/O pin	I	INPC <sub>16</sub> and INPC <sub>17</sub> are input pins for the time measurement function. OUTC <sub>14</sub> to OUTC <sub>17</sub> are output pins for the waveform generating function.
OUTC <sub>14</sub> to OUTC <sub>17</sub>		O	
P15 <sub>0</sub> to P15 <sub>7</sub>	I/O port P15	I/O	8-bit I/O ports having equivalent functions to P0
INPC <sub>00</sub> to INPC <sub>07</sub>	Intelligent I/O pin	I	INPC <sub>00</sub> to INPC <sub>07</sub> are input pins for the time measurement function. OUTC <sub>00</sub> , OUTC <sub>01</sub> , OUTC <sub>04</sub> and OUTC <sub>05</sub> are output pins for the waveform generating function. ISCLK <sub>0</sub> inputs and outputs the clock for the intelligent I/O communication function. ISRxD <sub>0</sub> and BE0 <sub>IN</sub> input received data for the intelligent I/O communication function. ISTxD <sub>0</sub> and BE0 <sub>OUT</sub> output transmit data for the intelligent I/O communication function.
OUTC <sub>00</sub> , OUTC <sub>01</sub>		O	
OUTC <sub>04</sub> , OUTC <sub>05</sub>		O	
ISCLK <sub>0</sub>		I/O	
ISRxD <sub>0</sub>		I	
BE0 <sub>IN</sub>		I	
ISTxD <sub>0</sub>		O	
BE0 <sub>OUT</sub>		O	
AN15 <sub>0</sub> to AN15 <sub>7</sub>	Analog input port	I	Analog input pins for the A/D converter

I : Input    O : Output    I/O : Input and output

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

A register bank comprises 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.



**Figure 2.1 CPU Register**

## 2.1 General Register

### 2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R3R1.

### 2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

### 2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

### 2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

### 2.1.5 Program Counter (PC)

PC is 24 bits wide. It indicates an address of an instruction to be executed.

### 2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating a starting address of an interrupt vector table.

### 2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

USP and ISP as the stack pointer are 24 bits wide. The U flag can switch USP to ISP and vice versa. Refer to "2.1.8 Flag Register (FLG)" about the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

### 2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

#### 2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow occurs after an instruction is executed.

#### 2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

#### 2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic calculation; otherwise "0".

#### 2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic calculation; otherwise "0".

### 2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

### 2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when a result of an arithmetic operation overflows; otherwise "0".

### 2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0" and is enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

### 2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".

The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### 2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide. It assigns an interrupt priority levels from level 0 to level 7.

If a requested interrupt has a greater priority than IPL, the interrupt is enabled.

### 2.1.8.10 Reserved Space

When writing to the reserved space, set to "0". When read, its content is indeterminate.

## 2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows.

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

## 2.3 DMAC-associated Registers

Registers associated with DMAC are as follows.

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

### 3. Memory

Figure 3.1 shows a memory map of the M32C/83 group.

The M32C/83 provides 16-Mbyte address space from addresses 000000<sub>16</sub> to FFFFFFF<sub>16</sub>.

The internal ROM is allocated in lower addresses beginning with address FFFFFFF<sub>16</sub>. For example, a 64-Kbyte internal ROM is allocated in addresses FF0000<sub>16</sub> to FFFFFFF<sub>16</sub>.

The fixed interrupt vectors are allocated in addresses FFFFDC<sub>16</sub> to FFFFFFF<sub>16</sub>. It stores the starting address of each interrupt routine.

The internal RAM is allocated in higher addresses beginning with address 000400<sub>16</sub>. For example, a 10-Kbyte internal RAM is allocated in addresses 000400<sub>16</sub> to 002BFF<sub>16</sub>. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

The SFR is allocated in addresses 000000<sub>16</sub> to 0003FF<sub>16</sub>. The control registers for peripheral functions such as I/O port, A/D conversion, serial I/O, timer are allocated here. All addresses, which have nothing allocated within the SFR, are reserved space and cannot be accessed by users.

The special page vectors are allocated in addresses FFFE00<sub>16</sub> to FFFFDB<sub>16</sub>. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **Software Manual** for details.

In memory expansion mode and microprocessor mode, some space are reserved and cannot be accessed by users.

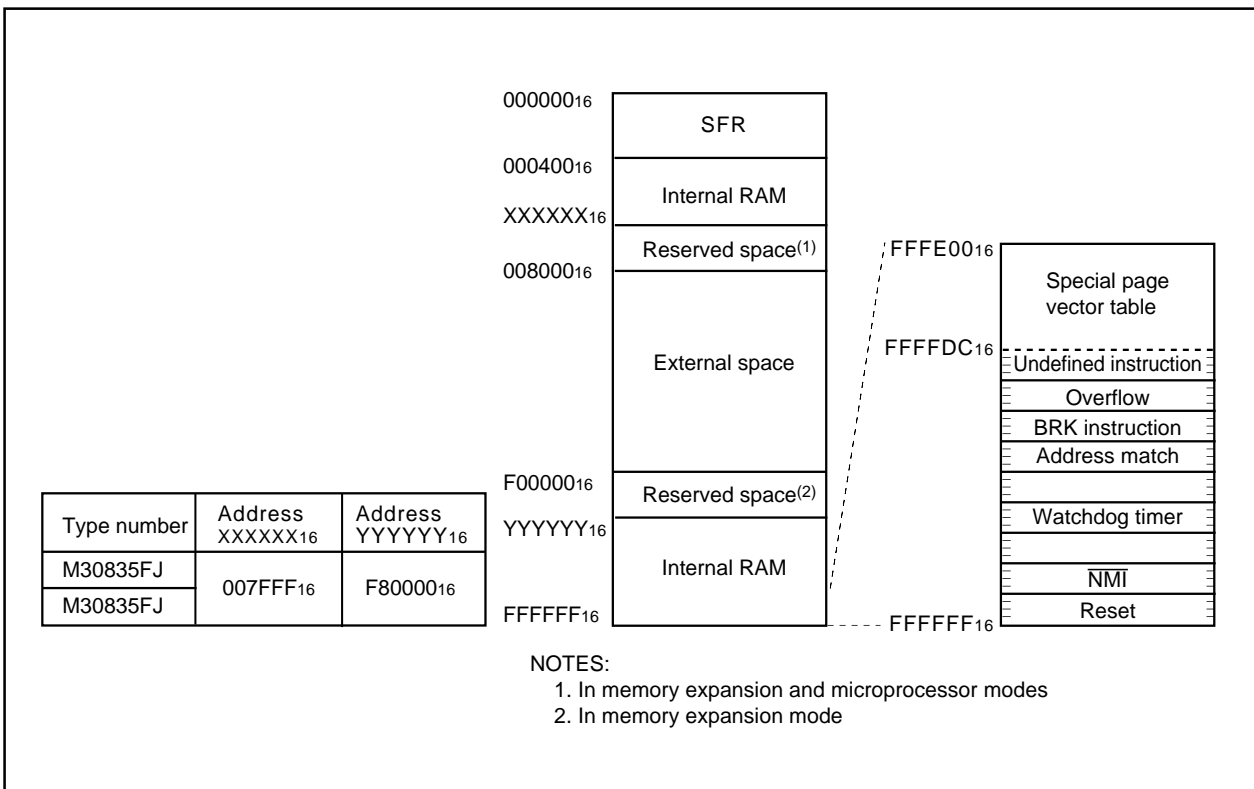


Figure 3.1 Memory Map

## 4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
0000 <sub>16</sub>			
0001 <sub>16</sub>			
0002 <sub>16</sub>			
0003 <sub>16</sub>			
0004 <sub>16</sub>	Processor mode register 0	PM0	1000 0000 <sub>2</sub> (CNVss pin ="L") 0000 0011 <sub>2</sub> (CNVss pin ="H")
0005 <sub>16</sub>	Processor mode register 1	PM1	0X00 0000 <sub>2</sub>
0006 <sub>16</sub>	System clock control register 0	CM0	0000 X000 <sub>2</sub>
0007 <sub>16</sub>	System clock control register 1	CM1	0010 0000 <sub>2</sub>
0008 <sub>16</sub>	Wait control register	WCR	1111 1111 <sub>2</sub>
0009 <sub>16</sub>	Address match interrupt enable register	AIER	XXXX 0000 <sub>2</sub>
000A <sub>16</sub>	Protect register	PRCR	XXXX 0000 <sub>2</sub>
000B <sub>16</sub>	External data bus width control register	DS	XXXX 1000 <sub>2</sub> (BYTE pin ="L") XXXX 0000 <sub>2</sub> (BYTE pin ="H")
000C <sub>16</sub>	Main clock division register	MCD	XXX0 1000 <sub>2</sub>
000D <sub>16</sub>	Oscillation stop detect register	CM2	00 <sub>16</sub>
000E <sub>16</sub>	Watchdog timer start register	WDTS	XX <sub>16</sub>
000F <sub>16</sub>	Watchdog timer control register	WDC	000X XXXX <sub>2</sub>
0010 <sub>16</sub>			
0011 <sub>16</sub>	Address match interrupt register 0	RMAD0	000000 <sub>16</sub>
0012 <sub>16</sub>			
0013 <sub>16</sub>			
0014 <sub>16</sub>			
0015 <sub>16</sub>	Address match interrupt register 1	RMAD1	000000 <sub>16</sub>
0016 <sub>16</sub>			
0017 <sub>16</sub>	VDC control register for PLL	PLV	XXXX XX01 <sub>2</sub>
0018 <sub>16</sub>			
0019 <sub>16</sub>	Address match interrupt register 2	RMAD2	000000 <sub>16</sub>
001A <sub>16</sub>			
001B <sub>16</sub>	VDC control register 0	VDC0	00 <sub>16</sub>
001C <sub>16</sub>			
001D <sub>16</sub>	Address match interrupt register 3	RMAD3	000000 <sub>16</sub>
001E <sub>16</sub>			
001F <sub>16</sub>			
0020 <sub>16</sub>			
0021 <sub>16</sub>			
0022 <sub>16</sub>			
0023 <sub>16</sub>			
0024 <sub>16</sub>			
0025 <sub>16</sub>			
0026 <sub>16</sub>			
0027 <sub>16</sub>			
0028 <sub>16</sub>			
0029 <sub>16</sub>			
002A <sub>16</sub>			
002B <sub>16</sub>			
002C <sub>16</sub>			
002D <sub>16</sub>			
002E <sub>16</sub>			
002F <sub>16</sub>			

X: Indeterminate

Blank spaces are reserved. No access is allowed.



Address	Register	Symbol	Value after RESET
0030 <sub>16</sub>			
0031 <sub>16</sub>			
0032 <sub>16</sub>			
0033 <sub>16</sub>			
0034 <sub>16</sub>			
0035 <sub>16</sub>			
0036 <sub>16</sub>			
0037 <sub>16</sub>			
0038 <sub>16</sub>			
0039 <sub>16</sub>			
003A <sub>16</sub>			
003B <sub>16</sub>			
003C <sub>16</sub>			
003D <sub>16</sub>			
003E <sub>16</sub>			
003F <sub>16</sub>			
0040 <sub>16</sub>	DRAM control register	DRAMCONT	XX <sub>16</sub>
0041 <sub>16</sub>	DRAM refresh interval set register	REFCNT	XX <sub>16</sub>
0042 <sub>16</sub>			
0043 <sub>16</sub>			
0044 <sub>16</sub>			
0045 <sub>16</sub>			
0046 <sub>16</sub>			
0047 <sub>16</sub>			
0048 <sub>16</sub>			
0049 <sub>16</sub>			
004A <sub>16</sub>			
004B <sub>16</sub>			
004C <sub>16</sub>			
004D <sub>16</sub>			
004E <sub>16</sub>			
004F <sub>16</sub>			
0050 <sub>16</sub>			
0051 <sub>16</sub>			
0052 <sub>16</sub>			
0053 <sub>16</sub>			
0054 <sub>16</sub>			
0055 <sub>16</sub>			
0056 <sub>16</sub>			
0057 <sub>16</sub>	Flash memory control register 0	FMR0	XX00 0001 <sub>2</sub>
0058 <sub>16</sub>			
0059 <sub>16</sub>			
005A <sub>16</sub>			
005B <sub>16</sub>			
005C <sub>16</sub>			
005D <sub>16</sub>			
005E <sub>16</sub>			
005F <sub>16</sub>			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0060 <sub>16</sub>			
0061 <sub>16</sub>			
0062 <sub>16</sub>			
0063 <sub>16</sub>			
0064 <sub>16</sub>			
0065 <sub>16</sub>			
0066 <sub>16</sub>			
0067 <sub>16</sub>			
0068 <sub>16</sub>	DMA0 interrupt control register	DM0IC	XXXX X000 <sub>2</sub>
0069 <sub>16</sub>	Timer B5 interrupt control register	TB5IC	XXXX X000 <sub>2</sub>
006A <sub>16</sub>	DMA2 interrupt control register	DM2IC	XXXX X000 <sub>2</sub>
006B <sub>16</sub>	UART2 receive /ACK interrupt control register	S2RIC	XXXX X000 <sub>2</sub>
006C <sub>16</sub>	Timer A0 interrupt control register	TA0IC	XXXX X000 <sub>2</sub>
006D <sub>16</sub>	UART3 receive /ACK interrupt control register	S3RIC	XXXX X000 <sub>2</sub>
006E <sub>16</sub>	Timer A2 interrupt control register	TA2IC	XXXX X000 <sub>2</sub>
006F <sub>16</sub>	UART4 receive /ACK interrupt control register	S4RIC	XXXX X000 <sub>2</sub>
0070 <sub>16</sub>	Timer A4 interrupt control register	TA4IC	XXXX X000 <sub>2</sub>
0071 <sub>16</sub>	UART0/UART3 bus conflict detect interrupt control register	BCN0IC/BCN3IC	XXXX X000 <sub>2</sub>
0072 <sub>16</sub>	UART0 receive/ACK interrupt control register	S0RIC	XXXX X000 <sub>2</sub>
0073 <sub>16</sub>	A/D0 conversion interrupt control register	AD0IC	XXXX X000 <sub>2</sub>
0074 <sub>16</sub>	UART1 receive/ACK interrupt control register	S1RIC	XXXX X000 <sub>2</sub>
0075 <sub>16</sub>	Intelligent I/O interrupt control register 0	IIO0IC	XXXX X000 <sub>2</sub>
0076 <sub>16</sub>	Timer B1 interrupt control register	TB1IC	XXXX X000 <sub>2</sub>
0077 <sub>16</sub>	Intelligent I/O interrupt control register 2	IIO2IC	XXXX X000 <sub>2</sub>
0078 <sub>16</sub>	Timer B3 interrupt control register	TB3IC	XXXX X000 <sub>2</sub>
0079 <sub>16</sub>	Intelligent I/O interrupt control register 4	IIO4IC	XXXX X000 <sub>2</sub>
007A <sub>16</sub>	INT5 interrupt control register	INT5IC	XX00 X000 <sub>2</sub>
007B <sub>16</sub>	Intelligent I/O interrupt control register 6	IIO6IC	XXXX X000 <sub>2</sub>
007C <sub>16</sub>	INT3 interrupt control register	INT3IC	XX00 X000 <sub>2</sub>
007D <sub>16</sub>	Intelligent I/O interrupt control register 8	IIO8IC	XXXX X000 <sub>2</sub>
007E <sub>16</sub>	INT1 interrupt control register	INT1IC	XX00 X000 <sub>2</sub>
007F <sub>16</sub>	Intelligent I/O interrupt control register 10/ CAN interrupt 1 control register	IIO10IC CAN1IC	XXXX X000 <sub>2</sub>
0080 <sub>16</sub>			
0081 <sub>16</sub>	Intelligent I/O interrupt control register 11/ CAN interrupt 2 control register	IIO11IC CAN2IC	XXXX X000 <sub>2</sub>
0082 <sub>16</sub>			
0083 <sub>16</sub>			
0084 <sub>16</sub>			
0085 <sub>16</sub>			
0086 <sub>16</sub>	A-D1 conversion interrupt control register	AD1IC	XXXX X000 <sub>2</sub>
0087 <sub>16</sub>			
0088 <sub>16</sub>	DMA1 interrupt control register	DM1IC	XXXX X000 <sub>2</sub>
0089 <sub>16</sub>	UART2 transmit /NACK interrupt control register	S2TIC	XXXX X000 <sub>2</sub>
008A <sub>16</sub>	DMA3 interrupt control register	DM3IC	XXXX X000 <sub>2</sub>
008B <sub>16</sub>	UART3 transmit /NACK interrupt control register	S3TIC	XXXX X000 <sub>2</sub>
008C <sub>16</sub>	Timer A1 interrupt control register	TA1IC	XXXX X000 <sub>2</sub>
008D <sub>16</sub>	UART4 transmit /NACK interrupt control register	S4TIC	XXXX X000 <sub>2</sub>
008E <sub>16</sub>	Timer A3 interrupt control register	TA3IC	XXXX X000 <sub>2</sub>
008F <sub>16</sub>	UART2 bus conflict detect interrupt control register	BCN2IC	XXXX X000 <sub>2</sub>

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Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0090 <sub>16</sub>	UART0 transmit /NACK interrupt control register	S0TIC	XXXX X000 <sub>2</sub>
0091 <sub>16</sub>	UART1/UART4 bus conflict detect interrupt control register	BCN11C/BCN41C	XXXX X000 <sub>2</sub>
0092 <sub>16</sub>	UART1 transmit/NACK interrupt control register	S1TIC	XXXX X000 <sub>2</sub>
0093 <sub>16</sub>	Key input interrupt control register	KUPIC	XXXX X000 <sub>2</sub>
0094 <sub>16</sub>	Timer B0 interrupt control register	TB01C	XXXX X000 <sub>2</sub>
0095 <sub>16</sub>	Intelligent I/O interrupt control register 1	IIO11C	XXXX X000 <sub>2</sub>
0096 <sub>16</sub>	Timer B2 interrupt control register	TB21C	XXXX X000 <sub>2</sub>
0097 <sub>16</sub>	Intelligent I/O interrupt control register 3	IIO31C	XXXX X000 <sub>2</sub>
0098 <sub>16</sub>	Timer B4 interrupt control register	TB41C	XXXX X000 <sub>2</sub>
0099 <sub>16</sub>	Intelligent I/O interrupt control register 5	IIO51C	XXXX X000 <sub>2</sub>
009A <sub>16</sub>	INT4 interrupt control register	INT41C	XX00 X000 <sub>2</sub>
009B <sub>16</sub>	Intelligent I/O interrupt control register 7	IIO71C	XXXX X000 <sub>2</sub>
009C <sub>16</sub>	INT2 interrupt control register	INT21C	XX00 X000 <sub>2</sub>
009D <sub>16</sub>	Intelligent I/O interrupt control register 9/ CAN interrupt 0 control register	IIO91C CAN01C	XXXX X000 <sub>2</sub>
009E <sub>16</sub>	INT0 interrupt control register	INT01C	XX00 X000 <sub>2</sub>
009F <sub>16</sub>	Exit priority control register	RLVL	XXXX 0000 <sub>2</sub>
00A0 <sub>16</sub>	Interrupt request register 0	IIO01R	0000 000X <sub>2</sub>
00A1 <sub>16</sub>	Interrupt request register 1	IIO11R	0000 000X <sub>2</sub>
00A2 <sub>16</sub>	Interrupt request register 2	IIO21R	0000 000X <sub>2</sub>
00A3 <sub>16</sub>	Interrupt request register 3	IIO31R	0000 000X <sub>2</sub>
00A4 <sub>16</sub>	Interrupt request register 4	IIO41R	0000 000X <sub>2</sub>
00A5 <sub>16</sub>	Interrupt request register 5	IIO51R	0000 000X <sub>2</sub>
00A6 <sub>16</sub>	Interrupt request register 6	IIO61R	0000 000X <sub>2</sub>
00A7 <sub>16</sub>	Interrupt request register 7	IIO71R	0000 000X <sub>2</sub>
00A8 <sub>16</sub>	Interrupt request register 8	IIO81R	0000 000X <sub>2</sub>
00A9 <sub>16</sub>	Interrupt request register 9	IIO91R	0000 000X <sub>2</sub>
00AA <sub>16</sub>	Interrupt request register 10	IIO101R	0000 000X <sub>2</sub>
00AB <sub>16</sub>	Interrupt request register 11	IIO111R	0000 000X <sub>2</sub>
00AC <sub>16</sub>			
00AD <sub>16</sub>			
00AE <sub>16</sub>			
00AF <sub>16</sub>			
00B0 <sub>16</sub>	Interrupt enable register 0	IIO01E	00 <sub>16</sub>
00B1 <sub>16</sub>	Interrupt enable register 1	IIO11E	00 <sub>16</sub>
00B2 <sub>16</sub>	Interrupt enable register 2	IIO21E	00 <sub>16</sub>
00B3 <sub>16</sub>	Interrupt enable register 3	IIO31E	00 <sub>16</sub>
00B4 <sub>16</sub>	Interrupt enable register 4	IIO41E	00 <sub>16</sub>
00B5 <sub>16</sub>	Interrupt enable register 5	IIO51E	00 <sub>16</sub>
00B6 <sub>16</sub>	Interrupt enable register 6	IIO61E	00 <sub>16</sub>
00B7 <sub>16</sub>	Interrupt enable register 7	IIO71E	00 <sub>16</sub>
00B8 <sub>16</sub>	Interrupt enable register 8	IIO81E	00 <sub>16</sub>
00B9 <sub>16</sub>	Interrupt enable register 9	IIO91E	00 <sub>16</sub>
00BA <sub>16</sub>	Interrupt enable register 10	IIO101E	00 <sub>16</sub>
00BB <sub>16</sub>	Interrupt enable register 11	IIO111E	00 <sub>16</sub>
00BC <sub>16</sub>			
00BD <sub>16</sub>			
00BE <sub>16</sub>			
00BF <sub>16</sub>			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0 <sub>16</sub> 00C1 <sub>16</sub>	Group 0 time measurement/waveform generating register 0	G0TM0/G0PO0	XX <sub>16</sub> XX <sub>16</sub>
00C2 <sub>16</sub> 00C3 <sub>16</sub>	Group 0 time measurement/waveform generating register 1	G0TM1/G0PO1	XX <sub>16</sub> XX <sub>16</sub>
00C4 <sub>16</sub> 00C5 <sub>16</sub>	Group 0 time measurement/waveform generating register 2	G0TM2/G0PO2	XX <sub>16</sub> XX <sub>16</sub>
00C6 <sub>16</sub> 00C7 <sub>16</sub>	Group 0 time measurement/waveform generating register 3	G0TM3/G0PO3	XX <sub>16</sub> XX <sub>16</sub>
00C8 <sub>16</sub> 00C9 <sub>16</sub>	Group 0 time measurement/waveform generating register 4	G0TM4/G0PO4	XX <sub>16</sub> XX <sub>16</sub>
00CA <sub>16</sub> 00CB <sub>16</sub>	Group 0 time measurement/waveform generating register 5	G0TM5/G0PO5	XX <sub>16</sub> XX <sub>16</sub>
00CC <sub>16</sub> 00CD <sub>16</sub>	Group 0 time measurement/waveform generating register 6	G0TM6/G0PO6	XX <sub>16</sub> XX <sub>16</sub>
00CE <sub>16</sub> 00CF <sub>16</sub>	Group 0 time measurement/waveform generating register 7	G0TM7/G0PO7	XX <sub>16</sub> XX <sub>16</sub>
00D0 <sub>16</sub>	Group 0 waveform generating control register 0	G0POCR0	0X00 X000 <sub>2</sub>
00D1 <sub>16</sub>	Group 0 waveform generating control register 1	G0POCR1	0X00 X000 <sub>2</sub>
00D2 <sub>16</sub>	Group 0 waveform generating control register 2	G0POCR2	0X00 X000 <sub>2</sub>
00D3 <sub>16</sub>	Group 0 waveform generating control register 3	G0POCR3	0X00 X000 <sub>2</sub>
00D4 <sub>16</sub>	Group 0 waveform generating control register 4	G0POCR4	0X00 X000 <sub>2</sub>
00D5 <sub>16</sub>	Group 0 waveform generating control register 5	G0POCR5	0X00 X000 <sub>2</sub>
00D6 <sub>16</sub>	Group 0 waveform generating control register 6	G0POCR6	0X00 X000 <sub>2</sub>
00D7 <sub>16</sub>	Group 0 waveform generating control register 7	G0POCR7	0X00 X000 <sub>2</sub>
00D8 <sub>16</sub>	Group 0 time measurement control register 0	G0TMCR0	00 <sub>16</sub>
00D9 <sub>16</sub>	Group 0 time measurement control register 1	G0TMCR1	00 <sub>16</sub>
00DA <sub>16</sub>	Group 0 time measurement control register 2	G0TMCR2	00 <sub>16</sub>
00DB <sub>16</sub>	Group 0 time measurement control register 3	G0TMCR3	00 <sub>16</sub>
00DC <sub>16</sub>	Group 0 time measurement control register 4	G0TMCR4	00 <sub>16</sub>
00DD <sub>16</sub>	Group 0 time measurement control register 5	G0TMCR5	00 <sub>16</sub>
00DE <sub>16</sub>	Group 0 time measurement control register 6	G0TMCR6	00 <sub>16</sub>
00DF <sub>16</sub>	Group 0 time measurement control register 7	G0TMCR7	00 <sub>16</sub>
00E0 <sub>16</sub> 00E1 <sub>16</sub>	Group 0 base timer register	G0BT	XX <sub>16</sub> XX <sub>16</sub>
00E2 <sub>16</sub>	Group 0 base timer control register 0	G0BCR0	00 <sub>16</sub>
00E3 <sub>16</sub>	Group 0 base timer control register 1	G0BCR1	00 <sub>16</sub>
00E4 <sub>16</sub>	Group 0 time measurement prescaler register 6	G0TPR6	00 <sub>16</sub>
00E5 <sub>16</sub>	Group 0 time measurement prescaler register 7	G0TPR7	00 <sub>16</sub>
00E6 <sub>16</sub>	Group 0 function enable register	G0FE	00 <sub>16</sub>
00E7 <sub>16</sub>	Group 0 function select register	G0FS	00 <sub>16</sub>
00E8 <sub>16</sub> 00E9 <sub>16</sub>	Group 0 SI/O receive buffer register	G0RB	XXXX XXXX <sub>2</sub> XX00 XXXX <sub>2</sub>
00EA <sub>16</sub> 00EB <sub>16</sub>	Group 0 transmit buffer/receive data register	G0TB/G0DR	XX <sub>16</sub>
00EC <sub>16</sub>	Group 0 receive input register	G0RI	XX <sub>16</sub>
00ED <sub>16</sub>	Group 0 SI/O communication mode register	G0MR	00 <sub>16</sub>
00EE <sub>16</sub>	Group 0 transmit output register	G0TO	XX <sub>16</sub>
00EF <sub>16</sub>	Group 0 SI/O communication control register	G0CR	0000 X000 <sub>2</sub>

X: Indeterminate

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Address	Register	Symbol	Value after RESET
00F0 <sub>16</sub>	Group 0 data compare register 0	G0CMP0	XX <sub>16</sub>
00F1 <sub>16</sub>	Group 0 data compare register 1	G0CMP1	XX <sub>16</sub>
00F2 <sub>16</sub>	Group 0 data compare register 2	G0CMP2	XX <sub>16</sub>
00F3 <sub>16</sub>	Group 0 data compare register 3	G0CMP3	XX <sub>16</sub>
00F4 <sub>16</sub>	Group 0 data mask register 0	G0MSK0	XX <sub>16</sub>
00F5 <sub>16</sub>	Group 0 data mask register 1	G0MSK1	XX <sub>16</sub>
00F6 <sub>16</sub>			
00F7 <sub>16</sub>			
00F8 <sub>16</sub> 00F9 <sub>16</sub>	Group 0 receive CRC code register	G0RCRC	XX <sub>16</sub> XX <sub>16</sub>
00FA <sub>16</sub> 00FB <sub>16</sub>	Group 0 transmit CRC code register	G0TCRC	00 <sub>16</sub> 00 <sub>16</sub>
00FC <sub>16</sub>	Group 0 SI/O extended mode register	G0EMR	00 <sub>16</sub>
00FD <sub>16</sub>	Group 0 SI/O extended receive control register	G0ERC	00 <sub>16</sub>
00FE <sub>16</sub>	Group 0 SI/O special communication interrupt detect register	G0IRF	0000 00XX <sub>2</sub>
00FF <sub>16</sub>	Group 0 SI/O extended transmit control register	G0ETC	0000 0XXX <sub>2</sub>
0100 <sub>16</sub> 0101 <sub>16</sub>	Group 1 time measurement/waveform generating register 0	G1TM0/G1PO0	XX <sub>16</sub> XX <sub>16</sub>
0102 <sub>16</sub> 0103 <sub>16</sub>	Group 1 time measurement/waveform generating register 1	G1TM1/G1PO1	XX <sub>16</sub> XX <sub>16</sub>
0104 <sub>16</sub> 0105 <sub>16</sub>	Group 1 time measurement/waveform generating register 2	G1TM2/G1PO2	XX <sub>16</sub> XX <sub>16</sub>
0106 <sub>16</sub> 0107 <sub>16</sub>	Group 1 time measurement/waveform generating register 3	G1TM3/G1PO3	XX <sub>16</sub> XX <sub>16</sub>
0108 <sub>16</sub> 0109 <sub>16</sub>	Group 1 time measurement/waveform generating register 4	G1TM4/G1PO4	XX <sub>16</sub> XX <sub>16</sub>
010A <sub>16</sub> 010B <sub>16</sub>	Group 1 time measurement/waveform generating register 5	G1TM5/G1PO5	XX <sub>16</sub> XX <sub>16</sub>
010C <sub>16</sub> 010D <sub>16</sub>	Group 1 time measurement/waveform generating register 6	G1TM6/G1PO6	XX <sub>16</sub> XX <sub>16</sub>
010E <sub>16</sub> 010F <sub>16</sub>	Group 1 time measurement/waveform generating register 7	G1TM7/G1PO7	XX <sub>16</sub> XX <sub>16</sub>
0110 <sub>16</sub>	Group 1 waveform generating control register 0	G1POCR0	0X00 X000 <sub>2</sub>
0111 <sub>16</sub>	Group 1 waveform generating control register 1	G1POCR1	0X00 X000 <sub>2</sub>
0112 <sub>16</sub>	Group 1 waveform generating control register 2	G1POCR2	0X00 X000 <sub>2</sub>
0113 <sub>16</sub>	Group 1 waveform generating control register 3	G1POCR3	0X00 X000 <sub>2</sub>
0114 <sub>16</sub>	Group 1 waveform generating control register 4	G1POCR4	0X00 X000 <sub>2</sub>
0115 <sub>16</sub>	Group 1 waveform generating control register 5	G1POCR5	0X00 X000 <sub>2</sub>
0116 <sub>16</sub>	Group 1 waveform generating control register 6	G1POCR6	0X00 X000 <sub>2</sub>
0117 <sub>16</sub>	Group 1 waveform generating control register 7	G1POCR7	0X00 X000 <sub>2</sub>
0118 <sub>16</sub>	Group 1 time measurement control register 0	G1TMCR0	00 <sub>16</sub>
0119 <sub>16</sub>	Group 1 time measurement control register 1	G1TMCR1	00 <sub>16</sub>
011A <sub>16</sub>	Group 1 time measurement control register 2	G1TMCR2	00 <sub>16</sub>
011B <sub>16</sub>	Group 1 time measurement control register 3	G1TMCR3	00 <sub>16</sub>
011C <sub>16</sub>	Group 1 time measurement control register 4	G1TMCR4	00 <sub>16</sub>
011D <sub>16</sub>	Group 1 time measurement control register 5	G1TMCR5	00 <sub>16</sub>
011E <sub>16</sub>	Group 1 time measurement control register 6	G1TMCR6	00 <sub>16</sub>
011F <sub>16</sub>	Group 1 time measurement control register 7	G1TMCR7	00 <sub>16</sub>

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Address	Register	Symbol	Value after RESET
0120 <sub>16</sub>	Group 1 base timer register	G1BT	XX <sub>16</sub>
0121 <sub>16</sub>			XX <sub>16</sub>
0122 <sub>16</sub>	Group 1 base timer control register 0	G1BCR0	00 <sub>16</sub>
0123 <sub>16</sub>	Group 1 base timer control register 1	G1BCR1	00 <sub>16</sub>
0124 <sub>16</sub>	Group 1 time measurement prescaler register 6	G1TPR6	00 <sub>16</sub>
0125 <sub>16</sub>	Group 1 time measurement prescaler register 7	G1TPR7	00 <sub>16</sub>
0126 <sub>16</sub>	Group 1 function enable register	G1FE	00 <sub>16</sub>
0127 <sub>16</sub>	Group 1 function select register	G1FS	00 <sub>16</sub>
0128 <sub>16</sub>	Group 1 SI/O receive buffer register	G1RB	XXXX XXXX <sub>2</sub>
0129 <sub>16</sub>			XX00 XXXX <sub>2</sub>
012A <sub>16</sub>	Group 1 transmit buffer/receive data register	G1TB/G1DR	XX <sub>16</sub>
012B <sub>16</sub>			
012C <sub>16</sub>	Group 1 receive input register	G1RI	XX <sub>16</sub>
012D <sub>16</sub>	Group 1 SI/O communication mode register	G1MR	00 <sub>16</sub>
012E <sub>16</sub>	Group 1 transmit output register	G1TO	XX <sub>16</sub>
012F <sub>16</sub>	Group 1 SI/O communication control register	G1CR	0000 X000 <sub>2</sub>
0130 <sub>16</sub>	Group 1 data compare register 0	G1CMP0	XX <sub>16</sub>
0131 <sub>16</sub>	Group 1 data compare register 1	G1CMP1	XX <sub>16</sub>
0132 <sub>16</sub>	Group 1 data compare register 2	G1CMP2	XX <sub>16</sub>
0133 <sub>16</sub>	Group 1 data compare register 3	G1CMP3	XX <sub>16</sub>
0134 <sub>16</sub>	Group 1 data mask register 0	G1MSK0	XX <sub>16</sub>
0135 <sub>16</sub>	Group 1 data mask register 1	G1MSK1	XX <sub>16</sub>
0136 <sub>16</sub>			
0137 <sub>16</sub>			
0138 <sub>16</sub>	Group 1 receive CRC code register	G1RCRC	XX <sub>16</sub>
0139 <sub>16</sub>			XX <sub>16</sub>
013A <sub>16</sub>	Group 1 transmit CRC code register	G1TCRC	00 <sub>16</sub>
013B <sub>16</sub>			00 <sub>16</sub>
013C <sub>16</sub>	Group 1 SI/O extended mode register	G1EMR	00 <sub>16</sub>
013D <sub>16</sub>	Group 1 SI/O extended receive control register	G1ERC	00 <sub>16</sub>
013E <sub>16</sub>	Group 1 SI/O special communication interrupt detect register	G1IRF	0000 00XX <sub>2</sub>
013F <sub>16</sub>	Group 1 SI/O extended transmit control register	G1ETC	0000 0XXX <sub>2</sub>
0140 <sub>16</sub>	Group 2 waveform generating register 0	G2PO0	XX <sub>16</sub>
0141 <sub>16</sub>			XX <sub>16</sub>
0142 <sub>16</sub>	Group 2 waveform generating register 1	G2PO1	XX <sub>16</sub>
0143 <sub>16</sub>			XX <sub>16</sub>
0144 <sub>16</sub>	Group 2 waveform generating register 2	G2PO2	XX <sub>16</sub>
0145 <sub>16</sub>			XX <sub>16</sub>
0146 <sub>16</sub>	Group 2 waveform generating register 3	G2PO3	XX <sub>16</sub>
0147 <sub>16</sub>			XX <sub>16</sub>
0148 <sub>16</sub>	Group 2 waveform generating register 4	G2PO4	XX <sub>16</sub>
0149 <sub>16</sub>			XX <sub>16</sub>
014A <sub>16</sub>	Group 2 waveform generating register 5	G2PO5	XX <sub>16</sub>
014B <sub>16</sub>			XX <sub>16</sub>
014C <sub>16</sub>	Group 2 waveform generating register 6	G2PO6	XX <sub>16</sub>
014D <sub>16</sub>			XX <sub>16</sub>
014E <sub>16</sub>	Group 2 waveform generating register 7	G2PO7	XX <sub>16</sub>
014F <sub>16</sub>			XX <sub>16</sub>

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Address	Register	Symbol	Value after RESET
0150 <sub>16</sub>	Group 2 waveform generating control register 0	G2POCR0	00 <sub>16</sub>
0151 <sub>16</sub>	Group 2 waveform generating control register 1	G2POCR1	00 <sub>16</sub>
0152 <sub>16</sub>	Group 2 waveform generating control register 2	G2POCR2	00 <sub>16</sub>
0153 <sub>16</sub>	Group 2 waveform generating control register 3	G2POCR3	00 <sub>16</sub>
0154 <sub>16</sub>	Group 2 waveform generating control register 4	G2POCR4	00 <sub>16</sub>
0155 <sub>16</sub>	Group 2 waveform generating control register 5	G2POCR5	00 <sub>16</sub>
0156 <sub>16</sub>	Group 2 waveform generating control register 6	G2POCR6	00 <sub>16</sub>
0157 <sub>16</sub>	Group 2 waveform generating control register 7	G2POCR7	00 <sub>16</sub>
0158 <sub>16</sub>			
0159 <sub>16</sub>			
015A <sub>16</sub>			
015B <sub>16</sub>			
015C <sub>16</sub>			
015D <sub>16</sub>			
015E <sub>16</sub>			
015F <sub>16</sub>			
0160 <sub>16</sub> 0161 <sub>16</sub>	Group 2 base timer register	G2BT	XX <sub>16</sub> XX <sub>16</sub>
0162 <sub>16</sub>	Group 2 base timer control register 0	G2BCR0	00 <sub>16</sub>
0163 <sub>16</sub>	Group 2 base timer control register 1	G2BCR1	00 <sub>16</sub>
0164 <sub>16</sub>	Base timer start register	BTSR	XXXX 0000 <sub>2</sub>
0165 <sub>16</sub>			
0166 <sub>16</sub>	Group 2 function enable register	G2FE	00 <sub>16</sub>
0167 <sub>16</sub>	Group 2 RTP output buffer register	G2RTP	00 <sub>16</sub>
0168 <sub>16</sub>			
0169 <sub>16</sub>			
016A <sub>16</sub>	Group 2 SI/O communication mode register	G2MR	00XX X000 <sub>2</sub>
016B <sub>16</sub>	Group 2 SI/O communication control register	G2CR	0000 X000 <sub>2</sub>
016C <sub>16</sub> 016D <sub>16</sub>	Group 2 SI/O transmit buffer register	G2TB	XX <sub>16</sub> XX <sub>16</sub>
016E <sub>16</sub> 016F <sub>16</sub>	Group 2 SI/O receive buffer register	G2RB	XX <sub>16</sub> XX <sub>16</sub>
0170 <sub>16</sub> 0171 <sub>16</sub>	Group 2 IEBus address register	IEAR	XX <sub>16</sub> XX <sub>16</sub>
0172 <sub>16</sub>	Group 2 IEBus control register	IECR	00XX X000 <sub>2</sub>
0173 <sub>16</sub>	Group 2 IEBus transmit interrupt cause detect register	IETIF	XXX0 0000 <sub>2</sub>
0174 <sub>16</sub>	Group 2 IEBus receive interrupt cause detect register	IERIF	XXX0 0000 <sub>2</sub>
0175 <sub>16</sub>			
0176 <sub>16</sub>			
0177 <sub>16</sub>			
0178 <sub>16</sub>	Input function select register	IPS	00 <sub>16</sub>
0179 <sub>16</sub>			
017A <sub>16</sub>	Group 3 SI/O communication mode register	G3MR	00XX 0000 <sub>2</sub>
017B <sub>16</sub>	Group 3 SI/O communication control register	G3CR	0000 X000 <sub>2</sub>
017C <sub>16</sub> 017D <sub>16</sub>	Group 3 SI/O transmit buffer register	G3TB	XX <sub>16</sub> XX <sub>16</sub>
017E <sub>16</sub> 017F <sub>16</sub>	Group 3 SI/O receive buffer register	G3RB	XX <sub>16</sub> XX <sub>16</sub>

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0180 <sub>16</sub> 0181 <sub>16</sub>	Group 3 waveform generating register 0	G3PO0	XX <sub>16</sub> XX <sub>16</sub>
0182 <sub>16</sub> 0183 <sub>16</sub>	Group 3 waveform generating register 1	G3PO1	XX <sub>16</sub> XX <sub>16</sub>
0184 <sub>16</sub> 0185 <sub>16</sub>	Group 3 waveform generating register 2	G3PO2	XX <sub>16</sub> XX <sub>16</sub>
0186 <sub>16</sub> 0187 <sub>16</sub>	Group 3 waveform generating register 3	G3PO3	XX <sub>16</sub> XX <sub>16</sub>
0188 <sub>16</sub> 0189 <sub>16</sub>	Group 3 waveform generating register 4	G3PO4	XX <sub>16</sub> XX <sub>16</sub>
018A <sub>16</sub> 018B <sub>16</sub>	Group 3 waveform generating register 5	G3PO5	XX <sub>16</sub> XX <sub>16</sub>
018C <sub>16</sub> 018D <sub>16</sub>	Group 3 waveform generating register 6	G3PO6	XX <sub>16</sub> XX <sub>16</sub>
018E <sub>16</sub> 018F <sub>16</sub>	Group 3 waveform generating register 7	G3PO7	XX <sub>16</sub> XX <sub>16</sub>
0190 <sub>16</sub>	Group 3 waveform generating control register 0	G3POCR0	00 <sub>16</sub>
0191 <sub>16</sub>	Group 3 waveform generating control register 1	G3POCR1	00 <sub>16</sub>
0192 <sub>16</sub>	Group 3 waveform generating control register 2	G3POCR2	00 <sub>16</sub>
0193 <sub>16</sub>	Group 3 waveform generating control register 3	G3POCR3	00 <sub>16</sub>
0194 <sub>16</sub>	Group 3 waveform generating control register 4	G3POCR4	00 <sub>16</sub>
0195 <sub>16</sub>	Group 3 waveform generating control register 5	G3POCR5	00 <sub>16</sub>
0196 <sub>16</sub>	Group 3 waveform generating control register 6	G3POCR6	00 <sub>16</sub>
0197 <sub>16</sub>	Group 3 waveform generating control register 7	G3POCR7	00 <sub>16</sub>
0198 <sub>16</sub> 0199 <sub>16</sub>	Group 3 waveform generating mask register 4	G3MK4	XX <sub>16</sub> XX <sub>16</sub>
019A <sub>16</sub> 019B <sub>16</sub>	Group 3 waveform generating mask register 5	G3MK5	XX <sub>16</sub> XX <sub>16</sub>
019C <sub>16</sub> 019D <sub>16</sub>	Group 3 waveform generating mask register 6	G3MK6	XX <sub>16</sub> XX <sub>16</sub>
019E <sub>16</sub> 019F <sub>16</sub>	Group 3 waveform generating mask register 7	G3MK7	XX <sub>16</sub> XX <sub>16</sub>
01A0 <sub>16</sub> 01A1 <sub>16</sub>	Group 3 base timer register	G3BT	XX <sub>16</sub> XX <sub>16</sub>
01A2 <sub>16</sub>	Group 3 base timer control register 0	G3BCR0	00 <sub>16</sub>
01A3 <sub>16</sub>	Group 3 base timer control register 1	G3BCR1	00 <sub>16</sub>
01A4 <sub>16</sub>			
01A5 <sub>16</sub>			
01A6 <sub>16</sub>	Group 3 function enable register	G3FE	00 <sub>16</sub>
01A7 <sub>16</sub>	Group 3 RTP output buffer register	G3RTP	00 <sub>16</sub>
01A8 <sub>16</sub>			
01A9 <sub>16</sub>			
01AA <sub>16</sub>			
01AB <sub>16</sub>			
01AC <sub>16</sub>			
01AD <sub>16</sub>	Group 3 SI/O communication flag register	G3FLG	XXXX XXX0 <sub>2</sub>
01AE <sub>16</sub>			
01AF <sub>16</sub>			

X: Indeterminate

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Address	Register	Symbol	Value after RESET
01B0 <sub>16</sub>			
01B1 <sub>16</sub>			
01B2 <sub>16</sub>			
01B3 <sub>16</sub>			
01B4 <sub>16</sub>			
01B5 <sub>16</sub>			
01B6 <sub>16</sub>			
01B7 <sub>16</sub>			
01B8 <sub>16</sub>			
01B9 <sub>16</sub>			
01BA <sub>16</sub>			
01BB <sub>16</sub>			
01BC <sub>16</sub>			
01BD <sub>16</sub>			
01BE <sub>16</sub>			
01BF <sub>16</sub>			
01C0 <sub>16</sub> 01C1 <sub>16</sub>	A/D1 register 0	AD10	XX <sub>16</sub> XX <sub>16</sub>
01C2 <sub>16</sub> 01C3 <sub>16</sub>	A/D1 register 1	AD11	XX <sub>16</sub> XX <sub>16</sub>
01C4 <sub>16</sub> 01C5 <sub>16</sub>	A/D1 register 2	AD12	XX <sub>16</sub> XX <sub>16</sub>
01C6 <sub>16</sub> 01C7 <sub>16</sub>	A/D1 register 3	AD13	XX <sub>16</sub> XX <sub>16</sub>
01C8 <sub>16</sub> 01C9 <sub>16</sub>	A/D1 register 4	AD14	XX <sub>16</sub> XX <sub>16</sub>
01CA <sub>16</sub> 01CB <sub>16</sub>	A/D1 register 5	AD15	XX <sub>16</sub> XX <sub>16</sub>
01CC <sub>16</sub> 01CD <sub>16</sub>	A/D1 register 6	AD16	XX <sub>16</sub> XX <sub>16</sub>
01CE <sub>16</sub> 01CF <sub>16</sub>	A/D1 register 7	AD17	XX <sub>16</sub> XX <sub>16</sub>
01D0 <sub>16</sub>			
01D1 <sub>16</sub>			
01D2 <sub>16</sub>			
01D3 <sub>16</sub>			
01D4 <sub>16</sub> 01D5 <sub>16</sub>	A/D1 control register 2	AD1CON2	X00X X000 <sub>2</sub>
01D6 <sub>16</sub>	A/D1 control register 0	AD1CON0	00 <sub>16</sub>
01D7 <sub>16</sub>	A/D1 control register 1	AD1CON1	XX00 0000 <sub>2</sub>
01D8 <sub>16</sub>			
01D9 <sub>16</sub>			
01DA <sub>16</sub>			
01DB <sub>16</sub>			
01DC <sub>16</sub>			
01DD <sub>16</sub>			
01DE <sub>16</sub>			
01DF <sub>16</sub>			

X: Indeterminate

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Address	Register	Symbol	Value after RESET
01E0 <sub>16</sub>	CAN0 message slot buffer 0 standard ID0	C0SLOT0_0	XX <sub>16</sub>
01E1 <sub>16</sub>	CAN0 message slot buffer 0 standard ID1	C0SLOT0_1	XX <sub>16</sub>
01E2 <sub>16</sub>	CAN0 message slot buffer 0 extended ID0	C0SLOT0_2	XX <sub>16</sub>
01E3 <sub>16</sub>	CAN0 message slot buffer 0 extended ID1	C0SLOT0_3	XX <sub>16</sub>
01E4 <sub>16</sub>	CAN0 message slot buffer 0 extended ID2	C0SLOT0_4	XX <sub>16</sub>
01E5 <sub>16</sub>	CAN0 message slot buffer 0 data length code	C0SLOT0_5	XX <sub>16</sub>
01E6 <sub>16</sub>	CAN0 message slot buffer 0 data 0	C0SLOT0_6	XX <sub>16</sub>
01E7 <sub>16</sub>	CAN0 message slot buffer 0 data 1	C0SLOT0_7	XX <sub>16</sub>
01E8 <sub>16</sub>	CAN0 message slot buffer 0 data 2	C0SLOT0_8	XX <sub>16</sub>
01E9 <sub>16</sub>	CAN0 message slot buffer 0 data 3	C0SLOT0_9	XX <sub>16</sub>
01EA <sub>16</sub>	CAN0 message slot buffer 0 data 4	C0SLOT0_10	XX <sub>16</sub>
01EB <sub>16</sub>	CAN0 message slot buffer 0 data 5	C0SLOT0_11	XX <sub>16</sub>
01EC <sub>16</sub>	CAN0 message slot buffer 0 data 6	C0SLOT0_12	XX <sub>16</sub>
01ED <sub>16</sub>	CAN0 message slot buffer 0 data 7	C0SLOT0_13	XX <sub>16</sub>
01EE <sub>16</sub>	CAN0 message slot buffer 0 time stamp high-order	C0SLOT0_14	XX <sub>16</sub>
01EF <sub>16</sub>	CAN0 message slot buffer 0 time stamp low-order	C0SLOT0_15	XX <sub>16</sub>
01F0 <sub>16</sub>	CAN0 message slot buffer 1 standard ID0	C0SLOT1_0	XX <sub>16</sub>
01F1 <sub>16</sub>	CAN0 message slot buffer 1 standard ID1	C0SLOT1_1	XX <sub>16</sub>
01F2 <sub>16</sub>	CAN0 message slot buffer 1 extended ID0	C0SLOT1_2	XX <sub>16</sub>
01F3 <sub>16</sub>	CAN0 message slot buffer 1 extended ID1	C0SLOT1_3	XX <sub>16</sub>
01F4 <sub>16</sub>	CAN0 message slot buffer 1 extended ID2	C0SLOT1_4	XX <sub>16</sub>
01F5 <sub>16</sub>	CAN0 message slot buffer 1 data length code	C0SLOT1_5	XX <sub>16</sub>
01F6 <sub>16</sub>	CAN0 message slot buffer 1 data 0	C0SLOT1_6	XX <sub>16</sub>
01F7 <sub>16</sub>	CAN0 message slot buffer 1 data 1	C0SLOT1_7	XX <sub>16</sub>
01F8 <sub>16</sub>	CAN0 message slot buffer 1 data 2	C0SLOT1_8	XX <sub>16</sub>
01F9 <sub>16</sub>	CAN0 message slot buffer 1 data 3	C0SLOT1_9	XX <sub>16</sub>
01FA <sub>16</sub>	CAN0 message slot buffer 1 data 4	C0SLOT1_10	XX <sub>16</sub>
01FB <sub>16</sub>	CAN0 message slot buffer 1 data 5	C0SLOT1_11	XX <sub>16</sub>
01FC <sub>16</sub>	CAN0 message slot buffer 1 data 6	C0SLOT1_12	XX <sub>16</sub>
01FD <sub>16</sub>	CAN0 message slot buffer 1 data 7	C0SLOT1_13	XX <sub>16</sub>
01FE <sub>16</sub>	CAN0 message slot buffer 1 time stamp high-order	C0SLOT1_14	XX <sub>16</sub>
01FF <sub>16</sub>	CAN0 message slot buffer 1 time stamp low-order	C0SLOT1_15	XX <sub>16</sub>
0200 <sub>16</sub> 0201 <sub>16</sub>	CAN0 control register 0	C0CTRL0	XX01 0X01 <sub>2</sub> <sup>(1)</sup> XXXX 0000 <sub>2</sub> <sup>(1)</sup>
0202 <sub>16</sub> 0203 <sub>16</sub>	CAN0 status register	C0STR	0000 0000 <sub>2</sub> <sup>(1)</sup> X000 0X01 <sub>2</sub> <sup>(1)</sup>
0204 <sub>16</sub> 0205 <sub>16</sub>	CAN0 extended ID register	C0IDR	00 <sub>16</sub> <sup>(1)</sup> 00 <sub>16</sub> <sup>(1)</sup>
0206 <sub>16</sub> 0207 <sub>16</sub>	CAN0 configuration register	C0CONR	0000 XXXX <sub>2</sub> <sup>(1)</sup> 0000 0000 <sub>2</sub> <sup>(1)</sup>
0208 <sub>16</sub> 0209 <sub>16</sub>	CAN0 time stamp register	C0TSR	00 <sub>16</sub> <sup>(1)</sup> 00 <sub>16</sub> <sup>(1)</sup>
020A <sub>16</sub>	CAN0 transmit error count register	C0TEC	00 <sub>16</sub> <sup>(1)</sup>
020B <sub>16</sub>	CAN0 receive error count register	C0REC	00 <sub>16</sub> <sup>(1)</sup>
020C <sub>16</sub> 020D <sub>16</sub>	CAN0 slot interrupt status register	C0SISTR	00 <sub>16</sub> <sup>(1)</sup> 00 <sub>16</sub> <sup>(1)</sup>
020E <sub>16</sub>			
020F <sub>16</sub>			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
0210 <sub>16</sub>	CAN0 slot interrupt mask register	C0SIMKR	00 <sub>16</sub> <sup>(2)</sup>
0211 <sub>16</sub>			00 <sub>16</sub> <sup>(2)</sup>
0212 <sub>16</sub>			
0213 <sub>16</sub>			
0214 <sub>16</sub>	CAN0 error interrupt mask register	C0EIMKR	XXXX X000 <sub>2</sub> <sup>(2)</sup>
0215 <sub>16</sub>	CAN0 error interrupt status register	C0EISTR	XXXX X000 <sub>2</sub> <sup>(2)</sup>
0216 <sub>16</sub>			
0217 <sub>16</sub>	CAN0 baud rate prescaler	C0BRP	0000 0001 <sub>2</sub> <sup>(2)</sup>
0218 <sub>16</sub>			
0219 <sub>16</sub>			
021A <sub>16</sub>			
021B <sub>16</sub>			
021C <sub>16</sub>			
021D <sub>16</sub>			
021E <sub>16</sub>			
021F <sub>16</sub>			
0220 <sub>16</sub>			
0221 <sub>16</sub>			
0222 <sub>16</sub>			
0223 <sub>16</sub>			
0224 <sub>16</sub>			
0225 <sub>16</sub>			
0226 <sub>16</sub>			
0227 <sub>16</sub>			
0228 <sub>16</sub>	CAN0 global mask register standard ID0	C0GMR0	XXX0 0000 <sub>2</sub> <sup>(2)</sup>
0229 <sub>16</sub>	CAN0 global mask register standard ID1	C0GMR1	XX00 0000 <sub>2</sub> <sup>(2)</sup>
022A <sub>16</sub>	CAN0 global mask register extended ID0	C0GMR2	XXXX 0000 <sub>2</sub> <sup>(2)</sup>
022B <sub>16</sub>	CAN0 global mask register extended ID1	C0GMR3	00 <sub>16</sub> <sup>(2)</sup>
022C <sub>16</sub>	CAN0 global mask register extended ID2	C0GMR4	XX00 0000 <sub>2</sub> <sup>(2)</sup>
022D <sub>16</sub>			
022E <sub>16</sub>			
022F <sub>16</sub>			
0230 <sub>16</sub>	CAN0 message slot 0 control register / CAN0 local mask register A standard ID0	C0MCTL0/ C0LMAR0	0000 0000 <sub>2</sub> <sup>(2)</sup> XXX0 0000 <sub>2</sub> <sup>(2)</sup>
0231 <sub>16</sub>	CAN0 message slot 1 control register / CAN0 local mask register A standard ID1	C0MCTL1/ C0LMAR1	0000 0000 <sub>2</sub> <sup>(2)</sup> XX00 0000 <sub>2</sub> <sup>(2)</sup>
0232 <sub>16</sub>	CAN0 message slot 2 control register / CAN0 local mask register A extended ID0	C0MCTL2/ C0LMAR2	0000 0000 <sub>2</sub> <sup>(2)</sup> XXXX 0000 <sub>2</sub> <sup>(2)</sup>
0233 <sub>16</sub>	CAN0 message slot 3 control register / CAN0 local mask register A extended ID1	C0MCTL3/ C0LMAR3	00 <sub>16</sub> <sup>(2)</sup> 00 <sub>16</sub> <sup>(2)</sup>
0234 <sub>16</sub>	CAN0 message slot 4 control register / CAN0 local mask register A extended ID2	C0MCTL4/ C0LMAR4	0000 0000 <sub>2</sub> <sup>(2)</sup> XX00 0000 <sub>2</sub> <sup>(2)</sup>
0235 <sub>16</sub>	CAN0 message slot 5 control register	C0MCTL5	00 <sub>16</sub> <sup>(2)</sup>
0236 <sub>16</sub>	CAN0 message slot 6 control register	C0MCTL6	00 <sub>16</sub> <sup>(2)</sup>
0237 <sub>16</sub>	CAN0 message slot 7 control register	C0MCTL7	00 <sub>16</sub> <sup>(2)</sup>
0238 <sub>16</sub>	CAN0 message slot 8 control register / CAN0 local mask register B standard ID0	C0MCTL8/ C0LMBR0	0000 0000 <sub>2</sub> <sup>(2)</sup> XXX0 0000 <sub>2</sub> <sup>(2)</sup>

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220<sub>16</sub> to 023F<sub>16</sub>.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
0239 <sub>16</sub>	CAN0 message slot 9 control register / CAN0 local mask register B standard ID1	C0MCTL9/ C0LMBR1	0000 0000 <sub>2</sub> <sup>(2)</sup> XX00 0000 <sub>2</sub> <sup>(2)</sup>
023A <sub>16</sub>	CAN0 message slot 10 control register / CAN0 local mask register B extended ID0	C0MCTL10/ C0LMBR2	0000 0000 <sub>2</sub> <sup>(2)</sup> XXXX 0000 <sub>2</sub> <sup>(2)</sup>
023B <sub>16</sub>	CAN0 message slot 11 control register / CAN0 local mask register B extended ID1	C0MCTL11/ C0LMBR3	00 <sub>16</sub> <sup>(2)</sup> 00 <sub>16</sub> <sup>(2)</sup>
023C <sub>16</sub>	CAN0 message slot 12 control register / CAN0 local mask register B extended ID2	C0MCTL12/ C0LMBR4	0000 0000 <sub>2</sub> <sup>(2)</sup> XX00 0000 <sub>2</sub> <sup>(2)</sup>
023D <sub>16</sub>	CAN0 message slot 13 control register	C0MCTL13	00 <sub>16</sub> <sup>(2)</sup>
023E <sub>16</sub>	CAN0 message slot 14 control register	C0MCTL14	00 <sub>16</sub> <sup>(2)</sup>
023F <sub>16</sub>	CAN0 message slot 15 control register	C0MCTL15	00 <sub>16</sub> <sup>(2)</sup>
0240 <sub>16</sub>	CAN0 slot buffer select register	C0SBS	00 <sub>16</sub> <sup>(2)</sup>
0241 <sub>16</sub>	CAN0 control register 1	C0CTRL1	XX00 00XX <sub>2</sub> <sup>(2)</sup>
0242 <sub>16</sub>	CAN0 sleep control register	C0SLPR	XXXX XXX0 <sub>2</sub>
0243 <sub>16</sub>			
0244 <sub>16</sub>	CAN0 acceptance filter support register	C0AFS	00 <sub>16</sub> <sup>(2)</sup>
0245 <sub>16</sub>			01 <sub>16</sub> <sup>(2)</sup>
0246 <sub>16</sub>			
0247 <sub>16</sub>			
0248 <sub>16</sub>			
0249 <sub>16</sub>			
024A <sub>16</sub>			
024B <sub>16</sub>			
024C <sub>16</sub>			
024D <sub>16</sub>			
024E <sub>16</sub>			
024F <sub>16</sub>			
0250 <sub>16</sub>			
0251 <sub>16</sub>			
0252 <sub>16</sub>			
0253 <sub>16</sub>			
0254 <sub>16</sub>			
0255 <sub>16</sub>			
0256 <sub>16</sub>			
0257 <sub>16</sub>			
0258 <sub>16</sub>			
0259 <sub>16</sub>			
025A <sub>16</sub>			
025B <sub>16</sub>			
025C <sub>16</sub>			
025D <sub>16</sub>			
025E <sub>16</sub>			
025F <sub>16</sub>			
0260 <sub>16</sub>			
0261 <sub>16</sub> to 02BF <sub>16</sub>			

(Note 1)

X: Indeterminate

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## NOTES:

1. The BANKSEL bit in the C0CTRL1 register switches functions for addresses 0220<sub>16</sub> to 023F<sub>16</sub>.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02C0 <sub>16</sub> 02C1 <sub>16</sub>	X0 register Y0 register	X0R,Y0R	XX <sub>16</sub> XX <sub>16</sub>
02C2 <sub>16</sub> 02C3 <sub>16</sub>	X1 register Y1 register	X1R,Y1R	XX <sub>16</sub> XX <sub>16</sub>
02C4 <sub>16</sub> 02C5 <sub>16</sub>	X2 register Y2 register	X2R,Y2R	XX <sub>16</sub> XX <sub>16</sub>
02C6 <sub>16</sub> 02C7 <sub>16</sub>	X3 register Y3 register	X3R,Y3R	XX <sub>16</sub> XX <sub>16</sub>
02C8 <sub>16</sub> 02C9 <sub>16</sub>	X4 register Y4 register	X4R,Y4R	XX <sub>16</sub> XX <sub>16</sub>
02CA <sub>16</sub> 02CB <sub>16</sub>	X5 register Y5 register	X5R,Y5R	XX <sub>16</sub> XX <sub>16</sub>
02CC <sub>16</sub> 02CD <sub>16</sub>	X6 register Y6 register	X6R,Y6R	XX <sub>16</sub> XX <sub>16</sub>
02CE <sub>16</sub> 02CF <sub>16</sub>	X7 register Y7 register	X7R,Y7R	XX <sub>16</sub> XX <sub>16</sub>
02D0 <sub>16</sub> 02D1 <sub>16</sub>	X8 register Y8 register	X8R,Y8R	XX <sub>16</sub> XX <sub>16</sub>
02D2 <sub>16</sub> 02D3 <sub>16</sub>	X9 register Y9 register	X9R,Y9R	XX <sub>16</sub> XX <sub>16</sub>
02D4 <sub>16</sub> 02D5 <sub>16</sub>	X10 register Y10 register	X10R,Y10R	XX <sub>16</sub> XX <sub>16</sub>
02D6 <sub>16</sub> 02D7 <sub>16</sub>	X11 register Y11 register	X11R,Y11R	XX <sub>16</sub> XX <sub>16</sub>
02D8 <sub>16</sub> 02D9 <sub>16</sub>	X12 register Y12 register	X12R,Y12R	XX <sub>16</sub> XX <sub>16</sub>
02DA <sub>16</sub> 02DB <sub>16</sub>	X13 register Y13 register	X13R,Y13R	XX <sub>16</sub> XX <sub>16</sub>
02DC <sub>16</sub> 02DD <sub>16</sub>	X14 register Y14 register	X14R,Y14R	XX <sub>16</sub> XX <sub>16</sub>
02DE <sub>16</sub> 02DF <sub>16</sub>	X15 register Y15 register	X15R,Y15R	XX <sub>16</sub> XX <sub>16</sub>
02E0 <sub>16</sub>	XY control register	XYC	XXXX XX00 <sub>2</sub>
02E1 <sub>16</sub>			
02E2 <sub>16</sub>			
02E3 <sub>16</sub>			
02E4 <sub>16</sub>	UART1 special mode register 4	U1SMR4	00 <sub>16</sub>
02E5 <sub>16</sub>	UART1 special mode register 3	U1SMR3	00 <sub>16</sub>
02E6 <sub>16</sub>	UART1 special mode register 2	U1SMR2	00 <sub>16</sub>
02E7 <sub>16</sub>	UART1 special mode register	U1SMR	00 <sub>16</sub>
02E8 <sub>16</sub>	UART1 transmit/receive mode register	U1MR	00 <sub>16</sub>
02E9 <sub>16</sub>	UART1 baud rate register	U1BRG	XX <sub>16</sub>
02EA <sub>16</sub> 02EB <sub>16</sub>	UART1 transmit buffer register	U1TB	XX <sub>16</sub> XX <sub>16</sub>
02EC <sub>16</sub>	UART1 transmit/receive control register 0	U1C0	0000 1000 <sub>2</sub>
02ED <sub>16</sub>	UART1 transmit/receive control register 1	U1C1	0000 0010 <sub>2</sub>
02EE <sub>16</sub> 02EF <sub>16</sub>	UART1 receive buffer register	U1RB	XX <sub>16</sub> XX <sub>16</sub>

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
02F0 <sub>16</sub>			
02F1 <sub>16</sub>			
02F2 <sub>16</sub>			
02F3 <sub>16</sub>			
02F4 <sub>16</sub>	UART4 special mode register 4	U4SMR4	00 <sub>16</sub>
02F5 <sub>16</sub>	UART4 special mode register 3	U4SMR3	00 <sub>16</sub>
02F6 <sub>16</sub>	UART4 special mode register 2	U4SMR2	00 <sub>16</sub>
02F7 <sub>16</sub>	UART4 special mode register	U4SMR	00 <sub>16</sub>
02F8 <sub>16</sub>	UART4 transmit/receive mode register	U4MR	00 <sub>16</sub>
02F9 <sub>16</sub>	UART4 baud rate register	U4BRG	XX <sub>16</sub>
02FA <sub>16</sub>	UART4 transmit buffer register	U4TB	XX <sub>16</sub>
02FB <sub>16</sub>			XX <sub>16</sub>
02FC <sub>16</sub>	UART4 transmit/receive control register 0	U4C0	0000 1000 <sub>2</sub>
02FD <sub>16</sub>	UART4 transmit/receive control register 1	U4C1	0000 0010 <sub>2</sub>
02FE <sub>16</sub>	UART4 receive buffer register	U4RB	XX <sub>16</sub>
02FF <sub>16</sub>			XX <sub>16</sub>
0300 <sub>16</sub>	Timer B3,B4,B5 count start flag	TBSR	000X XXXX <sub>2</sub>
0301 <sub>16</sub>			
0302 <sub>16</sub>	Timer A1-1 register	TA11	XX <sub>16</sub>
0303 <sub>16</sub>			XX <sub>16</sub>
0304 <sub>16</sub>	Timer A2-1 register	TA21	XX <sub>16</sub>
0305 <sub>16</sub>			XX <sub>16</sub>
0306 <sub>16</sub>	Timer A4-1 register	TA41	XX <sub>16</sub>
0307 <sub>16</sub>			XX <sub>16</sub>
0308 <sub>16</sub>	Three-phase PWM control register 0	INVC0	00 <sub>16</sub>
0309 <sub>16</sub>	Three-phase PWM control register 1	INVC1	00 <sub>16</sub>
030A <sub>16</sub>	Three-phase output buffer register 0	IDB0	XX <sub>11</sub> 1111 <sub>2</sub>
030B <sub>16</sub>	Three-phase output buffer register 1	IDB1	XX <sub>11</sub> 1111 <sub>2</sub>
030C <sub>16</sub>	Dead time timer	DTT	XX <sub>16</sub>
030D <sub>16</sub>	Timer B2 interrupt generating frequency set counter	ICTB2	XX <sub>16</sub>
030E <sub>16</sub>			
030F <sub>16</sub>			
0310 <sub>16</sub>	Timer B3 register	TB3	XX <sub>16</sub>
0311 <sub>16</sub>			XX <sub>16</sub>
0312 <sub>16</sub>	Timer B4 register	TB4	XX <sub>16</sub>
0313 <sub>16</sub>			XX <sub>16</sub>
0314 <sub>16</sub>	Timer B5 register	TB5	XX <sub>16</sub>
0315 <sub>16</sub>			XX <sub>16</sub>
0316 <sub>16</sub>			
0317 <sub>16</sub>			
0318 <sub>16</sub>			
0319 <sub>16</sub>			
031A <sub>16</sub>			
031B <sub>16</sub>	Timer B3 mode register	TB3MR	00XX 0000 <sub>2</sub>
031C <sub>16</sub>	Timer B4 mode register	TB4MR	00XX 0000 <sub>2</sub>
031D <sub>16</sub>	Timer B5 mode register	TB5MR	00XX 0000 <sub>2</sub>
031E <sub>16</sub>			
031F <sub>16</sub>	External interrupt cause select register	IFSR	00 <sub>16</sub>

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0320 <sub>16</sub>			
0321 <sub>16</sub>			
0322 <sub>16</sub>			
0323 <sub>16</sub>			
0324 <sub>16</sub>	UART3 special mode register 4	U3SMR4	00 <sub>16</sub>
0325 <sub>16</sub>	UART3 special mode register 3	U3SMR3	00 <sub>16</sub>
0326 <sub>16</sub>	UART3 special mode register 2	U3SMR2	00 <sub>16</sub>
0327 <sub>16</sub>	UART3 special mode register	U3SMR	00 <sub>16</sub>
0328 <sub>16</sub>	UART3 transmit/receive mode register	U3MR	00 <sub>16</sub>
0329 <sub>16</sub>	UART3 baud rate register	U3BRG	XX <sub>16</sub>
032A <sub>16</sub>	UART3 transmit buffer register	U3TB	XX <sub>16</sub>
032B <sub>16</sub>			XX <sub>16</sub>
032C <sub>16</sub>	UART3 transmit/receive control register 0	U3C0	0000 1000 <sub>2</sub>
032D <sub>16</sub>	UART3 transmit/receive control register 1	U3C1	0000 0010 <sub>2</sub>
032E <sub>16</sub>	UART3 receive buffer register	U3RB	XX <sub>16</sub>
032F <sub>16</sub>			XX <sub>16</sub>
0330 <sub>16</sub>			
0331 <sub>16</sub>			
0332 <sub>16</sub>			
0333 <sub>16</sub>			
0334 <sub>16</sub>	UART2 special mode register 4	U2SMR4	00 <sub>16</sub>
0335 <sub>16</sub>	UART2 special mode register 3	U2SMR3	00 <sub>16</sub>
0336 <sub>16</sub>	UART2 special mode register 2	U2SMR2	00 <sub>16</sub>
0337 <sub>16</sub>	UART2 special mode register	U2SMR	00 <sub>16</sub>
0338 <sub>16</sub>	UART2 transmit/receive mode register	U2MR	00 <sub>16</sub>
0339 <sub>16</sub>	UART2 baud rate register	U2BRG	XX <sub>16</sub>
033A <sub>16</sub>	UART2 transmit buffer register	U2TB	XX <sub>16</sub>
033B <sub>16</sub>			XX <sub>16</sub>
033C <sub>16</sub>	UART2 transmit/receive control register 0	U2C0	0000 1000 <sub>2</sub>
033D <sub>16</sub>	UART2 transmit/receive control register 1	U2C1	0000 0010 <sub>2</sub>
033E <sub>16</sub>	UART2 receive buffer register	U2RB	XX <sub>16</sub>
033F <sub>16</sub>			XX <sub>16</sub>
0340 <sub>16</sub>	Count start flag	TABSR	00 <sub>16</sub>
0341 <sub>16</sub>	Clock prescaler reset flag	CPSRF	0XXX XXXX <sub>2</sub>
0342 <sub>16</sub>	One-shot start flag	ONSF	00 <sub>16</sub>
0343 <sub>16</sub>	Trigger select register	TRGSR	00 <sub>16</sub>
0344 <sub>16</sub>	Up-down flag	UDF	00 <sub>16</sub>
0345 <sub>16</sub>			
0346 <sub>16</sub>	Timer A0 register	TA0	XX <sub>16</sub>
0347 <sub>16</sub>			XX <sub>16</sub>
0348 <sub>16</sub>	Timer A1 register	TA1	XX <sub>16</sub>
0349 <sub>16</sub>			XX <sub>16</sub>
034A <sub>16</sub>	Timer A2 register	TA2	XX <sub>16</sub>
034B <sub>16</sub>			XX <sub>16</sub>
034C <sub>16</sub>	Timer A3 register	TA3	XX <sub>16</sub>
034D <sub>16</sub>			XX <sub>16</sub>
034E <sub>16</sub>	Timer A4 register	TA4	XX <sub>16</sub>
034F <sub>16</sub>			XX <sub>16</sub>

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0350 <sub>16</sub> 0351 <sub>16</sub>	Timer B0 register	TB0	XX <sub>16</sub> XX <sub>16</sub>
0352 <sub>16</sub> 0353 <sub>16</sub>	Timer B1 register	TB1	XX <sub>16</sub> XX <sub>16</sub>
0354 <sub>16</sub> 0355 <sub>16</sub>	Timer B2 register	TB2	XX <sub>16</sub> XX <sub>16</sub>
0356 <sub>16</sub>	Timer A0 mode register	TA0MR	0000 0X00 <sub>2</sub>
0357 <sub>16</sub>	Timer A1 mode register	TA1MR	0000 0X00 <sub>2</sub>
0358 <sub>16</sub>	Timer A2 mode register	TA2MR	0000 0X00 <sub>2</sub>
0359 <sub>16</sub>	Timer A3 mode register	TA3MR	0000 0X00 <sub>2</sub>
035A <sub>16</sub>	Timer A4 mode register	TA4MR	0000 0X00 <sub>2</sub>
035B <sub>16</sub>	Timer B0 mode register	TB0MR	00XX 0000 <sub>2</sub>
035C <sub>16</sub>	Timer B1 mode register	TB1MR	00XX 0000 <sub>2</sub>
035D <sub>16</sub>	Timer B2 mode register	TB2MR	00XX 0000 <sub>2</sub>
035E <sub>16</sub>	Timer B2 special mode register	TB2SC	XXXX XXX0 <sub>2</sub>
035F <sub>16</sub>	Count source prescaler register	TCSPR	0XXX 0000 <sub>2</sub>
0360 <sub>16</sub>			
0361 <sub>16</sub>			
0362 <sub>16</sub>			
0363 <sub>16</sub>			
0364 <sub>16</sub>	UART0 special mode register 4	U0SMR4	00 <sub>16</sub>
0365 <sub>16</sub>	UART0 special mode register 3	U0SMR3	00 <sub>16</sub>
0366 <sub>16</sub>	UART0 special mode register 2	U0SMR2	00 <sub>16</sub>
0367 <sub>16</sub>	UART0 special mode register	U0SMR	00 <sub>16</sub>
0368 <sub>16</sub>	UART0 transmit/receive mode register	U0MR	00 <sub>16</sub>
0369 <sub>16</sub>	UART0 baud rate register	U0BRG	XX <sub>16</sub>
036A <sub>16</sub> 036B <sub>16</sub>	UART0 transmit buffer register	U0TB	XX <sub>16</sub> XX <sub>16</sub>
036C <sub>16</sub>	UART0 transmit/receive control register 0	U0C0	0000 1000 <sub>2</sub>
036D <sub>16</sub>	UART0 transmit/receive control register 1	U0C1	0000 0010 <sub>2</sub>
036E <sub>16</sub> 036F <sub>16</sub>	UART0 receive buffer register	U0RB	XX <sub>16</sub> XX <sub>16</sub>
0370 <sub>16</sub>			
0371 <sub>16</sub>			
0372 <sub>16</sub>			
0373 <sub>16</sub>			
0374 <sub>16</sub>			
0375 <sub>16</sub>			
0376 <sub>16</sub>	PLL control register 0	PLC0	0011 X100 <sub>2</sub>
0377 <sub>16</sub>	PLL control register 1	PLC1	XXXX 0000 <sub>2</sub>
0378 <sub>16</sub>	DMA0 cause select register	DM0SL	0X00 0000 <sub>2</sub>
0379 <sub>16</sub>	DMA1 cause select register	DM1SL	0X00 0000 <sub>2</sub>
037A <sub>16</sub>	DMA2 cause select register	DM2SL	0X00 0000 <sub>2</sub>
037B <sub>16</sub>	DMA3 cause select register	DM3SL	0X00 0000 <sub>2</sub>
037C <sub>16</sub> 037D <sub>16</sub>	CRC data register	CRCD	XX <sub>16</sub> XX <sub>16</sub>
037E <sub>16</sub> 037F <sub>16</sub>	CRC input register	CRCIN	XX <sub>16</sub>

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0380 <sub>16</sub> 0381 <sub>16</sub>	A/D0 register 0	AD00	XX <sub>16</sub> XX <sub>16</sub>
0382 <sub>16</sub> 0383 <sub>16</sub>	A/D0 register 1	AD01	XX <sub>16</sub> XX <sub>16</sub>
0384 <sub>16</sub> 0385 <sub>16</sub>	A/D0 register 2	AD02	XX <sub>16</sub> XX <sub>16</sub>
0386 <sub>16</sub> 0387 <sub>16</sub>	A/D0 register 3	AD03	XX <sub>16</sub> XX <sub>16</sub>
0388 <sub>16</sub> 0389 <sub>16</sub>	A/D0 register 4	AD04	XX <sub>16</sub> XX <sub>16</sub>
038A <sub>16</sub> 038B <sub>16</sub>	A/D0 register 5	AD05	XX <sub>16</sub> XX <sub>16</sub>
038C <sub>16</sub> 038D <sub>16</sub>	A/D0 register 6	AD06	XX <sub>16</sub> XX <sub>16</sub>
038E <sub>16</sub> 038F <sub>16</sub>	A/D0 register 7	AD07	XX <sub>16</sub> XX <sub>16</sub>
0390 <sub>16</sub>			
0391 <sub>16</sub>			
0392 <sub>16</sub>			
0393 <sub>16</sub>			
0394 <sub>16</sub> 0395 <sub>16</sub>	A/D0 control register 2	AD0CON2	X000 0000 <sub>2</sub>
0396 <sub>16</sub>	A/D0 control register 0	AD0CON0	00 <sub>16</sub>
0397 <sub>16</sub>	A/D0 control register 1	AD0CON1	00 <sub>16</sub>
0398 <sub>16</sub> 0399 <sub>16</sub>	D/A register 0	DA0	XX <sub>16</sub>
039A <sub>16</sub> 039B <sub>16</sub>	D/A register 1	DA1	XX <sub>16</sub>
039C <sub>16</sub> 039D <sub>16</sub>	D/A control register	DACON	XXXX XX00 <sub>2</sub>
039E <sub>16</sub>			
039F <sub>16</sub>			

X: Indeterminate

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&lt;144-pin package&gt;

Address	Register	Symbol	Value after RESET
03A0 <sub>16</sub>	Function select register A8	PS8	X000 0000 <sub>2</sub>
03A1 <sub>16</sub>	Function select register A9	PS9	00 <sub>16</sub>
03A2 <sub>16</sub>			
03A3 <sub>16</sub>			
03A4 <sub>16</sub>			
03A5 <sub>16</sub>			
03A6 <sub>16</sub>			
03A7 <sub>16</sub>			
03A8 <sub>16</sub>			
03A9 <sub>16</sub>			
03AA <sub>16</sub>			
03AB <sub>16</sub>			
03AC <sub>16</sub>			
03AD <sub>16</sub>			
03AE <sub>16</sub>			
03AF <sub>16</sub>	Function select register C	PSC	00X0 0000 <sub>2</sub>
03B0 <sub>16</sub>	Function select register A0	PS0	00 <sub>16</sub>
03B1 <sub>16</sub>	Function select register A1	PS1	00 <sub>16</sub>
03B2 <sub>16</sub>	Function select register B0	PSL0	00 <sub>16</sub>
03B3 <sub>16</sub>	Function select register B1	PSL1	00 <sub>16</sub>
03B4 <sub>16</sub>	Function select register A2	PS2	00X0 0000 <sub>2</sub>
03B5 <sub>16</sub>	Function select register A3	PS3	00 <sub>16</sub>
03B6 <sub>16</sub>	Function select register B2	PSL2	00X0 0000 <sub>2</sub>
03B7 <sub>16</sub>	Function select register B3	PSL3	00 <sub>16</sub>
03B8 <sub>16</sub>			
03B9 <sub>16</sub>	Function select register A5	PS5	XXX0 0000 <sub>2</sub>
03BA <sub>16</sub>			
03BB <sub>16</sub>			
03BC <sub>16</sub>	Function select register A6	PS6	00 <sub>16</sub>
03BD <sub>16</sub>	Function select register A7	PS7	00 <sub>16</sub>
03BE <sub>16</sub>			
03BF <sub>16</sub>			
03C0 <sub>16</sub>	Port P6 register	P6	XX <sub>16</sub>
03C1 <sub>16</sub>	Port P7 register	P7	XX <sub>16</sub>
03C2 <sub>16</sub>	Port P6 direction register	PD6	00 <sub>16</sub>
03C3 <sub>16</sub>	Port P7 direction register	PD7	00 <sub>16</sub>
03C4 <sub>16</sub>	Port P8 register	P8	XX <sub>16</sub>
03C5 <sub>16</sub>	Port P9 register	P9	XX <sub>16</sub>
03C6 <sub>16</sub>	Port P8 direction register	PD8	00X0 0000 <sub>2</sub>
03C7 <sub>16</sub>	Port P9 direction register	PD9	00 <sub>16</sub>
03C8 <sub>16</sub>	Port P10 register	P10	XX <sub>16</sub>
03C9 <sub>16</sub>	Port P11 register	P11	XX <sub>16</sub>
03CA <sub>16</sub>	Port P10 direction register	PD10	00 <sub>16</sub>
03CB <sub>16</sub>	Port P11 direction register	PD11	XXX0 0000 <sub>2</sub>
03CC <sub>16</sub>	Port P12 register	P12	XX <sub>16</sub>
03CD <sub>16</sub>	Port P13 register	P13	XX <sub>16</sub>
03CE <sub>16</sub>	Port P12 direction register	PD12	00 <sub>16</sub>
03CF <sub>16</sub>	Port P13 direction register	PD13	00 <sub>16</sub>

X: Indeterminate

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&lt;144-pin package&gt;

Address	Register	Symbol	Value after RESET
03D0 <sub>16</sub>	Port P14 register	P14	XX <sub>16</sub>
03D1 <sub>16</sub>	Port P15 register	P15	XX <sub>16</sub>
03D2 <sub>16</sub>	Port P14 direction register	PD14	X000 0000 <sub>2</sub>
03D3 <sub>16</sub>	Port P15 direction register	PD15	00 <sub>16</sub>
03D4 <sub>16</sub>			
03D5 <sub>16</sub>			
03D6 <sub>16</sub>			
03D7 <sub>16</sub>			
03D8 <sub>16</sub>			
03D9 <sub>16</sub>			
03DA <sub>16</sub>	Pull-up control register 2	PUR2	00 <sub>16</sub>
03DB <sub>16</sub>	Pull-up control register 3	PUR3	00 <sub>16</sub>
03DC <sub>16</sub>	Pull-up control register 4	PUR4	XXXX 0000 <sub>2</sub>
03DD <sub>16</sub>			
03DE <sub>16</sub>			
03DF <sub>16</sub>			
03E0 <sub>16</sub>	Port P0 register	P0	XX <sub>16</sub>
03E1 <sub>16</sub>	Port P1 register	P1	XX <sub>16</sub>
03E2 <sub>16</sub>	Port P0 direction register	PD0	00 <sub>16</sub>
03E3 <sub>16</sub>	Port P1 direction register	PD1	00 <sub>16</sub>
03E4 <sub>16</sub>	Port P2 register	P2	XX <sub>16</sub>
03E5 <sub>16</sub>	Port P3 register	P3	XX <sub>16</sub>
03E6 <sub>16</sub>	Port P2 direction register	PD2	00 <sub>16</sub>
03E7 <sub>16</sub>	Port P3 direction register	PD3	00 <sub>16</sub>
03E8 <sub>16</sub>	Port P4 register	P4	XX <sub>16</sub>
03E9 <sub>16</sub>	Port P5 register	P5	XX <sub>16</sub>
03EA <sub>16</sub>	Port P4 direction register	PD4	00 <sub>16</sub>
03EB <sub>16</sub>	Port P5 direction register	PD5	00 <sub>16</sub>
03EC <sub>16</sub>			
03ED <sub>16</sub>			
03EE <sub>16</sub>			
03EF <sub>16</sub>			
03F0 <sub>16</sub>	Pull-up control register 0	PUR0	00 <sub>16</sub>
03F1 <sub>16</sub>	Pull-up control register 1	PUR1	XXXX 0000 <sub>2</sub>
03F2 <sub>16</sub>			
03F3 <sub>16</sub>			
03F4 <sub>16</sub>			
03F5 <sub>16</sub>			
03F6 <sub>16</sub>			
03F7 <sub>16</sub>			
03F8 <sub>16</sub>			
03F9 <sub>16</sub>			
03FA <sub>16</sub>			
03FB <sub>16</sub>			
03FC <sub>16</sub>			
03FD <sub>16</sub>			
03FE <sub>16</sub>			
03FF <sub>16</sub>	Port control register	PCR	XXXX XXX0 <sub>2</sub>

X: Indeterminate

Blank spaces are reserved. No access is allowed.



<100-pin package>

Address	Register	Symbol	Value after RESET	
03A0 <sub>16</sub>				(Note 2)
03A1 <sub>16</sub>				
03A2 <sub>16</sub>				
03A3 <sub>16</sub>				
03A4 <sub>16</sub>				
03A5 <sub>16</sub>				
03A6 <sub>16</sub>				
03A7 <sub>16</sub>				
03A8 <sub>16</sub>				
03A9 <sub>16</sub>				
03AA <sub>16</sub>				
03AB <sub>16</sub>				
03AC <sub>16</sub>				
03AD <sub>16</sub>				
03AE <sub>16</sub>				
03AF <sub>16</sub>	Function select register C	PSC	0X00 0000 <sub>2</sub>	
03B0 <sub>16</sub>	Function select register A0	PS0	00 <sub>16</sub>	
03B1 <sub>16</sub>	Function select register A1	PS1	00 <sub>16</sub>	
03B2 <sub>16</sub>	Function select register B0	PSL0	00 <sub>16</sub>	
03B3 <sub>16</sub>	Function select register B1	PSL1	00 <sub>16</sub>	
03B4 <sub>16</sub>	Function select register A2	PS2	00X0 0000 <sub>2</sub>	
03B5 <sub>16</sub>	Function select register A3	PS3	00 <sub>16</sub>	
03B6 <sub>16</sub>	Function select register B2	PSL2	00X0 0000 <sub>2</sub>	
03B7 <sub>16</sub>	Function select register B3	PSL3	00 <sub>16</sub>	
03B8 <sub>16</sub>				
03B9 <sub>16</sub>				(Note 2)
03BA <sub>16</sub>				
03BB <sub>16</sub>				
03BC <sub>16</sub>				(Note 2)
03BD <sub>16</sub>				
03BE <sub>16</sub>				
03BF <sub>16</sub>				
03C0 <sub>16</sub>	Port P6 register	P6	XX <sub>16</sub>	
03C1 <sub>16</sub>	Port P7 register	P7	XX <sub>16</sub>	
03C2 <sub>16</sub>	Port P6 direction register	PD6	00 <sub>16</sub>	
03C3 <sub>16</sub>	Port P7 direction register	PD7	00 <sub>16</sub>	
03C4 <sub>16</sub>	Port P8 register	P8	XX <sub>16</sub>	
03C5 <sub>16</sub>	Port P9 register	P9	XX <sub>16</sub>	
03C6 <sub>16</sub>	Port P8 direction register	PD8	00X0 0000 <sub>2</sub>	
03C7 <sub>16</sub>	Port P9 direction register	PD9	00 <sub>16</sub>	
03C8 <sub>16</sub>	Port P10 register	P10	XX <sub>16</sub>	
03C9 <sub>16</sub>				(Note 2)
03CA <sub>16</sub>	Port P10 direction register	PD10	00 <sub>16</sub>	
03CB <sub>16</sub>				(Note 1)
03CC <sub>16</sub>				(Note 2)
03CD <sub>16</sub>				
03CE <sub>16</sub>				(Note 1)
03CF <sub>16</sub>				

X: Indeterminate

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NOTES:

-  Set address spaces 03CB<sub>16</sub>, 03CE<sub>16</sub> and 03CF<sub>16</sub> to "FF<sub>16</sub>" in the 100-pin package.
-  Address spaces 03A0<sub>16</sub>, 03A1<sub>16</sub>, 03B9<sub>16</sub>, 03BC<sub>16</sub>, 03BD<sub>16</sub>, 03C9<sub>16</sub>, 03CC<sub>16</sub> and 03CD<sub>16</sub> are not provided in the 100-pin package.




&lt;100-pin package&gt;

Address	Register	Symbol	Value after RESET	
03D0 <sub>16</sub>				(Note 3)
03D1 <sub>16</sub>				
03D2 <sub>16</sub>				(Note 1)
03D3 <sub>16</sub>				
03D4 <sub>16</sub>				
03D5 <sub>16</sub>				
03D6 <sub>16</sub>				
03D7 <sub>16</sub>				
03D8 <sub>16</sub>				
03D9 <sub>16</sub>				
03DA <sub>16</sub>	Pull-up control register 2	PUR2	00 <sub>16</sub>	
03DB <sub>16</sub>	Pull-up control register 3	PUR3	00 <sub>16</sub>	
03DC <sub>16</sub>				(Note 2)
03DD <sub>16</sub>				
03DE <sub>16</sub>				
03DF <sub>16</sub>				
03E0 <sub>16</sub>	Port P0 register	P0	XX <sub>16</sub>	
03E1 <sub>16</sub>	Port P1 register	P1	XX <sub>16</sub>	
03E2 <sub>16</sub>	Port P0 direction register	PD0	00 <sub>16</sub>	
03E3 <sub>16</sub>	Port P1 direction register	PD1	00 <sub>16</sub>	
03E4 <sub>16</sub>	Port P2 register	P2	XX <sub>16</sub>	
03E5 <sub>16</sub>	Port P3 register	P3	XX <sub>16</sub>	
03E6 <sub>16</sub>	Port P2 direction register	PD2	00 <sub>16</sub>	
03E7 <sub>16</sub>	Port P3 direction register	PD3	00 <sub>16</sub>	
03E8 <sub>16</sub>	Port P4 register	P4	XX <sub>16</sub>	
03E9 <sub>16</sub>	Port P5 register	P5	XX <sub>16</sub>	
03EA <sub>16</sub>	Port P4 direction register	PD4	00 <sub>16</sub>	
03EB <sub>16</sub>	Port P5 direction register	PD5	00 <sub>16</sub>	
03EC <sub>16</sub>				
03ED <sub>16</sub>				
03EE <sub>16</sub>				
03EF <sub>16</sub>				
03F0 <sub>16</sub>	Pull-up control register 0	PUR0	00 <sub>16</sub>	
03F1 <sub>16</sub>	Pull-up control register 1	PUR1	XXXX 0000 <sub>2</sub>	
03F2 <sub>16</sub>				
03F3 <sub>16</sub>				
03F4 <sub>16</sub>				
03F5 <sub>16</sub>				
03F6 <sub>16</sub>				
03F7 <sub>16</sub>				
03F8 <sub>16</sub>				
03F9 <sub>16</sub>				
03FA <sub>16</sub>				
03FB <sub>16</sub>				
03FC <sub>16</sub>				
03FD <sub>16</sub>				
03FE <sub>16</sub>				
03FF <sub>16</sub>	Port control register	PCR	XXXX XXX0 <sub>2</sub>	

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

-  Set address spaces 03D2<sub>16</sub> and 03D3<sub>16</sub> to "FF<sub>16</sub>" in the 100-pin package.
-  Set address spaces 03DC<sub>16</sub> to "00<sub>16</sub>" in the 100-pin package.
-  Address spaces 03D0<sub>16</sub> and 03D1<sub>16</sub> are not provided in the 100-pin package.

## 5. Electrical Characteristics

**Table 5.1 Absolute Maximum Ratings**

Symbol	Parameter	Condition	Value	Unit
V <sub>cc</sub>	Supply voltage	V <sub>cc</sub> =AV <sub>cc</sub>	-0.3 to 6.0	V
AV <sub>cc</sub>	Analog supply voltage	V <sub>cc</sub> =AV <sub>cc</sub>	-0.3 to 6.0	V
V <sub>i</sub>	Input voltage	RESET, CNV <sub>ss</sub> , BYTE, P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>2</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup> , V <sub>REF</sub> , X <sub>IN</sub>	-0.3 to V <sub>cc</sub> +0.3	V
		P7 <sub>0</sub> , P7 <sub>1</sub>	-0.3 to 6.0	
V <sub>o</sub>	Output voltage	P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>2</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>4</sub> , P8 <sub>6</sub> , P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup> , X <sub>OUT</sub>	-0.3 to V <sub>cc</sub> +0.3	V
		P7 <sub>0</sub> , P7 <sub>1</sub>	-0.3 to 6.0	V
P <sub>d</sub>	Power Dissipation	T <sub>opr</sub> =25° C	500	mW
T <sub>opr</sub>	Operating ambient temperature		-20 to 85/-40 to 85 <sup>(2)</sup>	° C
T <sub>stg</sub>	Storage temperature		-65 to 150	° C

**NOTES:**

1. P11 to P15 are provided in the 144-pin package.
2. This is an option that is on request basis.

**Table 5.2 Recommended Operating Conditions ( $V_{CC} = 3.0V$  to  $5.5V$  at  $T_{opr} = -20$  to  $85^{\circ}C/-40$  to  $85^{\circ}C^{(3)}$ )**

Symbol	Parameter		Standard			Unit
			Min	Typ	Max	
$V_{CC}$	Supply voltage (Through VDC)		3.0	5.0	5.5	V
	Supply voltage (Not through VDC)		3.0	3.3	3.6	V
$AV_{CC}$	Analog supply voltage			$V_{CC}$		V
$V_{SS}$	Supply voltage			0		V
$AV_{SS}$	Analog supply voltage			0		V
$V_{IH}$	Input high ("H") voltage	P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87 <sup>(4)</sup> , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(5)</sup> , $X_{IN}$ , $\overline{RESET}$ , $CNV_{SS}$ , BYTE	$0.8V_{CC}$		$V_{CC}$	V
		P70, P71	$0.8V_{CC}$		6.0	
		P00-P07, P10-P17 (In single-chip mode)	$0.8V_{CC}$		$V_{CC}$	V
		P00-P07, P10-P17 (In memory expansion mode and microprocessor mode)	$0.5V_{CC}$		$V_{CC}$	V
$V_{IL}$	Input low ("L") voltage	P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87 <sup>(4)</sup> , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(5)</sup> , $X_{IN}$ , $\overline{RESET}$ , $CNV_{SS}$ , BYTE	0		$0.2V_{CC}$	V
		P00-P07, P10-P17 (In single-chip mode)	0		$0.2V_{CC}$	V
		P00-P07, P10-P17 (In memory expansion mode and microprocessor mode)	0		$0.16V_{CC}$	V
$I_{OH(peak)}$	Peak output high ("H") current <sup>(2)</sup>	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(5)</sup>			-10.0	mA
$I_{OH(avg)}$	Average output high ("H") current <sup>(1)</sup>	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(5)</sup>			-5.0	mA
$I_{OL(peak)}$	Peak output low ("L") current <sup>(2)</sup>	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(5)</sup>			10.0	mA
$I_{OL(avg)}$	Average output low ("L") current <sup>(1)</sup>	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(5)</sup>			5.0	mA
$f(X_{IN})$	Main clock input frequency	Through VDC	$V_{CC}=4.2$ to $5.5V$	0	32	MHz
			$V_{CC}=3.0$ to $4.3V$	0	20	MHz
		Not through VDC	$V_{CC}=3.0$ to $3.6$	0	20	MHz
$f(X_{CIN})$	Sub clock oscillation frequency			32.768	50	kHz

## NOTES:

- Output current is averaged with 100ms.
- Total  $I_{OL(peak)}$  for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be less than or equal to 80mA.  
Total  $I_{OH(peak)}$  for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be less than or equal to -80mA.  
Total  $I_{OL(peak)}$  for P3, P4, P5, P6, P7, P80 to P84, P12 and P13 must be less than or equal to 80mA.  
Total  $I_{OH(peak)}$  for P3, P4, P5, P6, P72 to P77, P80 to P84, P12 and P13 must be less than or equal to -80mA.
- This is an option that is on request basis.
- $V_{IH}$  and  $V_{IL}$  reference for P87 applies to P87 used as a programmable input ports. It does not apply to P87 used as  $X_{CIN}$ .
- P11 to P15 are provided in the 144-pin package only.

V<sub>CC</sub> = 5V

**Table 5.3 Electrical Characteristics (V<sub>CC</sub>=4.2 to 5.5V, V<sub>SS</sub>=0V  
at Topr= -20 to 85°C, f(X<sub>IN</sub>)=30MHz unless otherwise specified)**

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V <sub>OH</sub>	Output high ("H") voltage	P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>2</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>4</sub> , P8 <sub>6</sub> , P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup>	I <sub>OH</sub> =-5mA	3.0			V
		P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>2</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>4</sub> , P8 <sub>6</sub> , P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup>	I <sub>OH</sub> =-200μA	4.7			
		X <sub>OUT</sub>	I <sub>OH</sub> =-1mA	3.0			V
		X <sub>COU</sub> T	No load applied		3.3		V
V <sub>OL</sub>	Output low ("L") voltage	P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>4</sub> , P8 <sub>6</sub> , P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup>	I <sub>OL</sub> =5mA			2.0	V
		P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>4</sub> , P8 <sub>6</sub> , P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup>	I <sub>OL</sub> =200μA			0.45	V
		X <sub>OUT</sub>	I <sub>OL</sub> =1mA			2.0	V
		X <sub>COU</sub> T	No load applied		0		V
V <sub>T+</sub> -V <sub>T-</sub>	Hysteresis	HOLD, RDY, TA0 <sub>IN</sub> -TA4 <sub>IN</sub> , TB0 <sub>IN</sub> -TB5 <sub>IN</sub> , INT0-INT5, AD <sub>TRG</sub> , CTS0-CTS4, CLK0-CLK4, TA0 <sub>OUT</sub> -TA4 <sub>OUT</sub> , NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I <sub>IH</sub>	Input high ("H") current	P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	V <sub>I</sub> =5V			5.0	μA
I <sub>IL</sub>	Input low ("L") current	P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>0</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	V <sub>I</sub> =0V			-5.0	μA
R <sub>PULLUP</sub>	Pull-up resistance	P0 <sub>0</sub> -P0 <sub>7</sub> , P1 <sub>0</sub> -P1 <sub>7</sub> , P2 <sub>0</sub> -P2 <sub>7</sub> , P3 <sub>0</sub> -P3 <sub>7</sub> , P4 <sub>0</sub> -P4 <sub>7</sub> , P5 <sub>0</sub> -P5 <sub>7</sub> , P6 <sub>0</sub> -P6 <sub>7</sub> , P7 <sub>2</sub> -P7 <sub>7</sub> , P8 <sub>0</sub> -P8 <sub>4</sub> , P8 <sub>6</sub> , P8 <sub>7</sub> , P9 <sub>0</sub> -P9 <sub>7</sub> , P10 <sub>0</sub> -P10 <sub>7</sub> , P11 <sub>0</sub> -P11 <sub>4</sub> , P12 <sub>0</sub> -P12 <sub>7</sub> , P13 <sub>0</sub> -P13 <sub>7</sub> , P14 <sub>0</sub> -P14 <sub>6</sub> , P15 <sub>0</sub> -P15 <sub>7</sub> <sup>(1)</sup>	V <sub>I</sub> =0V	30	50	167	kΩ
R <sub>fXIN</sub>	Feedback resistance	X <sub>IN</sub>			1.5		MΩ
R <sub>fXCIN</sub>	Feedback resistance	X <sub>CIN</sub>			10		MΩ
V <sub>RAM</sub>	RAM standby voltage	Through VDC		2.5			V
I <sub>CC</sub>	Power supply current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V <sub>SS</sub> .	f(X <sub>IN</sub> )=32 MHz, square wave, no division		41	58	mA
			f(X <sub>IN</sub> )=30 MHz, square wave, no division		38	54	mA
			f(X <sub>CIN</sub> )=32 kHz, with a wait state, Topr=25° C		470		μA
			Topr=25° C when the clock stops		0.4	20	μA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.



V<sub>CC</sub> = 5V

**Table 5.4 A/D Conversion Characteristics (V<sub>CC</sub> = AV<sub>CC</sub> = V<sub>REF</sub> = 4.2 to 5.5V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V  
at Topr = -20 to 85°C, f(X<sub>IN</sub>) = 30MHz unless otherwise specified)**

Symbol	Parameter	Measurement condition	Standard			Unit	
			Min	Typ	Max		
-	Resolution	V <sub>REF</sub> =V <sub>CC</sub>			10	Bits	
INL	Integral nonlinearity error	V <sub>REF</sub> =V <sub>CC</sub> =5V	AN <sub>0</sub> to AN <sub>7</sub> AN <sub>EX0</sub> , AN <sub>EX1</sub>			±3	LSB
							LSB
						±7	LSB
		External op-amp connection mode				LSB	
DNL	Differential nonlinearity error				±1	LSB	
-	Offset error				±3	LSB	
-	Gain error				±3	LSB	
R <sub>LADDER</sub>	Resistor ladder	V <sub>REF</sub> =V <sub>CC</sub>	8		40	kΩ	
t <sub>CONV</sub>	10-bit conversion time		2.1			μs	
t <sub>CONV</sub>	8-bit conversion time		1.8			μs	
t <sub>SAMP</sub>	Sample time		0.2			μs	
V <sub>REF</sub>	Reference voltage		2		V <sub>CC</sub>	V	
V <sub>IA</sub>	Analog input voltage		0		V <sub>REF</sub>	V	

## NOTES:

1. Divide f(X<sub>IN</sub>), if exceeding 16 MHz, to keep φ<sub>AD</sub> frequency less than or equal to 16 MHz.

**Table 5.5 D/A Conversion Characteristics (V<sub>CC</sub> = V<sub>REF</sub> = 4.2 to 5.5V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V  
at Topr = -20 to 85°C, f(X<sub>IN</sub>) = 30MHz unless otherwise specified)**

Symbol	Parameter	Measurement condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute accuracy				1.0	%
t <sub>SU</sub>	Setup time				3	μs
R <sub>O</sub>	Output resistance		4	10	20	kΩ
I <sub>VREF</sub>	Reference power supply input current	(Note 1)			1.5	mA

## NOTES:

1. Measurement condition is that one of two D/A converters is used and the DA<sub>i</sub> register (i=0, 1) for the unused D/A converter to "0016". The resistor ladder in the A/D converter is excluded.  
I<sub>VREF</sub> flows even if the ADiCON1 register is set to "0" (no V<sub>REF</sub> connection).

**Table 5.6 Flash Memory Characteristics**

Parameter	Standard			Unit
	Min	Typ	Max	
Program time (1 Page)		8	120	ms
Block erase time (1 Block)		50	600	ms

## NOTES:

1. V<sub>CC</sub> = 4.2 to 5.5V (through VDC), 3.0 to 3.6 V (not through VDC), Topr = 0 to 60° C unless otherwise specified.

V<sub>CC</sub> = 5VTiming Requirements (V<sub>CC</sub> = 4.2 to 5.5V, V<sub>SS</sub> = 0V at Topr = -20 to 85°C unless otherwise specified)

Table 5.7 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>c</sub>	External clock input cycle time	33		ns
t <sub>w(H)</sub>	External clock input high ("H") pulse width	13		ns
t <sub>w(L)</sub>	External clock input low ("L") pulse width	13		ns
t <sub>r</sub>	External clock rising edge time		5	ns
t <sub>f</sub>	External clock falling edge time		5	ns

Table 5.8 Memory Expansion and Microprocessor Modes

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>ac1(RD-DB)</sub>	Data input access time (RD standard, with no wait state)		(Note 1)	ns
t <sub>ac1(AD-DB)</sub>	Data input access time (AD standard, CS standard, with no wait state)		(Note 1)	ns
t <sub>ac2(RD-DB)</sub>	Data input access time (RD standard, with a wait state)		(Note 1)	ns
t <sub>ac2(AD-DB)</sub>	Data input access time (AD standard, CS standard, with a wait state)		(Note 1)	ns
t <sub>ac3(RD-DB)</sub>	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
t <sub>ac3(AD-DB)</sub>	Data input access time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
t <sub>ac4(RAS-DB)</sub>	Data input access time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
t <sub>ac4(CAS-DB)</sub>	Data input access time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
t <sub>ac4(CAD-DB)</sub>	Data input access time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
t <sub>su(DB-BCLK)</sub>	Data input setup time	26		ns
t <sub>su(RDY-BCLK)</sub>	$\overline{\text{RDY}}$ input setup time	26		ns
t <sub>su(HOLD-BCLK)</sub>	$\overline{\text{HOLD}}$ input setup time	30		ns
t <sub>h(RD-DB)</sub>	Data input hold time	0		ns
t <sub>h(CAS-DB)</sub>	Data input hold time	0		ns
t <sub>h(BCLK-RDY)</sub>	$\overline{\text{RDY}}$ input hold time	0		ns
t <sub>h(BCLK-HOLD)</sub>	$\overline{\text{HOLD}}$ input hold time	0		ns
t <sub>d(BCLK-HLDA)</sub>	$\overline{\text{HLDA}}$ output delay time		25	ns

## NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency. Insert a wait state or use lower f<sub>(BCLK)</sub> as an operation frequency if a calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}]$$

$$t_{ac1(AD-DB)} = \frac{10^9}{f_{(BCLK)}} - 35 \quad [\text{ns}]$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \quad (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$t_{ac3(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$t_{ac4(RAS-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$t_{ac4(CAS-DB)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (n=1 \text{ with 1 wait state and } n=3 \text{ when 2 wait states})$$

$$t_{ac4(CAD-DB)} = \frac{10^9 \times l}{f_{(BCLK)}} - 35 \quad [\text{ns}] \quad (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

V<sub>CC</sub> = 5V**Timing Requirements**(V<sub>CC</sub> = 4.2 to 5.5V, V<sub>SS</sub> = 0V at T<sub>opr</sub> = -20 to 85°C unless otherwise specified)**Table 5.9 Timer A Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TA <sub>in</sub> input cycle time	100		ns
tw(TAH)	TA <sub>in</sub> input high ("H") pulse width	40		ns
tw(TAL)	TA <sub>in</sub> input low ("L") pulse width	40		ns

**Table 5.10 Timer A Input (Gate Input in Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TA <sub>in</sub> input cycle time	400		ns
tw(TAH)	TA <sub>in</sub> input high ("H") pulse width	200		ns
tw(TAL)	TA <sub>in</sub> input low ("L") pulse width	200		ns

**Table 5.11 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TA <sub>in</sub> input cycle time	200		ns
tw(TAH)	TA <sub>in</sub> input high ("H") pulse width	100		ns
tw(TAL)	TA <sub>in</sub> input low ("L") pulse width	100		ns

**Table 5.12 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(TAH)	TA <sub>in</sub> input high ("H") pulse width	100		ns
tw(TAL)	TA <sub>in</sub> input low ("L") pulse width	100		ns

**Table 5.13 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(UP)	TA <sub>IOU</sub> T input cycle time	2000		ns
tw(UPH)	TA <sub>IOU</sub> T input high ("H") pulse width	1000		ns
tw(UPL)	TA <sub>IOU</sub> T input low ("L") pulse width	1000		ns
tsu(UP-TIN)	TA <sub>IOU</sub> T input setup time	400		ns
th(TIN-UP)	TA <sub>IOU</sub> T input hold time	400		ns

V<sub>CC</sub> = 5V**Timing Requirements**(V<sub>CC</sub> = 4.2 to 5.5V, V<sub>SS</sub> = 0V at T<sub>opr</sub> = -20 to 85°C unless otherwise specified)**Table 5.14 Timer B Input (Count Source Input in eEvent Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>C(TB)</sub>	TBi <sub>IN</sub> input cycle time (counted on one edge)	100		ns
t <sub>w(TBH)</sub>	TBi <sub>IN</sub> input high ("H") pulse width (counted on one edge)	40		ns
t <sub>w(TBL)</sub>	TBi <sub>IN</sub> input low ("L") pulse width (counted on one edge)	40		ns
t <sub>C(TB)</sub>	TBi <sub>IN</sub> input cycle time (counted on both edges)	200		ns
t <sub>w(TBH)</sub>	TBi <sub>IN</sub> input high ("H") pulse width (counted on both edges)	80		ns
t <sub>w(TBL)</sub>	TBi <sub>IN</sub> input low ("L") pulse width (counted on both edges)	80		ns

**Table 5.15 Timer B Input (Pulse Period Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>C(TB)</sub>	TBi <sub>IN</sub> input cycle time	400		ns
t <sub>w(TBH)</sub>	TBi <sub>IN</sub> input high ("H") pulse width	200		ns
t <sub>w(TBL)</sub>	TBi <sub>IN</sub> input low ("L") pulse width	200		ns

**Table 5.16 Timer B Input (Pulse Width Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>C(TB)</sub>	TBi <sub>IN</sub> input cycle time	400		ns
t <sub>w(TBH)</sub>	TBi <sub>IN</sub> input high ("H") pulse width	200		ns
t <sub>w(TBL)</sub>	TBi <sub>IN</sub> input low ("L") pulse width	200		ns

**Table 5.17 A/D trigger Input**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>C(AD)</sub>	$\overline{\text{AD}}_{\text{TRG}}$ input high ("H") pulse width (trigger available at minimum)	1000		ns
t <sub>w(ADL)</sub>	$\overline{\text{AD}}_{\text{TRG}}$ input low ("L") pulse width	125		ns

**Table 5.18 Serial I/O**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>C(CLK)</sub>	CLK <sub>i</sub> input cycle time	200		ns
t <sub>w(CLKH)</sub>	CLK <sub>i</sub> input high ("H") pulse width	100		ns
t <sub>w(CLKL)</sub>	CLK <sub>i</sub> input low ("L") pulse width	100		ns
t <sub>d(C-Q)</sub>	TxD <sub>i</sub> output delay time		80	ns
t <sub>h(C-Q)</sub>	TxD <sub>i</sub> hold time	0		ns
t <sub>SU(D-C)</sub>	RxD <sub>i</sub> input hold time	30		ns
t <sub>h(C-Q)</sub>	RxD <sub>i</sub> input hold time	90		ns

**Table 5.19 External Interrupt  $\overline{\text{INT}}_i$  Input**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>w(INH)</sub>	$\overline{\text{INT}}_i$ input high ("H") pulse width	250		ns
t <sub>w(INL)</sub>	$\overline{\text{INT}}_i$ input low ("L") pulse width	250		ns

V<sub>CC</sub> = 5V**Switching Characteristics**(V<sub>CC</sub> = 4.2 to 5.5V, V<sub>SS</sub> = 0V at T<sub>opr</sub> = -20 to 85°C unless otherwise specified)**Table 5.20 Memory Expansion Mode and Microprocessor Mode (with No Wait State)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
t <sub>d(BCLK-AD)</sub>	Address output delay time	See Figure 5.1		18	ns
t <sub>h(BCLK-AD)</sub>	Address output hold time (BCLK standard)		-3		ns
t <sub>h(RD-AD)</sub>	Address output hold time (RD standard)		0		ns
t <sub>h(WR-AD)</sub>	Address output hold time (WR standard)		(Note 1)		ns
t <sub>d(BCLK-CS)</sub>	Chip-select signal output delay time			18	ns
t <sub>h(BCLK-CS)</sub>	Chip-select signal output hold time (BCLK standard)		-3		ns
t <sub>h(RD-CS)</sub>	Chip-select signal output hold time (RD standard)		0		ns
t <sub>h(WR-CS)</sub>	Chip-select signal output hold time (WR standard)		(Note 1)		ns
t <sub>d(BCLK-ALE)</sub>	ALE signal output delay time			18	ns
t <sub>h(BCLK-ALE)</sub>	ALE signal output hold time		-2		ns
t <sub>d(BCLK-RD)</sub>	RD signal output delay time			18	ns
t <sub>h(BCLK-RD)</sub>	RD signal output hold time		-5		ns
t <sub>d(BCLK-WR)</sub>	WR signal output delay time			18	ns
t <sub>d(BCLK-WR)</sub>	WR signal output hold time		-3		ns
t <sub>d(DB-WR)</sub>	Data output delay time (WR standard)		(Note 1)		ns
t <sub>h(WR-DB)</sub>	Data output hold time (WR standard)		(Note 1)		ns
t <sub>w(WR)</sub>	WR output width		(Note 1)		ns

## NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [\text{ns}]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{w(WR)} = \frac{10^9}{f_{(BCLK)} \times 2} - 15 \quad [\text{ns}]$$

V<sub>CC</sub> = 5V**Switching Characteristics**(V<sub>CC</sub> = 4.2 to 5.5V, V<sub>SS</sub> = 0V at T<sub>opr</sub> = -20 to 85°C unless otherwise specified)**Table 5.21 Memory Expansion Mode and Microprocessor Mode  
(With a Wait State, Accessing an External Memory)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)		0		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time			18	ns
th(BCLK-ALE)	ALE signal output hold time		-2		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
td(BCLK-WR)	WR signal output hold time		-3		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(WR-DB)	Data output hold time (WR standard)		(Note 1)		ns
tw(WR)	WR output width		(Note 1)		ns

**NOTES:**

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$td(DB - WR) = \frac{10^9 \times n}{f(BCLK)} - 20 \quad [ns] \quad (n=1 \text{ with 1 wait state, } n=2 \text{ with 2 wait states} \\ \text{and } n=3 \text{ with 3 wait states})$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \quad [ns] \quad (n=1 \text{ with 1 wait state, } n=3 \text{ with 2 wait states} \\ \text{and } n=5 \text{ with 3 wait states})$$

V<sub>CC</sub> = 5V**Switching Characteristics**(V<sub>CC</sub> = 4.2 to 5.5V, V<sub>SS</sub> = 0V at T<sub>opr</sub> = -20 to 85°C unless otherwise specified)**Table 5.22 Memory Expansion Mode and Microprocessor Mode  
(With a Wait State, Accessing an External Memory and Selecting a Space with the  
Multiplexed Bus)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)		(Note 1)		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-AD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		-3		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(WR-DB)	Data output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		-2		ns
td(AD-ALE)	ALE signal output delay time (address standard)		(Note 1)	18	ns
th(ALE-AD)	ALE signal output hold time (address standard)		(Note 1)		ns
tdZ(RD-AD)	Address output high-impedance time			8	ns

**NOTES:**

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$th(RD - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(DB - WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(AD - ALE) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

$$th(ALE - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

V<sub>CC</sub> = 5V**Switching Characteristics**(V<sub>CC</sub> = 4.2 to 5.5V, V<sub>SS</sub> = 0V at T<sub>opr</sub> = -20 to 85°C unless otherwise specified)**Table 5.23 Memory Expansion Mode and Microprocessor Mode  
(With a Wait State, Accessing an External Memory and Selecting a DRAM Space)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
t <sub>d(BCLK-AD)</sub>	Row address output delay time	See Figure 5.1		18	ns
t <sub>h(BCLK-AD)</sub>	Row address output hold time (BCLK standard)		-3		ns
t <sub>h(BCLK-CAD)</sub>	Column address output delay time			18	ns
t <sub>d(BCLK-CAD)</sub>	Column address output hold time (BCLK standard)		-3		ns
t <sub>h(RAS-RAD)</sub>	Row address output hold time after RAS output		(Note 1)		ns
t <sub>d(BCLK-RAS)</sub>	RAS output delay time (BCLK standard)			18	ns
t <sub>h(BCLK-RAS)</sub>	RAS output hold time (BCLK standard)		-3		ns
t <sub>RP</sub>	RAS high ("H") hold time		(Note 1)		ns
t <sub>d(BCLK-CAS)</sub>	CAS output delay time (BCLK standard)			18	ns
t <sub>h(BCLK-CAS)</sub>	CAS output hold time (BCLK standard)		-3		ns
t <sub>d(BCLK-DW)</sub>	DW output delay time (BCLK standard)			18	ns
t <sub>h(BCLK-DW)</sub>	DW output hold time (BCLK standard)		-5		ns
t <sub>su(DB-CAS)</sub>	CAS output setup time after DB output		(Note 1)		ns
t <sub>h(BCLK-DB)</sub>	DB signal output hold time (BCLK standard)		-7		ns
t <sub>su(CAS-RAS)</sub>	CAS output setup time before RAS output (refresh)		(Note 1)		ns

## NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

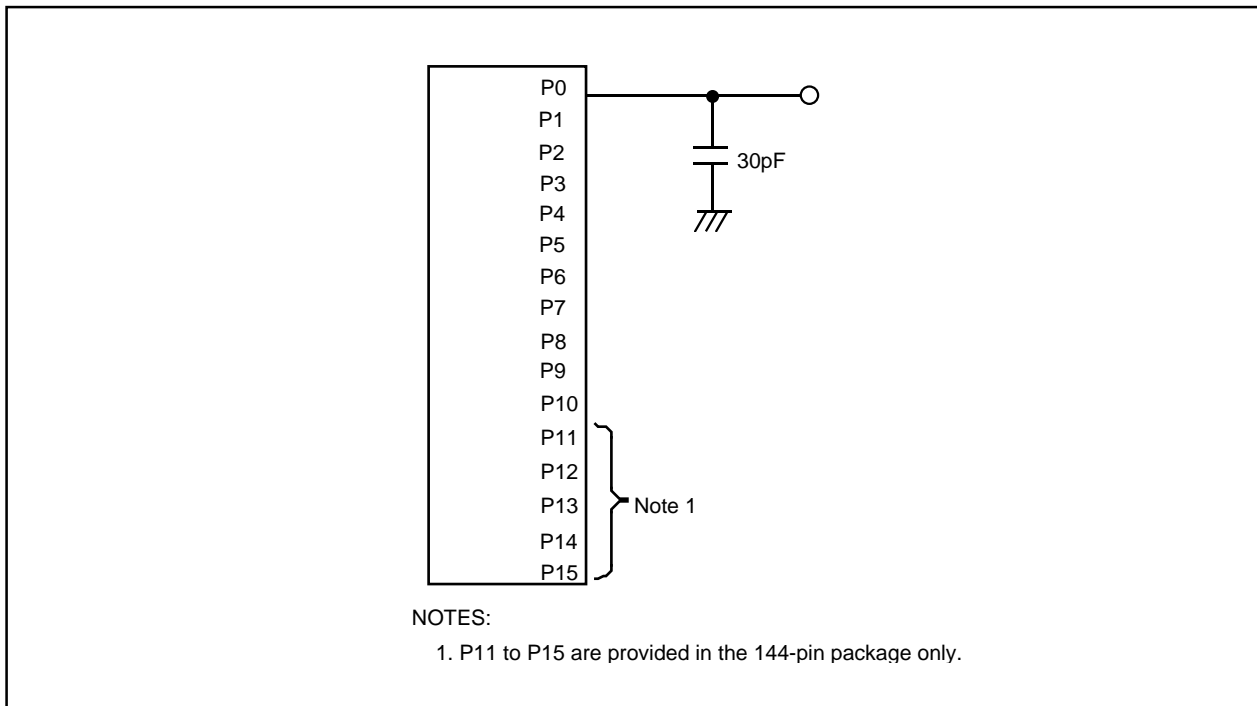
$$t_{h(RAS - RAD)} = \frac{10^9}{f(\text{BCLK}) \times 2} - 13 \quad [\text{ns}]$$

$$t_{RP} = \frac{10^9}{f(\text{BCLK}) \times 2} \times 3 - 20 \quad [\text{ns}]$$

$$t_{su(\text{DB} - \text{CAS})} = \frac{10^9}{f(\text{BCLK})} - 20 \quad [\text{ns}]$$

$$t_{su(\text{CAS} - \text{RAS})} = \frac{10^9}{f(\text{BCLK}) \times 2} - 13 \quad [\text{ns}]$$





**Figure 5.1 P0 to P15 Measurement Circuit**

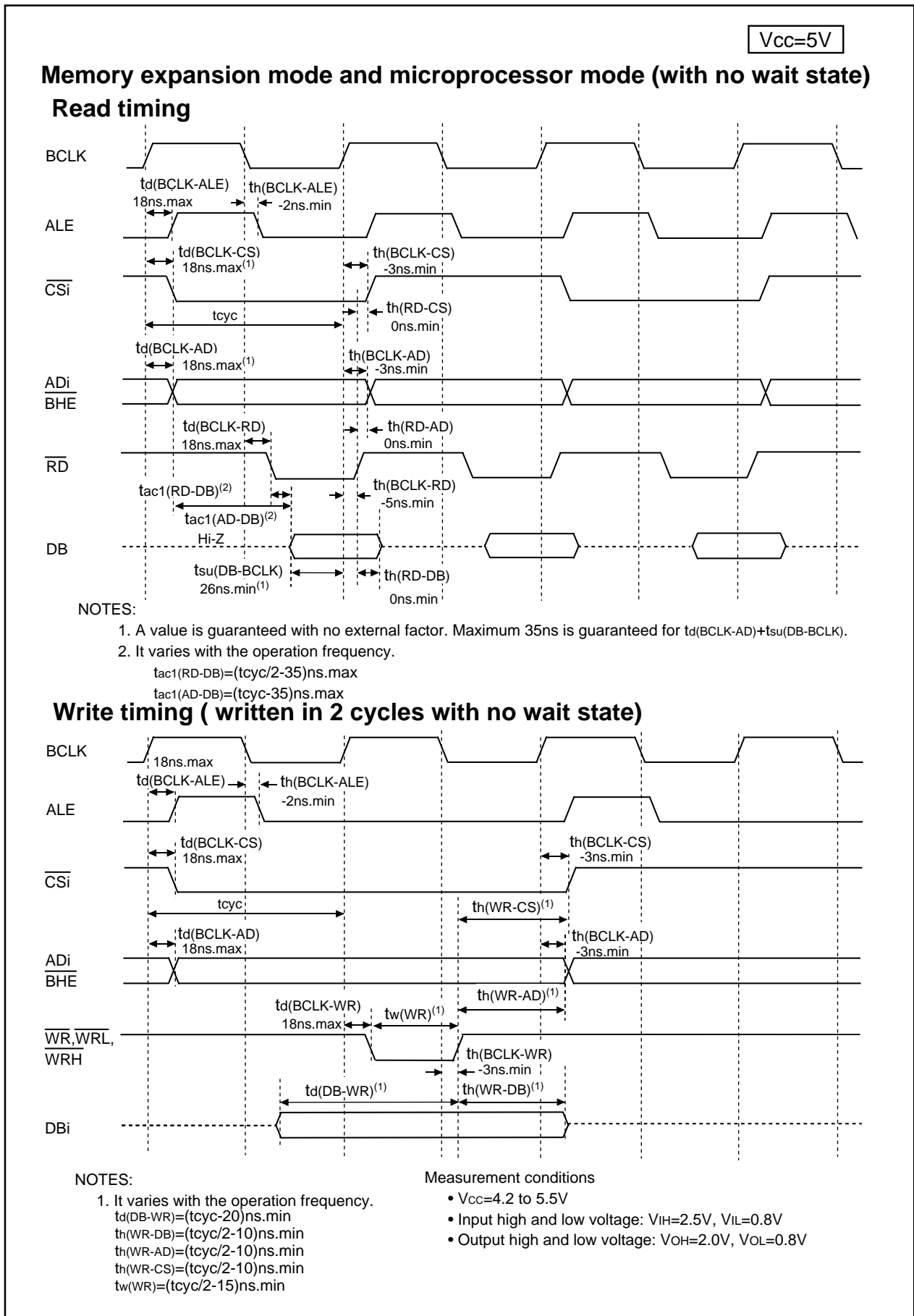


Figure 5.2 Vcc=5V Timing Diagram (1)

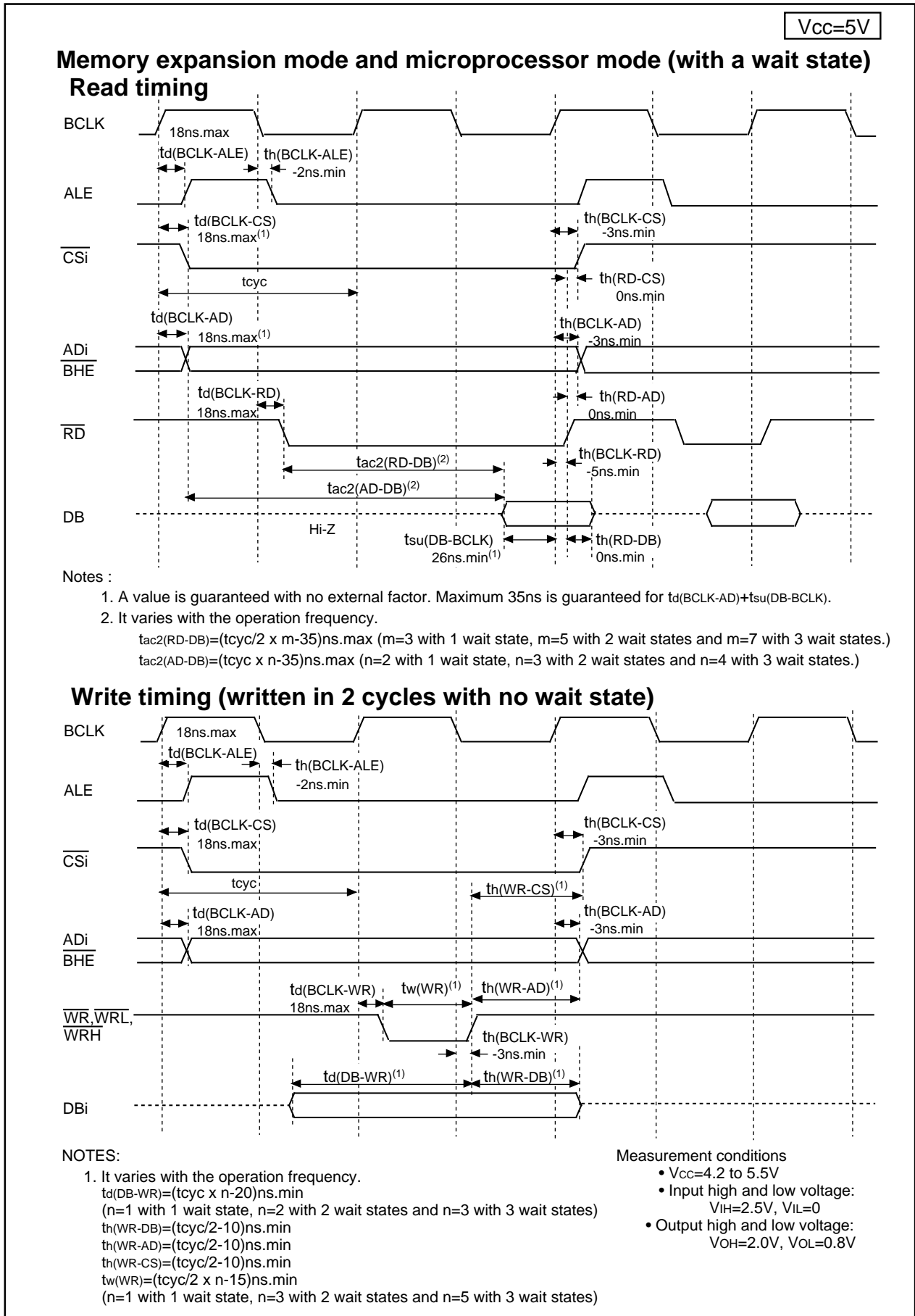


Figure 5.3 VCC=5V Timing Diagram (2)

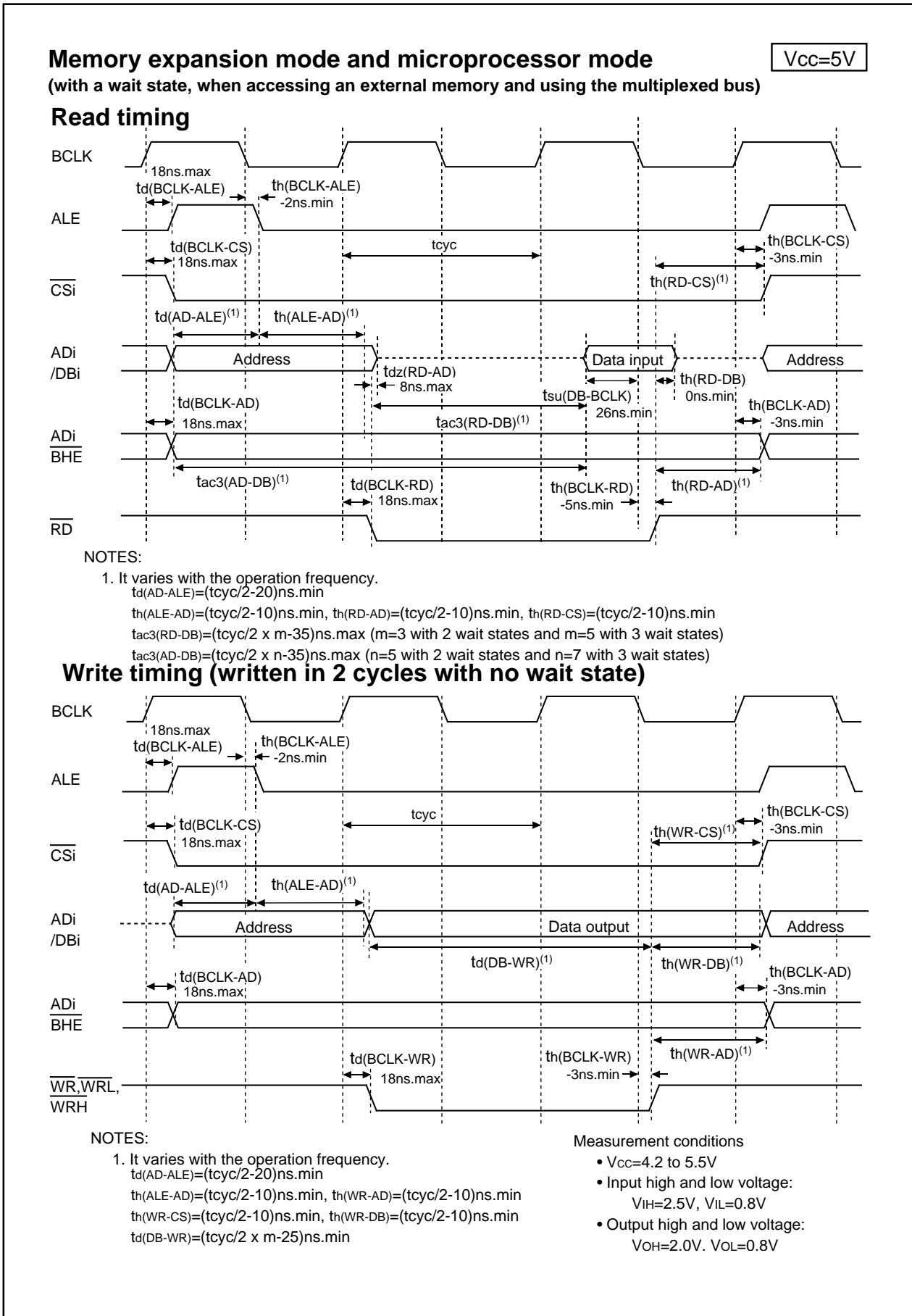


Figure 5.4 VCC=5V Timing Diagram (3)

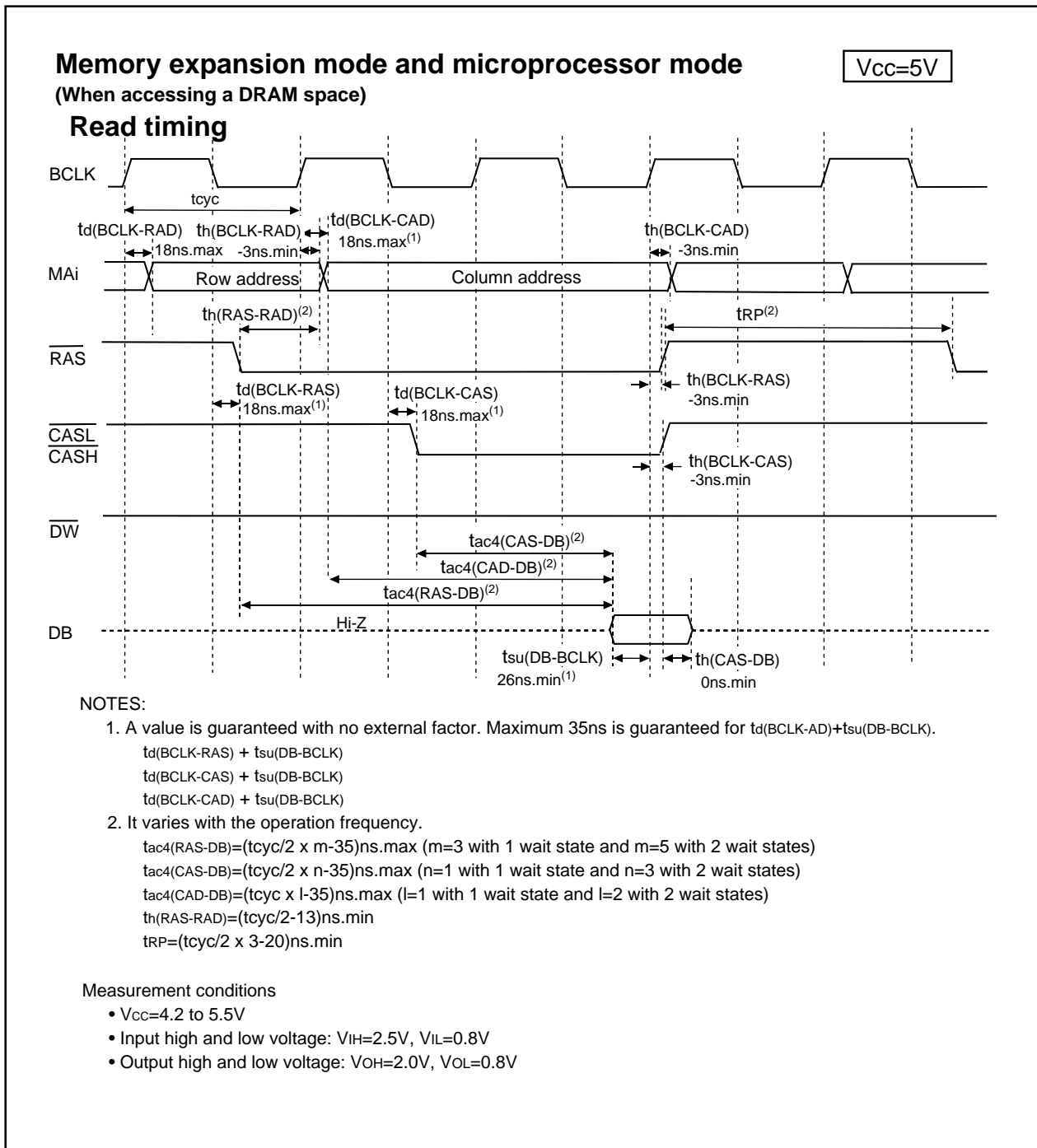


Figure 5.5 VCC=5V Timing Diagram (4)

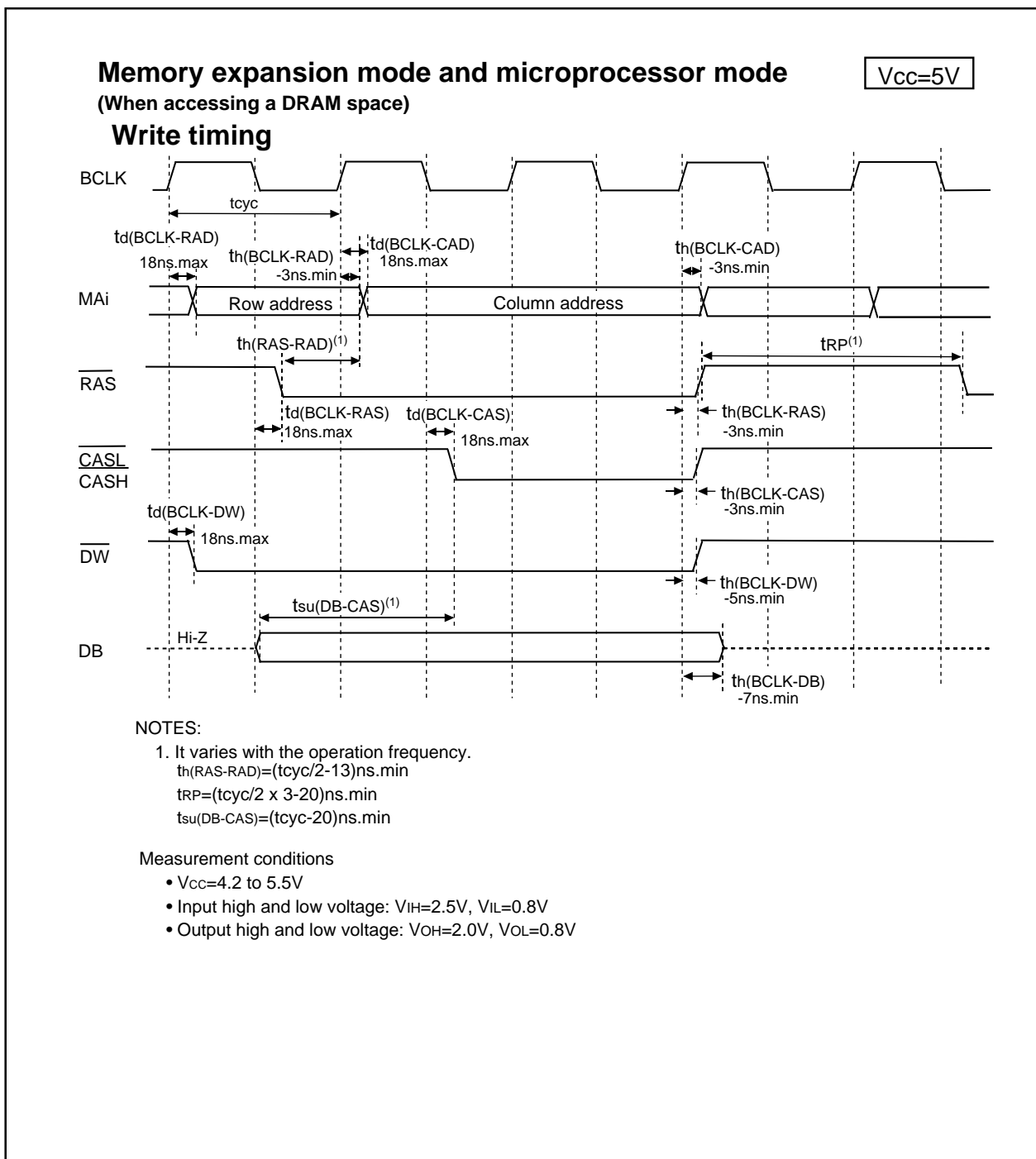


Figure 5.6 V<sub>CC</sub>=5V Timing Diagram (5)

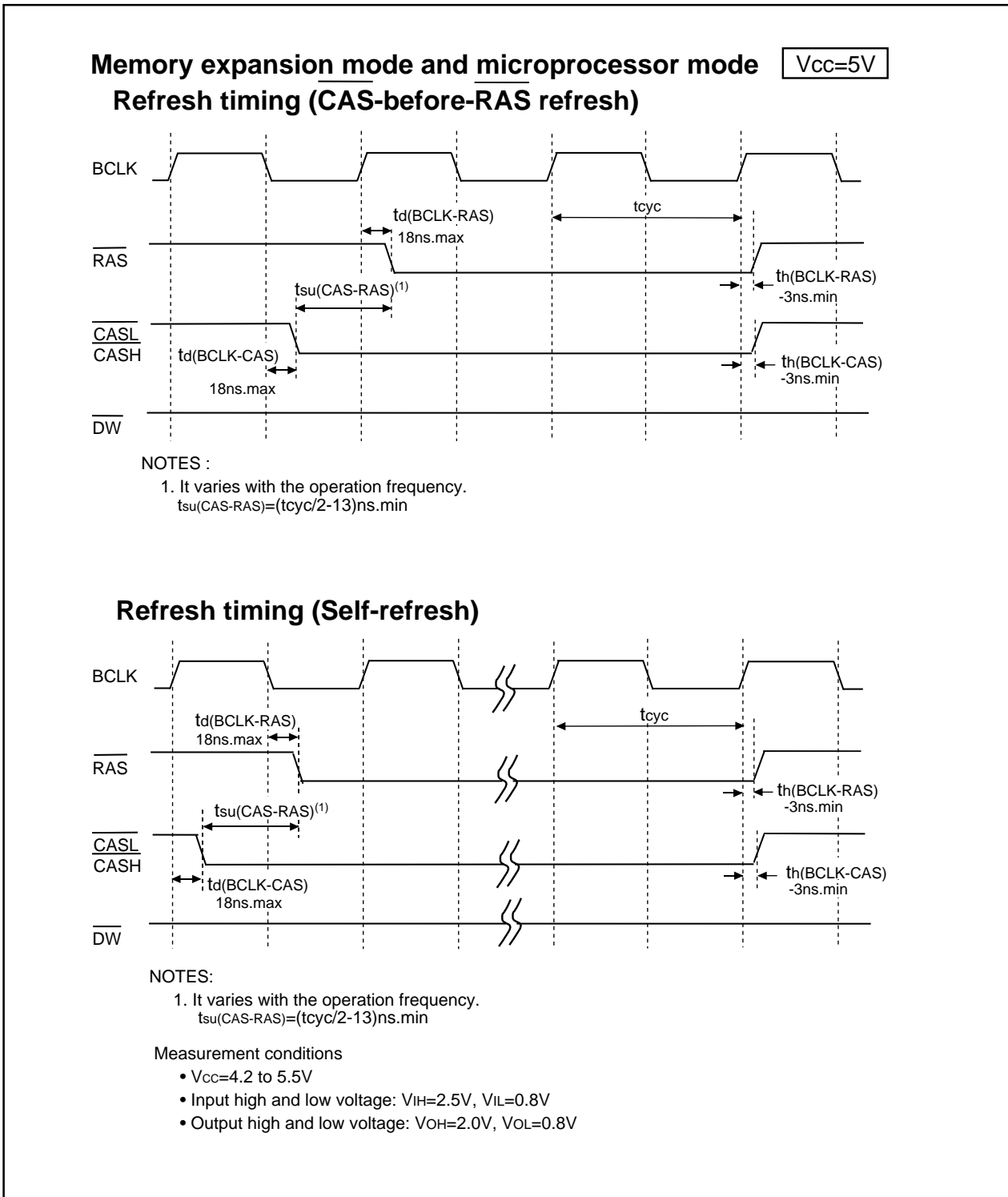


Figure 5.7 V<sub>CC</sub>=5V Timing Diagram (6)

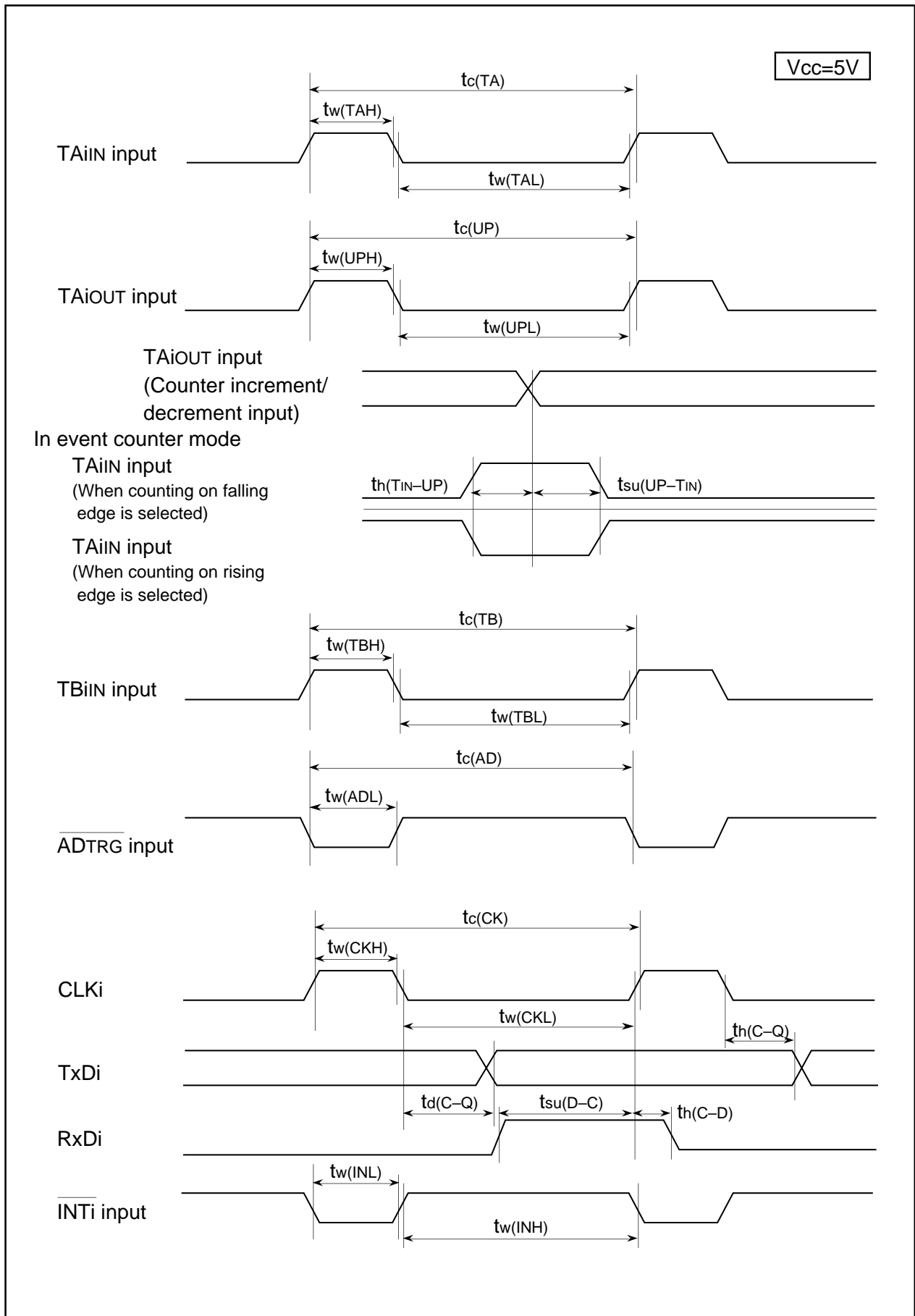


Figure 5.8 Vcc=5V Timing Diagram (7)



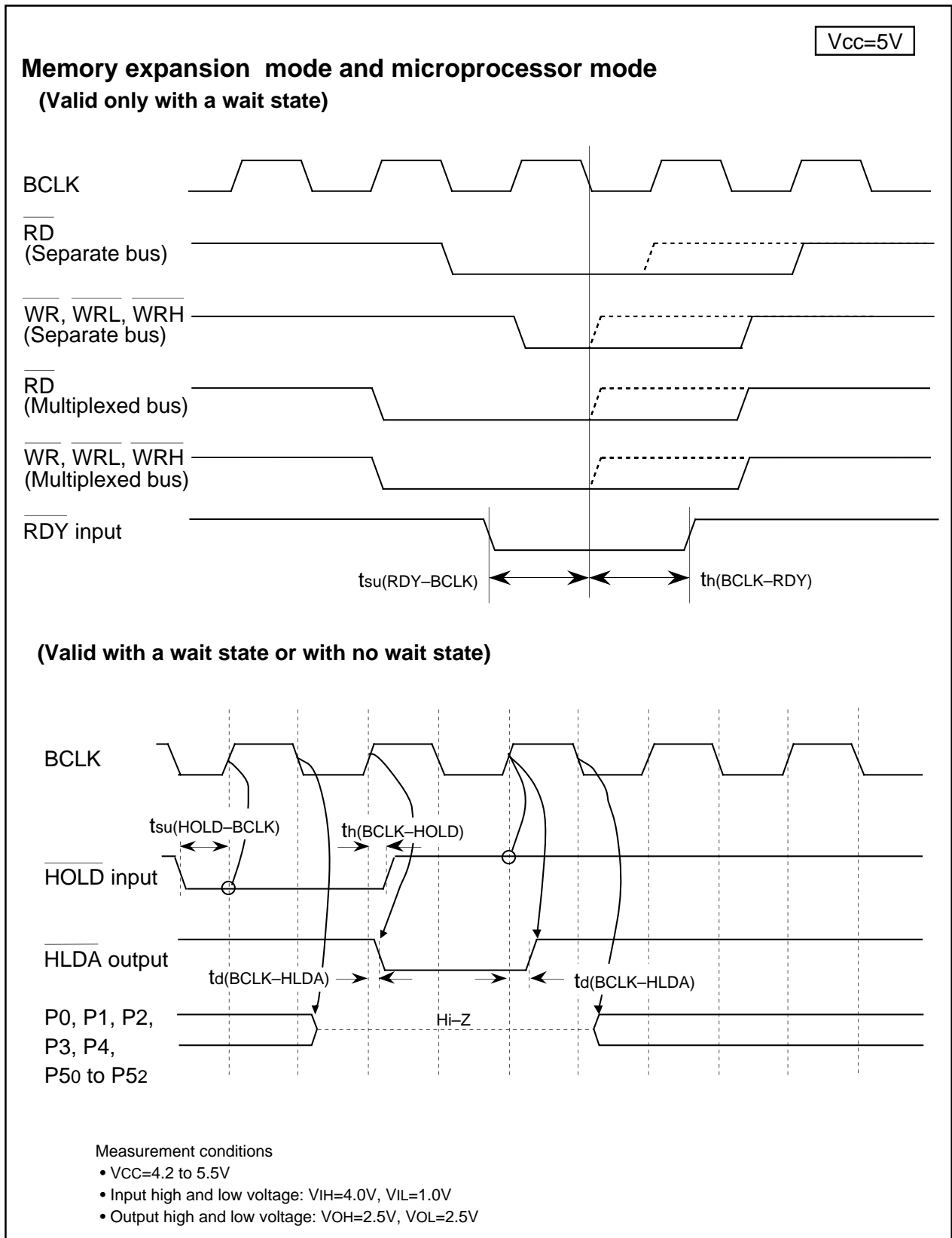


Figure 5.9 Vcc=5V Timing Diagram (8)

VCC = 3.3V

**Table 5.24 Electrical Characteristics (VCC=3.0 to 3.6V, VSS=0V at Topr = -20 to 85°C,  
f(XIN)=20MHz unless otherwise specified)**

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
VOH	Output high ("H") voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>	I <sub>OH</sub> =-1mA	2.7			V
		X <sub>OUT</sub>	I <sub>OH</sub> =-0.1mA	2.7			V
		X <sub>COU</sub> T	No load applied		3.3		V
VOL	Output low ("L") voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>	I <sub>OL</sub> =1mA			0.5	V
		X <sub>OUT</sub>	I <sub>OL</sub> =0.1mA			0.5	V
		X <sub>COU</sub> T	No load applied		0		V
VT+-VT-	Hysteresis	HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, ADTRG, CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I <sub>IH</sub>	Input high ("H") current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	V <sub>I</sub> =3V			4.0	μA
I <sub>IL</sub>	Input low ("L") current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	V <sub>I</sub> =0V			-4.0	μA
R <sub>PULLUP</sub>	Pull-up resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 <sup>(1)</sup>	V <sub>I</sub> =0V	66	120	500	kΩ
R <sub>fXIN</sub>	Feedback resistance	X <sub>IN</sub>			3.0		MΩ
R <sub>fXCIN</sub>	Feedback resistance	X <sub>CIN</sub>			20.0		MΩ
V <sub>RAM</sub>	RAM standby voltage	Through VDC		2.5			V
		Not through VDC		2.0			
I <sub>CC</sub>	Power supply current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to V <sub>SS</sub> .	f(X <sub>IN</sub> )=20 MHz, square wave, no division		26	38	mA
			f(X <sub>CIN</sub> )=32 kHz, with a wait state, not through VDC, Topr=25° C		5.0		μA
			f(X <sub>CIN</sub> )=32 kHz, with a wait state, through VDC, Topr=25° C		340		μA
			Topr=25° C when the clock stops		0.4	20	μA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

**VCC = 3.3V****VSS = AVSS = 0V****Table 5.25 A/D Conversion Characteristics (VCC = AVCC = VREF = 3.0 to 3.6V, at Topr = -20 to 85°C, f(XIN) = 20MHz unless otherwise specified)**

Symbol	Parameter		Measurement condition	Standard			Unit
				Min	Typ	Max	
-	Resolution		VREF=VCC			10	Bits
INL	Integral nonlinearity error	No S&H function (8-bit)	VCC=VREF=3.3V			±2	LSB
DNL	Differential nonlinearity error	No S&H function (8-bit)				±1	LSB
-	Offset error	No S&H function (8-bit)				±2	LSB
-	Gain error	No S&H function (8-bit)				±2	LSB
RLADDER	Resistor ladder		VREF=VCC	8		40	kΩ
tCONV	8-bit conversion time			4.9			μs
VREF	Reference voltage			3.0		VCC	V
VIA	Analog input voltage			0		VREF	V

S&amp;H: Sample and hold

## NOTES:

1. Divide f(XIN), if exceeding 10 MHz, to keep φAD frequency less than or equal to 10 MHz.

**Table 5.26 D/A Conversion Characteristics (VCC = VREF = 3.0 to 3.6V, VSS = AVSS = 0V at Topr = -20 to 85°C, f(XIN) = 20MHz unless otherwise specified)**

Symbol	Parameter	Measurement condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute accuracy				1.0	%
tsu	Setup time				3	μs
Ro	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(Note 1)			1.0	mA

## NOTES:

1. Measurement condition is that one of two D/A converters is used and the DAi register (i=0, 1) for the unused D/A converter to "0016". The resistor ladder in the A/D converter is excluded. IVREF flows even if the ADiCON1 register is set to "0" (no VREF connection).

**Table 5.27 Flash Memory Characteristics**

Parameter	Standard			Unit
	Min	Typ	Max	
Program time (1 Page)		8	120	ms
Block erase time (1 Block)		50	600	ms

## NOTES:

1. VCC = 4.2 to 5.5V (through VDC), 3.0 to 3.6 V (not through VDC), Topr = 0 to 60° C unless otherwise specified.

V<sub>CC</sub> = 3.3VTiming Requirements (V<sub>CC</sub> = 3.0 to 3.6V, V<sub>SS</sub> = 0V at Topr = -20 to 85°C unless otherwise specified)**Table 5.28 External Clock Input**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>c</sub>	External clock input cycle time	50		ns
t <sub>w(H)</sub>	External clock input high ("H") pulse width	22		ns
t <sub>w(L)</sub>	External clock input low ("L") pulse width	22		ns
t <sub>r</sub>	External clock rising-edge time		5	ns
t <sub>f</sub>	External clock falling-edge time		5	ns

**Table 5.29 Memory Expansion Mode and Microprocessor Mode**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>ac1(RD-DB)</sub>	Data input access time (RD standard, with no wait state)		(Note 1)	ns
t <sub>ac1(AD-DB)</sub>	Data input access time (AD standard, CS standard, with no wait state)		(Note 1)	ns
t <sub>ac2(RD-DB)</sub>	Data input access time (RD standard, with a wait state)		(Note 1)	ns
t <sub>ac2(AD-DB)</sub>	Data input access time (AD standard, CS standard, with a wait state)		(Note 1)	ns
t <sub>ac3(RD-DB)</sub>	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
t <sub>ac3(AD-DB)</sub>	Data input access time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
t <sub>ac4(RAS-DB)</sub>	Data input access time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
t <sub>ac4(CAS-DB)</sub>	Data input access time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
t <sub>ac4(CAD-DB)</sub>	Data input access time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
t <sub>su(DB-BCLK)</sub>	Data input setup time	30		ns
t <sub>su(RDY-BCLK)</sub>	RDY input setup time	40		ns
t <sub>su(HOLD-BCLK)</sub>	HOLD input setup time	60		ns
t <sub>h(RD-DB)</sub>	Data input hold time	0		ns
t <sub>h(CAS-DB)</sub>	Data input hold time	0		ns
t <sub>h(BCLK-RDY)</sub>	RDY input hold time	0		ns
t <sub>h(BCLK-HOLD)</sub>	HOLD input hold time	0		ns
t <sub>d(BCLK-HLDA)</sub>	HLDA output delay time		25	ns

## NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency. Insert a wait state or use lower f<sub>(BCLK)</sub> as an operation frequency if a calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}]$$

$$t_{ac1(AD-DB)} = \frac{10^9}{f_{(BCLK)}} - 35 \quad [\text{ns}]$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \quad (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$t_{ac3(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$t_{ac4(RAS-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$t_{ac4(CAS-DB)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (n=1 \text{ with 1 wait state and } n=3 \text{ when 2 wait states})$$

$$t_{ac4(CAD-DB)} = \frac{10^9 \times l}{f_{(BCLK)}} - 35 \quad [\text{ns}] \quad (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

V<sub>CC</sub> = 3.3V**Timing Requirements****(V<sub>CC</sub> = 3.0 to 3.6V, V<sub>SS</sub> = 0V at Topr = -20 to 85°C unless otherwise specified)****Table 5.30 Timer A Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>c(TA)</sub>	TA <sub>in</sub> input cycle time	100		ns
t <sub>w(TAH)</sub>	TA <sub>in</sub> input high ("H") pulse width	40		ns
t <sub>w(TAL)</sub>	TA <sub>in</sub> input low ("L") pulse width	40		ns

**Table 5.31 Timer A Input (Gate Input in Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>c(TA)</sub>	TA <sub>in</sub> input cycle time	400		ns
t <sub>w(TAH)</sub>	TA <sub>in</sub> input high ("H") pulse width	200		ns
t <sub>w(TAL)</sub>	TA <sub>in</sub> input low ("L") pulse width	200		ns

**Table 5.32 Timer A Input (External Trigger Input in One-Shot Timer Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>c(TA)</sub>	TA <sub>in</sub> input cycle time	200		ns
t <sub>w(TAH)</sub>	TA <sub>in</sub> input high ("H") pulse width	100		ns
t <sub>w(TAL)</sub>	TA <sub>in</sub> input low ("L") pulse width	100		ns

**Table 5.33 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>w(TAH)</sub>	TA <sub>in</sub> input high ("H") pulse width	100		ns
t <sub>w(TAL)</sub>	TA <sub>in</sub> input low ("L") pulse width	100		ns

**Table 5.34 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>c(UP)</sub>	TA <sub>IOU</sub> T input cycle time	2000		ns
t <sub>w(UPH)</sub>	TA <sub>IOU</sub> T input high ("H") pulse width	1000		ns
t <sub>w(UPL)</sub>	TA <sub>IOU</sub> T input low ("L") pulse width	1000		ns
t <sub>su(UP-TIN)</sub>	TA <sub>IOU</sub> T input setup time	400		ns
t <sub>h(TIN-UP)</sub>	TA <sub>IOU</sub> T input hold time	400		ns

VCC = 3.3V

**Timing Requirements****(VCC = 3.0 to 3.6V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)****Table 5.35 Timer B input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>C(TB)</sub>	TB <sub>IN</sub> input cycle time (counted on one edge)	100		ns
t <sub>w(TBH)</sub>	TB <sub>IN</sub> input high ("H") pulse width (counted on one edge)	40		ns
t <sub>w(TBL)</sub>	TB <sub>IN</sub> input low ("L") pulse width (counted on one edge)	40		ns
t <sub>C(TB)</sub>	TB <sub>IN</sub> input cycle time (counted on both edges)	200		ns
t <sub>w(TBH)</sub>	TB <sub>IN</sub> input high ("H") pulse width (counted on both edges)	80		ns
t <sub>w(TBL)</sub>	TB <sub>IN</sub> input low ("L") pulse width (counted on both edges)	80		ns

**Table 5.36 Timer B input (Pulse Period Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>C(TB)</sub>	TB <sub>IN</sub> input cycle time	400		ns
t <sub>w(TBH)</sub>	TB <sub>IN</sub> input high ("H") pulse width	200		ns
t <sub>w(TBL)</sub>	TB <sub>IN</sub> input low ("L") pulse width	200		ns

**Table 5.37 Timer B input (Pulse Width Measurement Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>C(TB)</sub>	TB <sub>IN</sub> input cycle time	400		ns
t <sub>w(TBH)</sub>	TB <sub>IN</sub> input high ("H") pulse width	200		ns
t <sub>w(TBL)</sub>	TB <sub>IN</sub> input low ("L") pulse width	200		ns

**Table 5.38 A/D Trigger Input**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>C(AD)</sub>	$\overline{\text{ADTRG}}$ input high ("H") pulse width (trigger available at minimum)	1000		ns
t <sub>w(ADL)</sub>	$\overline{\text{ADTRG}}$ input low ("L") pulse width	125		ns

**Table 5.39 Serial I/O**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>C(CLK)</sub>	CLK <sub>I</sub> input cycle time	200		ns
t <sub>w(CLKH)</sub>	CLK <sub>I</sub> input high ("H") pulse width	100		ns
t <sub>w(CLKL)</sub>	CLK <sub>I</sub> input low ("L") pulse width	100		ns
t <sub>d(C-Q)</sub>	TxD <sub>I</sub> output delay time		80	ns
t <sub>h(C-Q)</sub>	TxD <sub>I</sub> hold time	0		ns
t <sub>su(D-C)</sub>	RxD <sub>I</sub> input hold time	30		ns
t <sub>h(C-Q)</sub>	RxD <sub>I</sub> input hold time	90		ns

**Table 5.40 External Interrupt INT<sub>I</sub> input**

Symbol	Parameter	Standard		Unit
		Min	Max	
t <sub>w(INH)</sub>	INT <sub>I</sub> input high ("H") pulse width	250		ns
t <sub>w(INL)</sub>	INT <sub>I</sub> input low ("L") pulse width	250		ns

V<sub>CC</sub> = 3.3V**Switching Characteristics**(V<sub>CC</sub> = 3.0 to 3.6V, V<sub>SS</sub> = 0V at T<sub>opr</sub> = -20 to 85°C, unless otherwise specified)**Table 5.41 Memory Expansion Mode and Microprocessor Mode (with No Wait State)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
t <sub>d(BCLK-AD)</sub>	Address output delay time	See Figure 5.1		18	ns
t <sub>h(BCLK-AD)</sub>	Address output hold time (BCLK standard)		0		ns
t <sub>h(RD-AD)</sub>	Address output hold time (RD standard)		0		ns
t <sub>h(WR-AD)</sub>	Address output hold time (WR standard)		(Note 1)		ns
t <sub>d(BCLK-CS)</sub>	Chip-select signal output delay time			18	ns
t <sub>h(BCLK-CS)</sub>	Chip-select signal output hold time (BCLK standard)		0		ns
t <sub>h(RD-CS)</sub>	Chip-select signal output hold time (RD standard)		0		ns
t <sub>h(WR-CS)</sub>	Chip-select signal output hold time (WR standard)		(Note 1)		ns
t <sub>d(BCLK-ALE)</sub>	ALE signal output delay time			18	ns
t <sub>h(BCLK-ALE)</sub>	ALE signal output hold time		-2		ns
t <sub>d(BCLK-RD)</sub>	RD signal output delay time			18	ns
t <sub>h(BCLK-RD)</sub>	RD signal output hold time		-3		ns
t <sub>d(BCLK-WR)</sub>	WR signal output delay time			18	ns
t <sub>d(BCLK-WR)</sub>	WR signal output hold time		0		ns
t <sub>d(DB-WR)</sub>	Data output delay time (WR standard)		(Note 1)		ns
t <sub>h(WR-DB)</sub>	Data output hold time (WR standard)		(Note 1)		ns
t <sub>w(WR)</sub>	WR output width		(Note 1)		ns

## NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [\text{ns}]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{w(WR)} = \frac{10^9}{f_{(BCLK)} \times 2} - 15 \quad [\text{ns}]$$

V<sub>CC</sub> = 3.3V**Switching Characteristics**(V<sub>CC</sub> = 3.0 to 3.6V, V<sub>SS</sub> = 0V at T<sub>opr</sub> = -20 to 85°C unless otherwise specified)**Table 5.42 Memory Expansion Mode and Microprocessor Mode  
(With a Wait State, Accessing an External Memory)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
t <sub>d(BCLK-AD)</sub>	Address output delay time	See Figure 5.1		18	ns
t <sub>h(BCLK-AD)</sub>	Address output hold time (BCLK standard)		0		ns
t <sub>h(RD-AD)</sub>	Address output hold time (RD standard)		0		ns
t <sub>h(WR-AD)</sub>	Address output hold time (WR standard)		(Note 1)		ns
t <sub>d(BCLK-CS)</sub>	Chip-select signal output delay time			18	ns
t <sub>h(BCLK-CS)</sub>	Chip-select signal output hold time (BCLK standard)		0		ns
t <sub>h(RD-CS)</sub>	Chip-select signal output hold time (RD standard)		0		ns
t <sub>h(WR-CS)</sub>	Chip-select signal output hold time (WR standard)		(Note 1)		ns
t <sub>d(BCLK-ALE)</sub>	ALE signal output delay time			18	ns
t <sub>h(BCLK-ALE)</sub>	ALE signal output hold time		-2		ns
t <sub>d(BCLK-RD)</sub>	RD signal output delay time			18	ns
t <sub>h(BCLK-RD)</sub>	RD signal output hold time		-3		ns
t <sub>d(BCLK-WR)</sub>	WR signal output delay time			18	ns
t <sub>d(BCLK-WR)</sub>	WR signal output hold time		0		ns
t <sub>d(DB-WR)</sub>	Data output delay time (WR standard)		(Note 1)		ns
t <sub>h(WR-DB)</sub>	Data output hold time (WR standard)		(Note 1)		ns
t <sub>w(WR)</sub>	WR output width		(Note 1)		ns

**NOTES:**

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9 \times n}{f_{(BCLK)}} - 20 \quad [\text{ns}] \quad (n=1 \text{ with 1 wait state, } n=2 \text{ with 2 wait states} \\ \text{and } n=3 \text{ with 3 wait states})$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [\text{ns}] \quad (n=1 \text{ with 1 wait state, } n=3 \text{ with 2 wait states} \\ \text{and } n=5 \text{ with 3 wait states})$$



V<sub>CC</sub> = 3.3V**Switching Characteristics**(V<sub>CC</sub> = 3.0 to 3.6V, V<sub>SS</sub> = 0V at Topr = -20 to 85°C unless otherwise specified)**Table 5.43 Memory Expansion Mode and Microprocessor Mode  
(With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		0		ns
th(RD-AD)	Address output hold time (RD standard)		(Note 1)		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		0		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-AD)	RD signal output hold time		-3		ns
td(BCLK-WR)	WR signal output delay time			18	ns
td(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(WR-DB)	Data output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		-2		ns
td(AD-ALE)	ALE signal output delay time (address standard)		(Note 1)	18	ns
th(ALE-AD)	ALE signal output hold time (address standard)		(Note 1)		ns
tdZ(RD-AD)	Address output high-impedance time			8	ns

## NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$th(RD - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(DB - WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(AD - ALE) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

$$th(ALE - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

V<sub>CC</sub> = 3.3V**Switching Characteristics**(V<sub>CC</sub> = 3.0 to 3.6V, V<sub>SS</sub> = 0V at T<sub>opr</sub> = -20 to 85°C unless otherwise specified)**Table 5.44 Memory Expansion Mode and Microprocessor Mode  
(With a Wait State, Accessing an External Memory and Selecting a DRAM Space)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
t <sub>d(BCLK-AD)</sub>	Row address output delay time	See Figure 5.1		18	ns
t <sub>h(BCLK-AD)</sub>	Row address output hold time (BCLK standard)		0		ns
t <sub>h(BCLK-CAD)</sub>	Column address output delay time			18	ns
t <sub>d(BCLK-CAD)</sub>	Column address output hold time (BCLK standard)		0		ns
t <sub>h(RAS-RAD)</sub>	Row address output hold time after RAS output		(Note 1)		ns
t <sub>d(BCLK-RAS)</sub>	RAS output delay time (BCLK standard)			18	ns
t <sub>h(BCLK-RAS)</sub>	RAS output hold time (BCLK standard)		0		ns
t <sub>RP</sub>	RAS high ("H") hold time		(Note 1)		ns
t <sub>d(BCLK-CAS)</sub>	CAS output delay time (BCLK standard)			18	ns
t <sub>h(BCLK-CAS)</sub>	CAS output hold time (BCLK standard)		0		ns
t <sub>d(BCLK-DW)</sub>	DW output delay time (BCLK standard)			18	ns
t <sub>h(BCLK-DW)</sub>	DW output hold time (BCLK standard)		-3		ns
t <sub>SU(DB-CAS)</sub>	CAS output setup time after DB output		(Note 1)		ns
t <sub>h(BCLK-DB)</sub>	DB signal output hold time (BCLK standard)		-7		ns
t <sub>SU(CAS-RAS)</sub>	CAS output setup time before RAS output (refresh)		(Note 1)		ns

## NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{h(RAS-RAD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [\text{ns}]$$

$$t_{RP} = \frac{10^9 \times 3}{f_{(BCLK)} \times 2} - 20 \quad [\text{ns}]$$

$$t_{SU(DB-CAS)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [\text{ns}]$$

$$t_{SU(CAS-RAS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [\text{ns}]$$

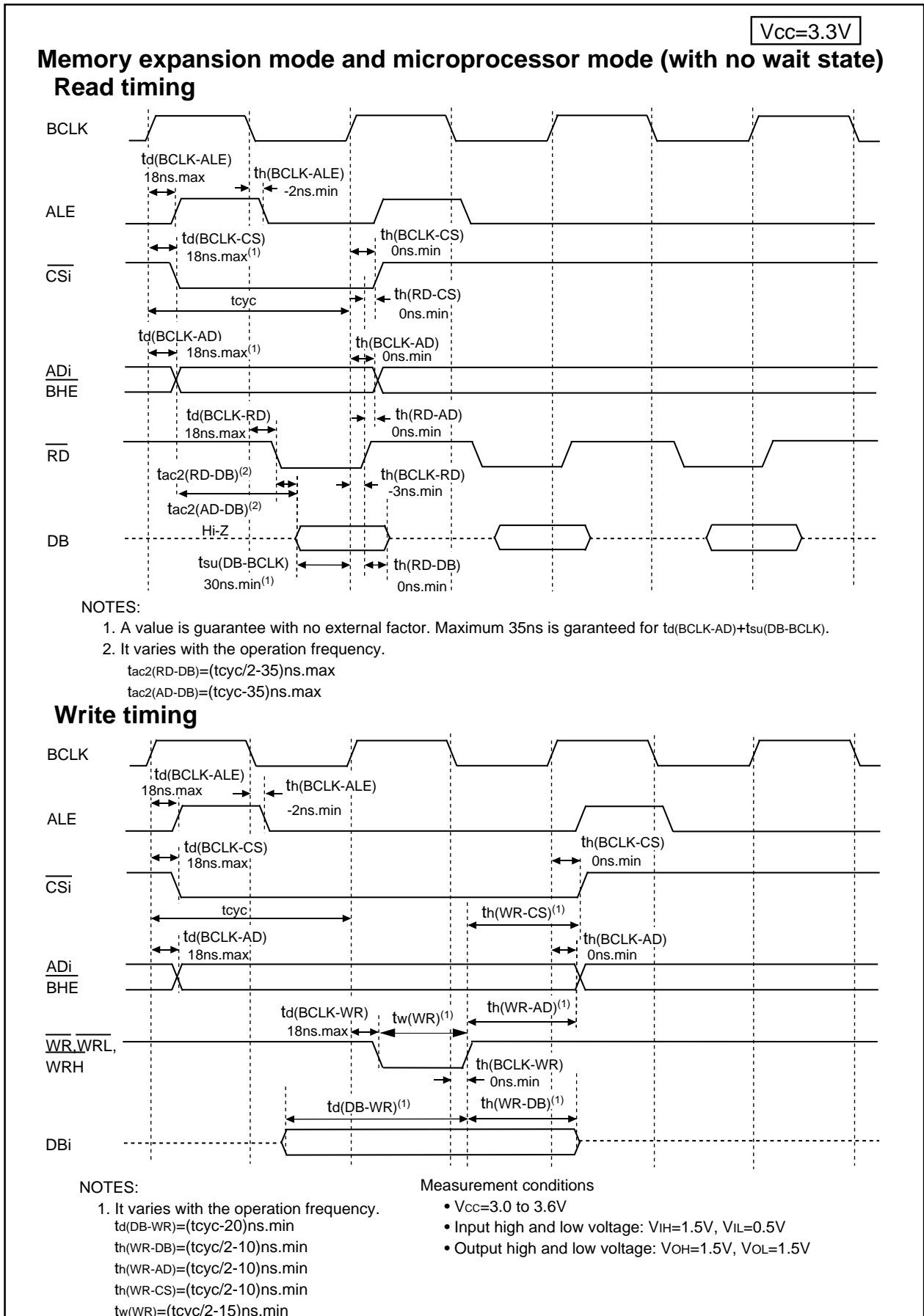


Figure 5.10 V<sub>CC</sub>=3.3V Timing Diagram (1)

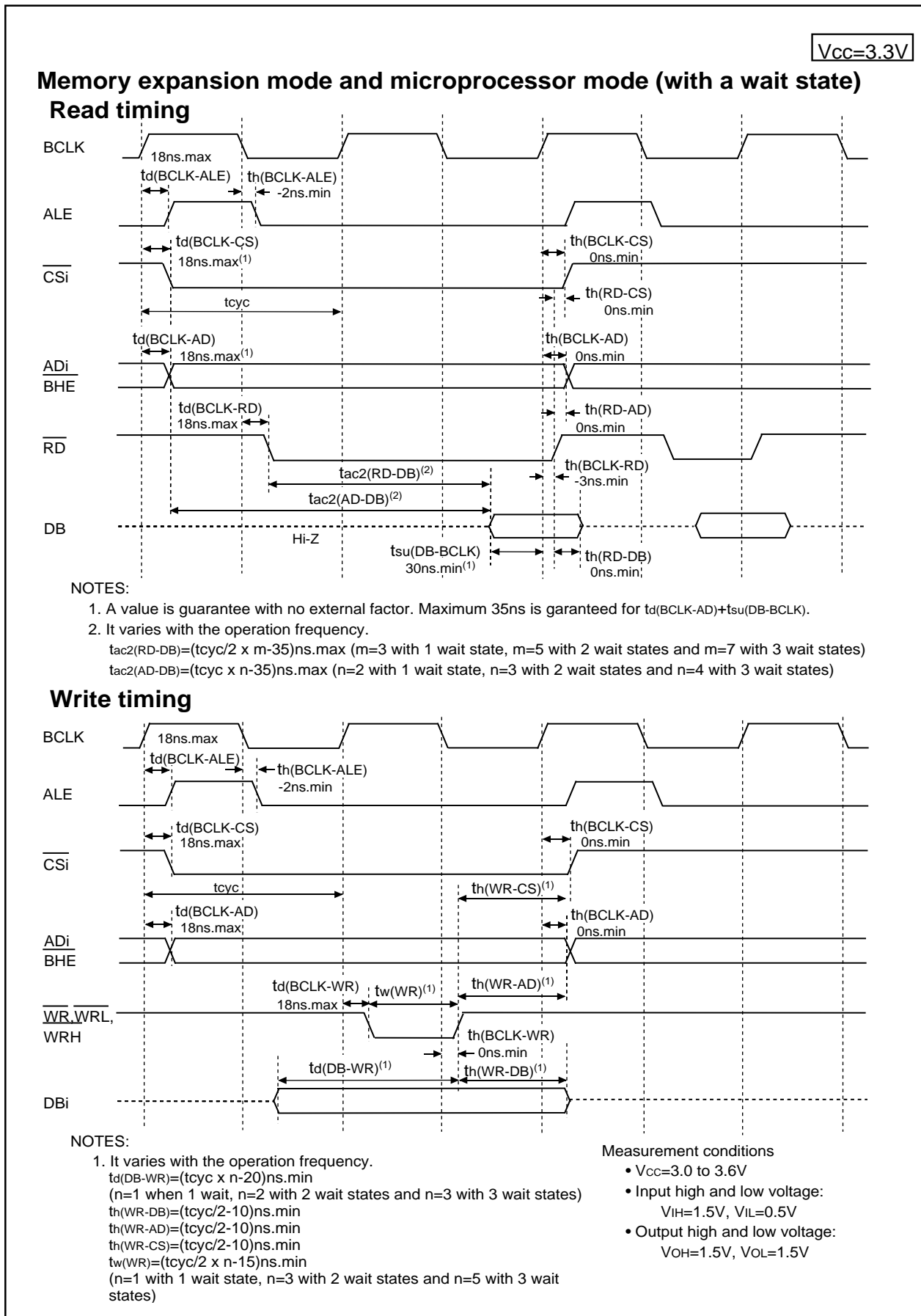


Figure 5.11 VCC=3.3V Timing Diagram (2)

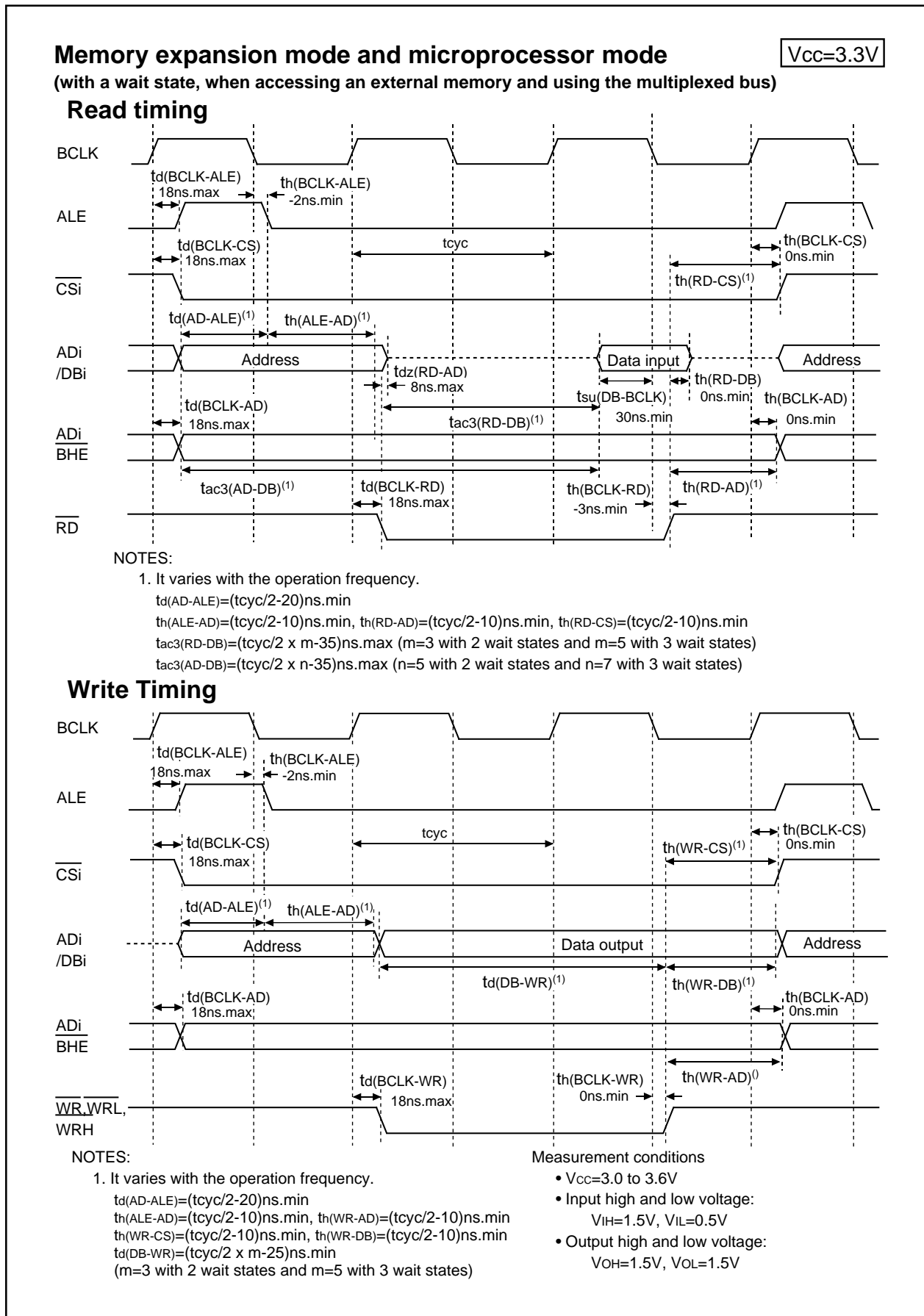
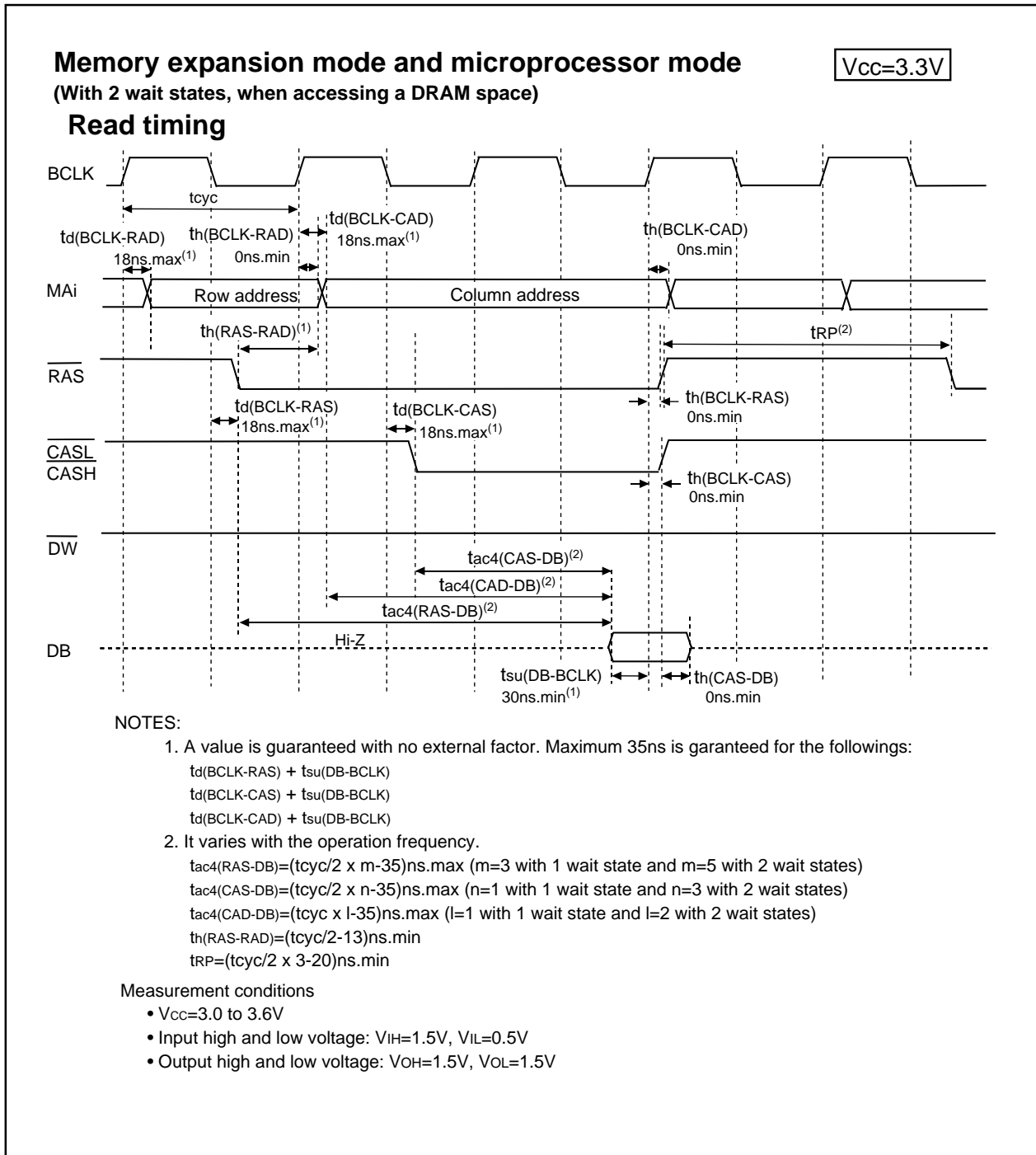


Figure 5.12 V<sub>CC</sub>=3.3V Timing Diagram (3)

Figure 5.13 V<sub>CC</sub>=3.3V Timing Diagram (4)

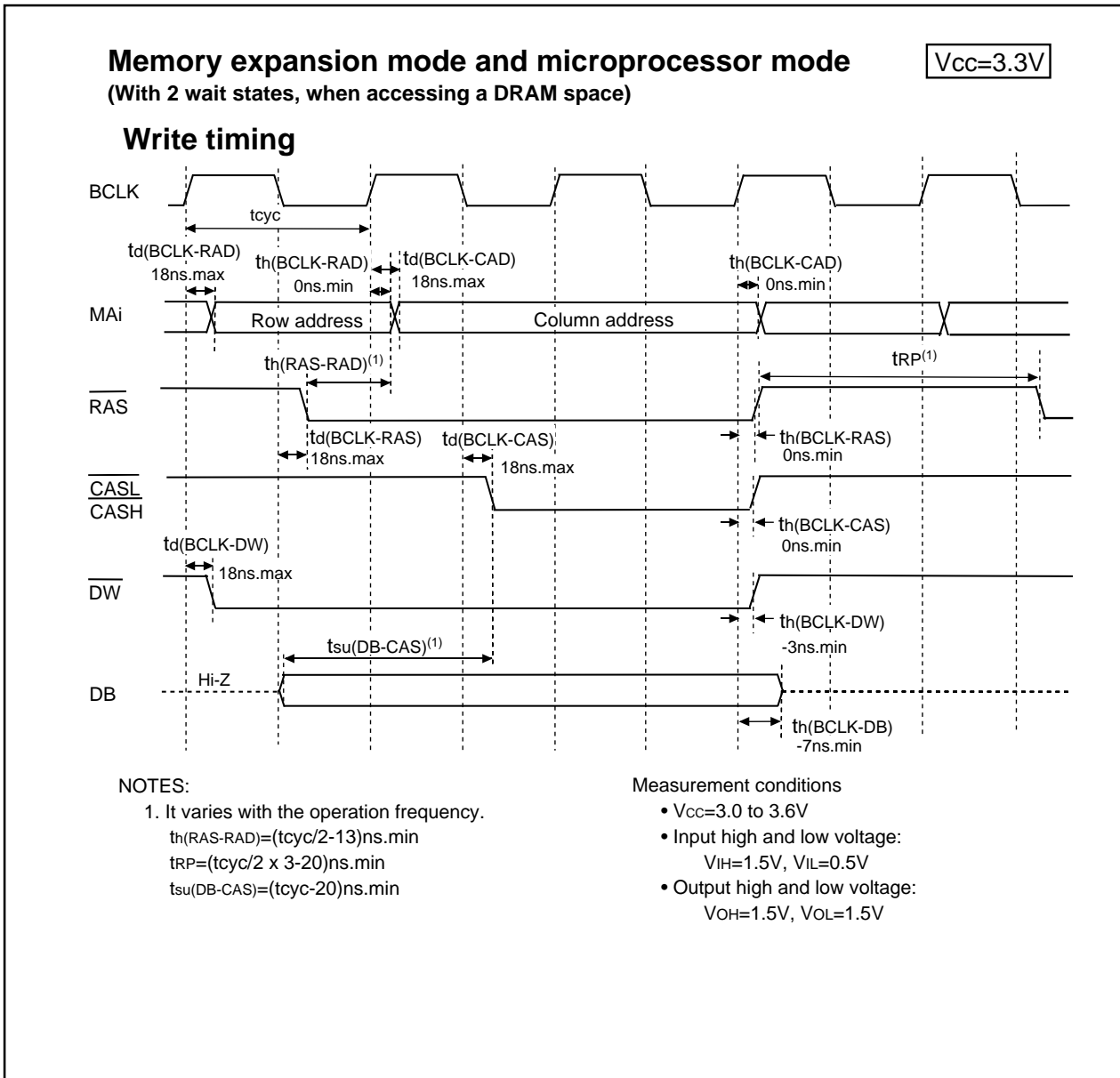


Figure 5.14 V<sub>CC</sub>=3.3V Timing Diagram (5)

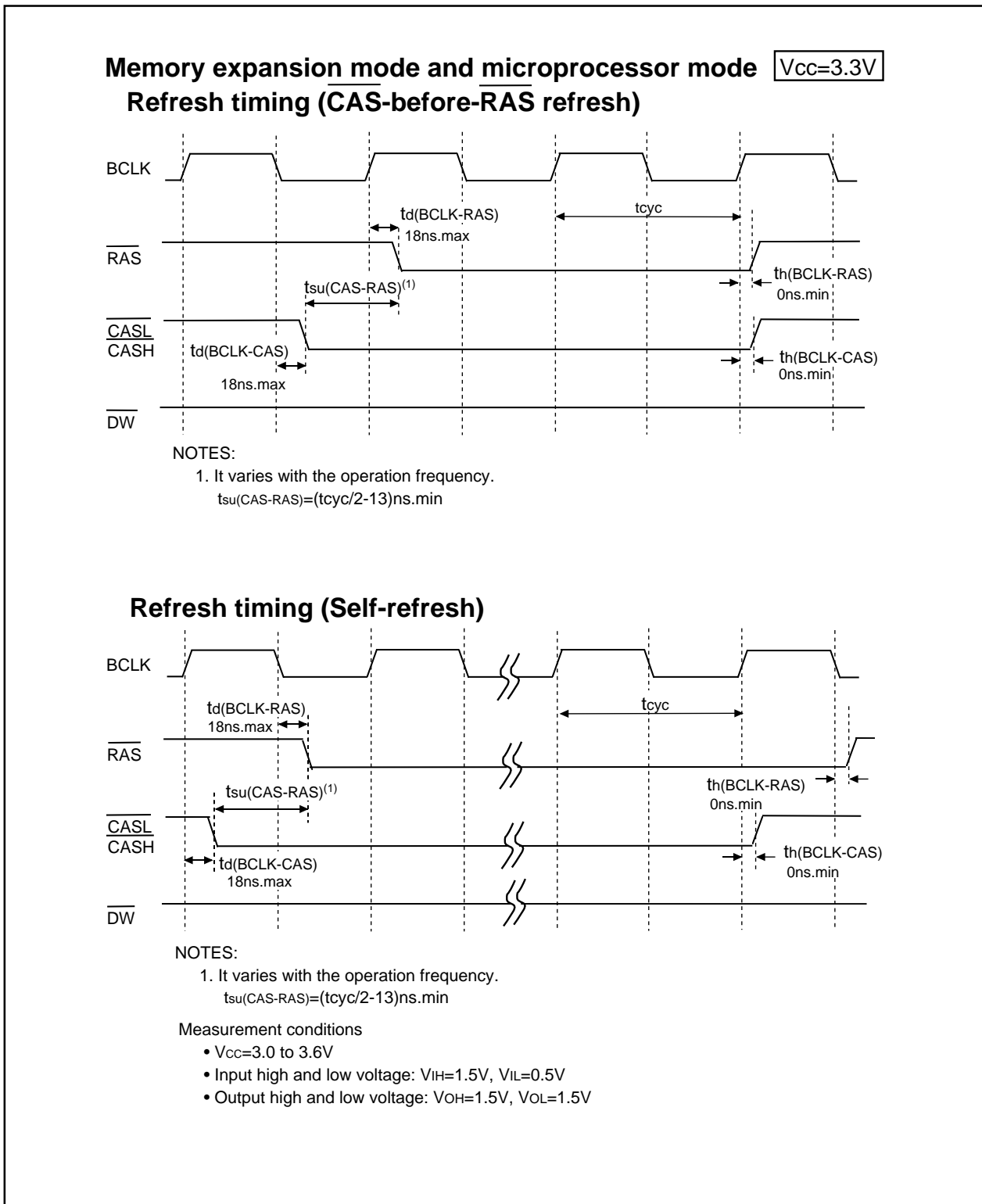


Figure 5.15 V<sub>CC</sub>=3.3V Timing Diagram (6)



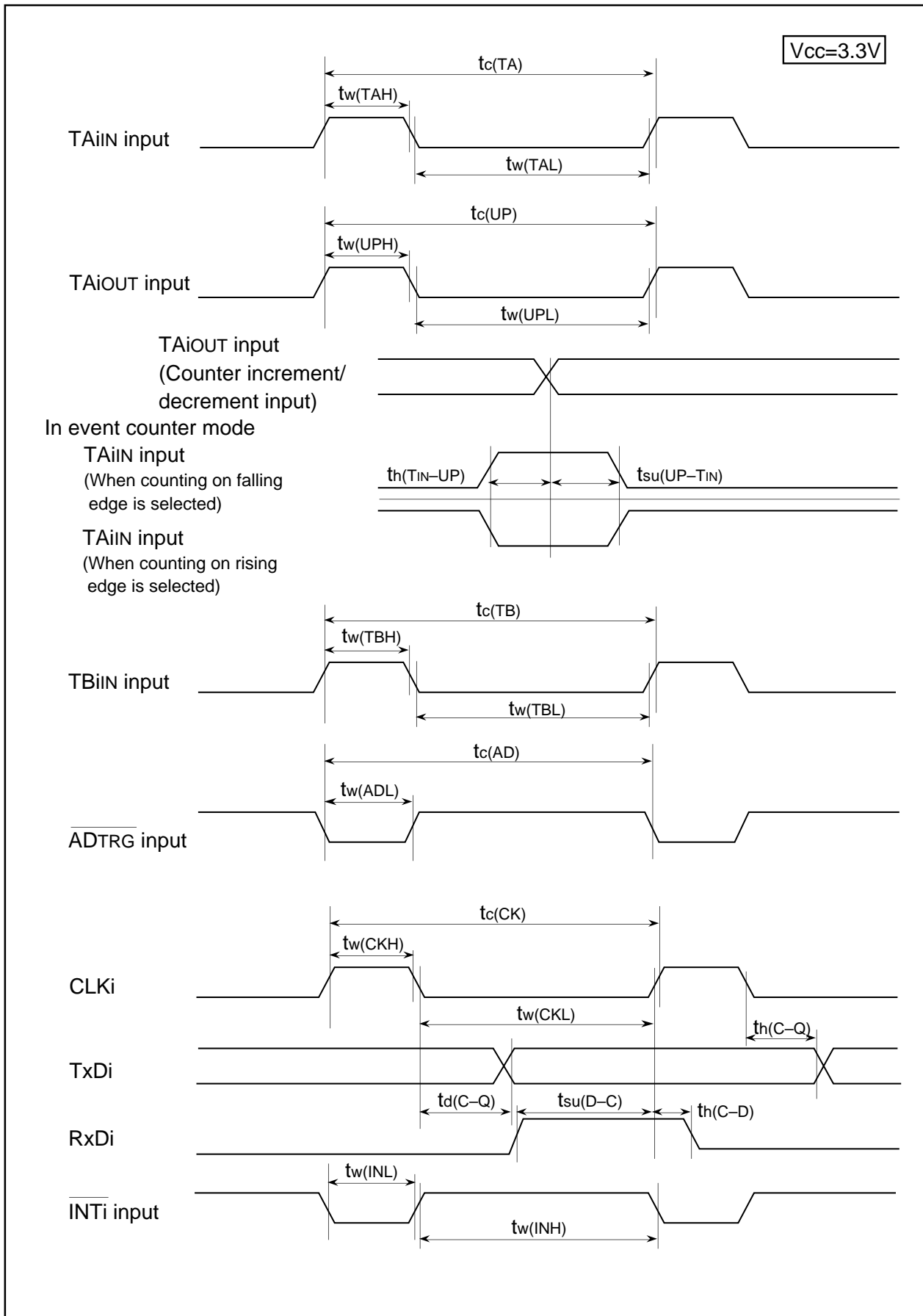


Figure 5.16 V<sub>CC</sub>=3.3V Timing Diagram (7)

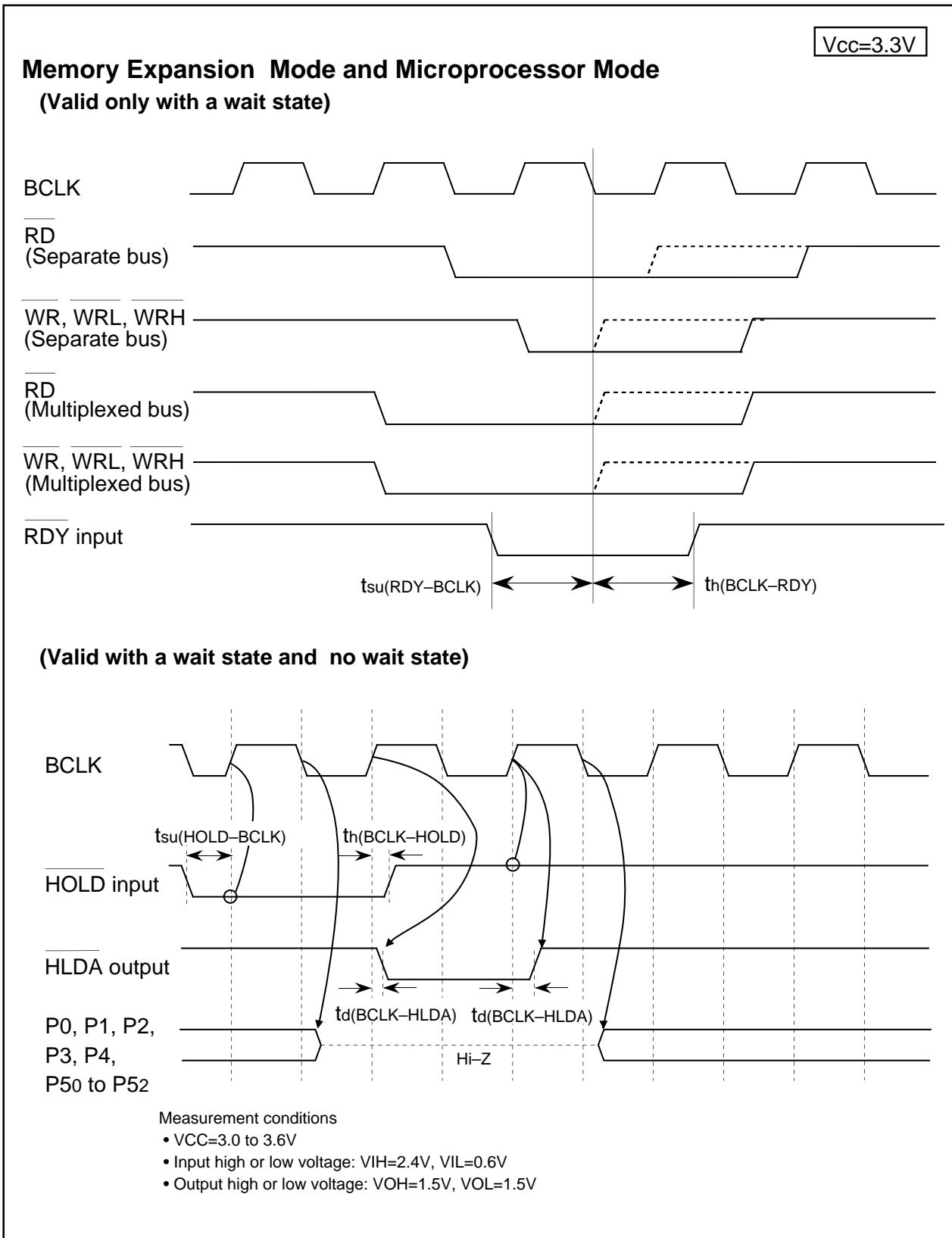


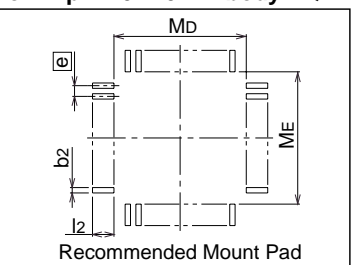
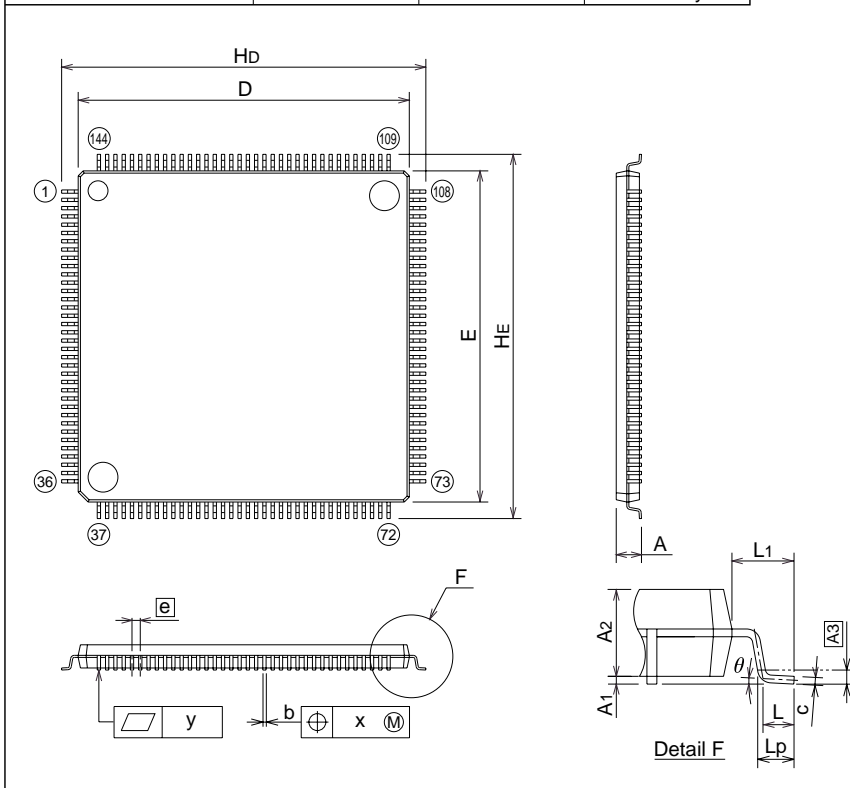
Figure 5.17 VCC=3.3V Timing Diagram (8)

# Package Dimensions

## 144P6Q-A Recommended

### Plastic 144pin 20X20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP144-P-2020-0.50	-	1.23	Cu Alloy

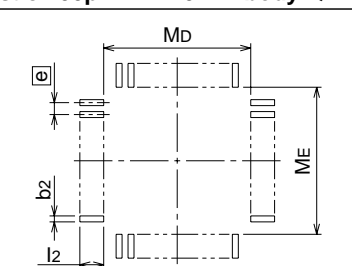
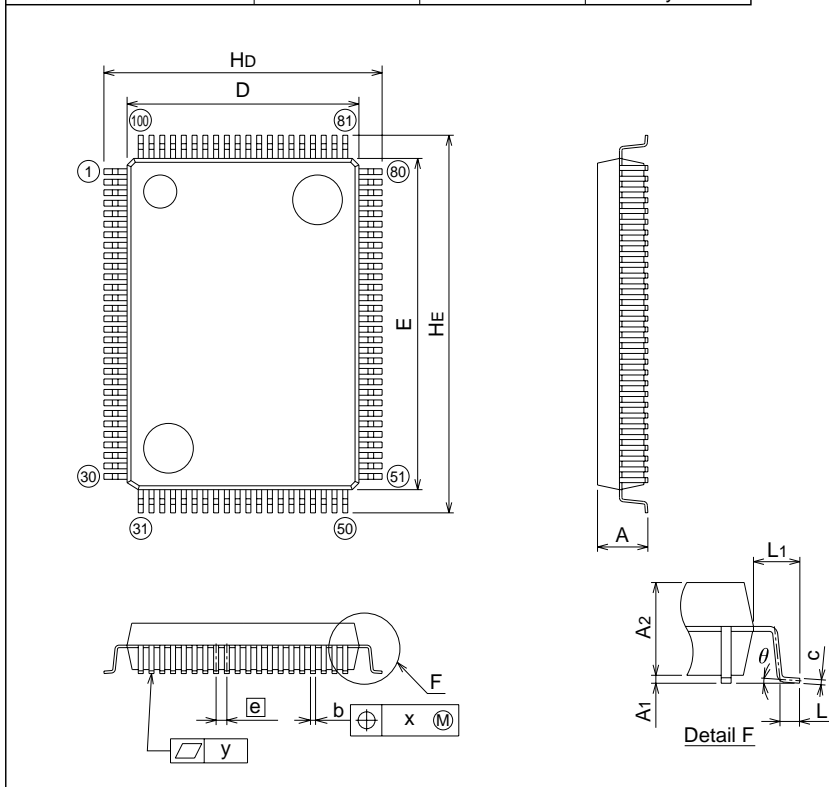


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0.05	0.125	0.2
A2	-	1.4	-
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	-	0.5	-
Hd	21.8	22.0	22.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	-	1.0	-
Lp	0.45	0.6	0.75
A3	-	0.25	-
x	-	-	0.08
y	-	-	0.1
theta	0°	-	8°
b2	-	0.225	-
l2	0.95	-	-
MD	-	20.4	-
ME	-	20.4	-

## 100P6S-A Recommended

### Plastic 100pin 14X20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	-	1.58	Alloy 42

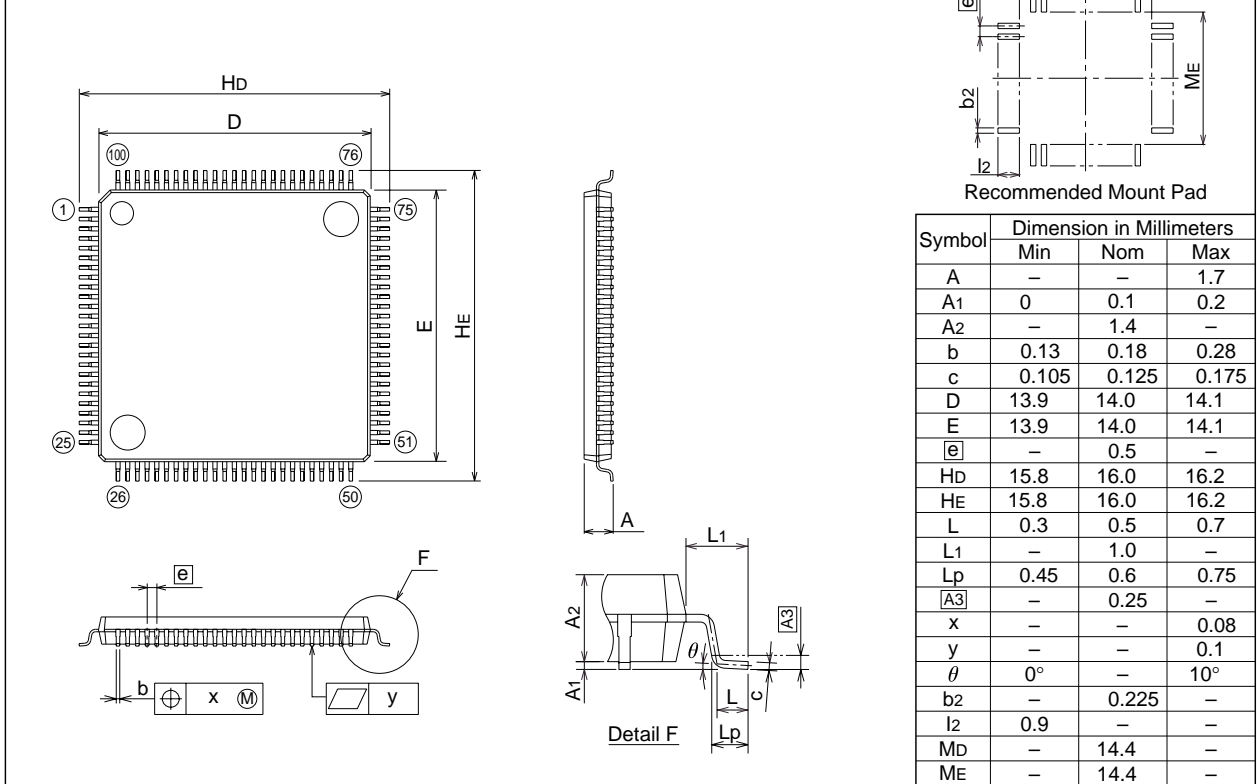


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	3.05
A1	0	0.1	0.2
A2	-	2.8	-
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	-	0.65	-
Hd	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	-	1.4	-
x	-	-	0.13
y	-	-	0.1
theta	0°	-	10°
b2	-	0.35	-
l2	1.3	-	-
MD	-	14.6	-
ME	-	20.6	-

**100P6Q-A** Recommended

**Plastic 100pin 14X14mm body LQFP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	-	0.63	Cu Alloy



REVISION HISTORY

M32C/83 Group Short Sheet/Data Sheet

Rev.	Date	Description	
		Page	Summary
1.10	Sep. 30,2003	-	New Document
1.20	Dec. 11,2003		Maximum operating frequency changed from 30 MHz to 32 MHz. Overview, Electrical Characteristics Table 1.1 M32C/83 Group Performance (144-Pin Package) Table 1.2 M32C/83 Group Performance (100-Pin Package) Table 5.2 Recommended Operating Conditions Table 5.3 Electrical Characteristics
1.30	Jun. 01, 2004	All pages	Words standardized: On-chip oscillator, A/D converter and D/A converter

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