

ON Semiconductor®

# **FDMC6683**

# P-Channel PowerTrench<sup>®</sup> MOSFET -20 V, -18 A, 8.3 m $\Omega$

#### **Features**

- Max  $r_{DS(on)} = 8.3 \text{ m}\Omega$  at  $V_{GS} = -4.5 \text{ V}$ ,  $I_D = -12 \text{ A}$
- Max  $r_{DS(on)}$  = 10 m $\Omega$  at  $V_{GS}$  = -2.5 V,  $I_D$  = -10 A
- Max  $r_{DS(on)}$  = 20 m $\Omega$  at  $V_{GS}$  = -1.8 V,  $I_D$  = -9.3 A
- High performance trench technology for extremely low r<sub>DS(on)</sub>
- High power and current handling capability in a widely used surface mount package
- 100% UIL Tested
- Termination is Lead-free and RoHS Compliant

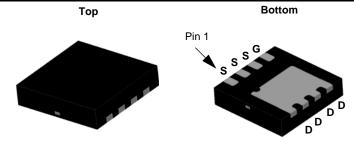
# **General Description**

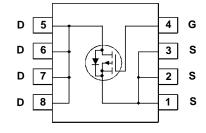
This P-Channel MOSFET is produced using ON Semiconductor's advanced Power Trench® process that has been optimized for  $r_{DS(ON)}$ , switching performance and ruggedness.

### **Applications**

- Battery Management
- Load Switch







MLP 3.3x3.3

### MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units	
V <sub>DS</sub>	Drain to Source Voltage			-20	V	
V <sub>GS</sub>	Gate to Source Voltage			±8	V	
	Drain Current -Continuous (Package limited)	T <sub>C</sub> = 25 °C		-18		
	-Continuous (Silicon limited)	T <sub>C</sub> = 25 °C		-54	^	
ID	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	-12	Α	
	-Pulsed			-50		
E <sub>AS</sub>	Single Pulse Avalanche Energy			37	mJ	
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25 °C		41	W	
	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	2.3	VV	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature R	ange		-55 to +150	°C	

#### **Thermal Characteristics**

$R_{ heta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1	a) 53	C/VV

## **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC6683	FDMC6683	MLP 3.3X3.3	13 "	12 mm	3000 units

# **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

Symbol	Parameter Test Conditions		Min	Тур	Max	Units
Off Chara	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, referenced to 25 °C		-12		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V			-1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

#### **On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-0.4	-0.5	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, referenced to 25 °C		3		mV/°C
	Static Drain to Source On Resistance	$V_{GS} = -4.5 \text{ V}, I_D = -12 \text{ A}$		6.2	8.3	- mΩ
_		$V_{GS} = -2.5 \text{ V}, I_D = -10 \text{ A}$		7.3	10	
r <sub>DS(on)</sub>		$V_{GS} = -1.8 \text{ V}, I_D = -9.3 \text{ A}$		8.9	20	
		$V_{GS} = -4.5 \text{ V}, I_D = -12 \text{ A}, T_J = 125 \text{ °C}$		8.5	11.4	1
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_{D} = -12 \text{ A}$		75		S

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	5890	7835	pF
C <sub>oss</sub>	Output Capacitance		819	1090	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		729	1095	pF

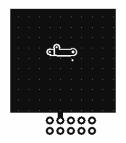
### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time				15	27	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = -10 V, I <sub>D</sub> = -12	$V_{DD}$ = -10 V, $I_{D}$ = -12 A, $V_{GS}$ = -4.5 V, $R_{GEN}$ = 6 $\Omega$		34	55	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = -4.5 V, R <sub>GEN</sub>			315	504	ns
t <sub>f</sub>	Fall Time				158	253	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to -4.5 V}$			81	114	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to -2.5 V}$	$V_{DD} = -10 \text{ V},$		49	69	nC
$Q_{gs}$	Gate to Source Charge		I <sub>D</sub> = -12 A		6.3		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge				19.9		nC

#### **Drain-Source Diode Characteristics**

V <sub>SD</sub> Source to Drain Diode Forward	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = -12 \text{ A}$ (Note 2)	0.7	0 1.3	V
	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -2 \text{ A}$ (Note 2)	0.5	4 1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = -12 A, di/dt = 100 A/μs	32	52	ns
Q <sub>rr</sub>	Reverse Recovery Charge	1F = -12 A, αι/αι = 100 A/μs	17	31	nC

<sup>&</sup>lt;sup>13</sup> R<sub>0,JA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0,JC</sub> is guaranteed by design while R<sub>0,JA</sub> is determined by the user's board design.



a) 53 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) 125 °C/W when mounted on a minimum pad of 2 oz copper

- 2: Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%. 3: Starting T $_J$  = 25  $^{\circ}$ C; P-Ch: L = 3 mH, I $_A$ S = -5 A, V $_D$ D = -20 V, V $_G$ S = -4.5 V.

# Typical Characteristics $T_J = 25$ °C unless otherwise noted

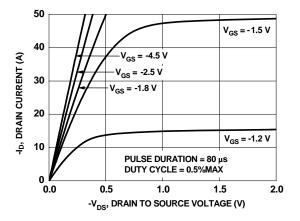


Figure 1. On Region Characteristics

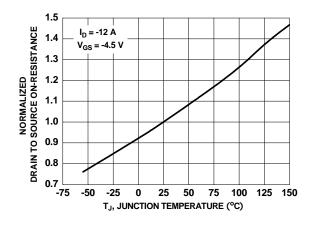


Figure 3. Normalized On Resistance vs. Junction Temperature

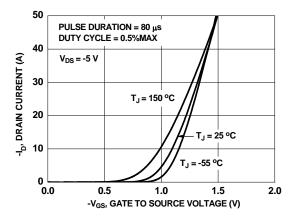


Figure 5. Transfer Characteristics

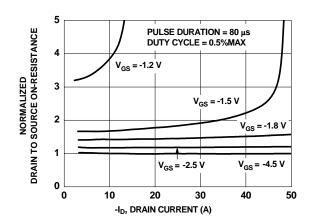


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

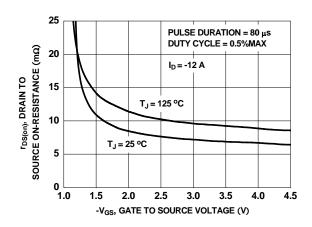


Figure 4. On-Resistance vs. Gate to Source Voltage

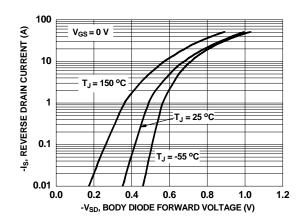


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

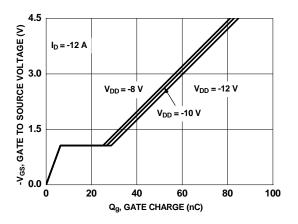


Figure 7. Gate Charge Characteristics

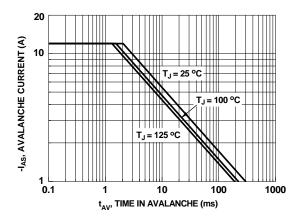


Figure 9. Unclamped Inductive Switching Capability

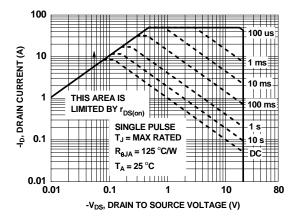


Figure 11. Forward Bias Safe Operating Area

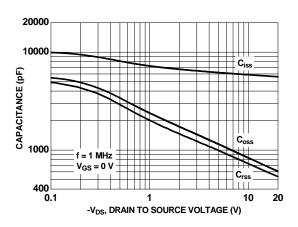


Figure 8. Capacitance vs. Drain to Source Voltage

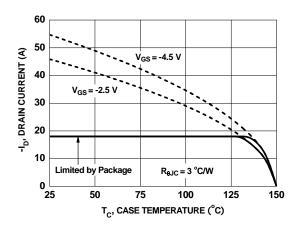


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

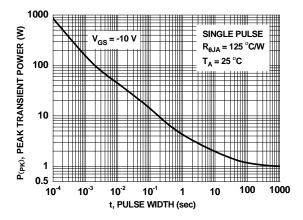


Figure 12. Single Pulse Maximum Power Dissipation



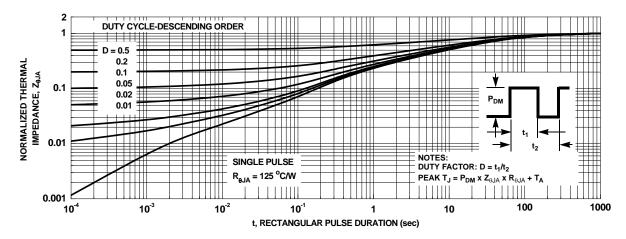
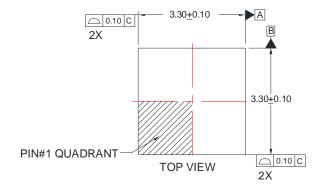
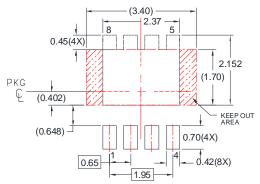
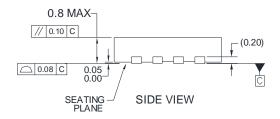


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

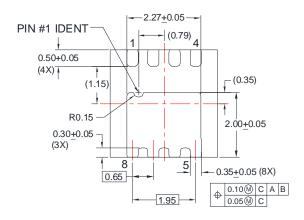
# **Dimensional Outline and Pad Layout**











**BOTTOM VIEW** 

#### NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY
- E. DRAWING FILE NAME : MKT-MLP08Srev2
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