

National Semiconductor is now part of
Texas Instruments.

Search <http://www.ti.com/> for the latest technical
information and details on our current products and services.

LP8720

One Step-Down DC/DC and Five Linear Regulators with I2C Compatible Interface

General Description

The LP8720 is a multi-function, programmable Power Management Unit, optimized for sub block power requirement solution. This device integrates one highly efficient 400 mA step-down DC/DC converter with Dynamic Voltage Scale (DVS), five low noise low dropout (LDO) voltage regulators and a 400 KHz I²C-compatible interface to allow a host controller access to the internal control registers of the LP8720. The LP8720 additionally features programmable power-on sequencing.

LDO regulators provide high PSRR and low noise ideally suited for supplying power to both analog and digital loads. The package will be the smallest 2.5 mm x 2.0 mm micro SMD 20-bump package.

Applications

- Cellular Handsets
- Portable hand-held products

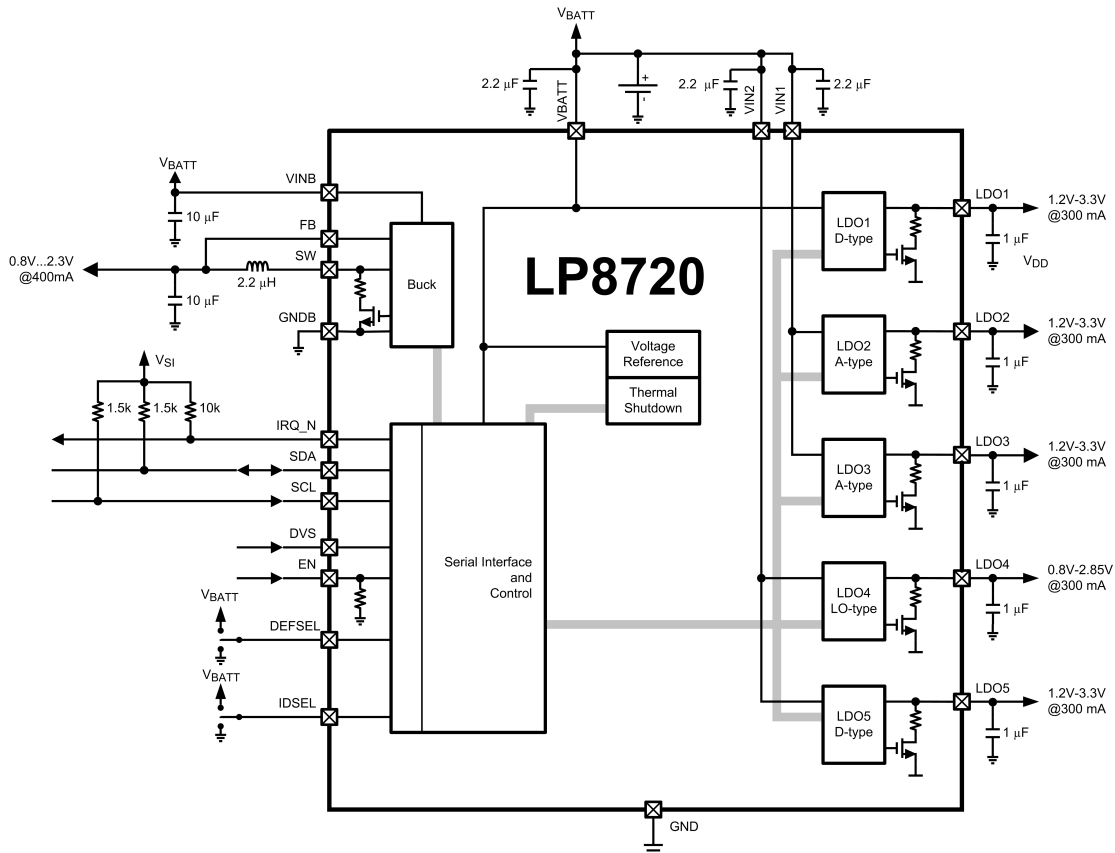
Features

- 5 Low Noise LDO's for up to 300 mA
- One high-efficiency Synchronous Magnetic Buck Regulator, I_{OUT} 400 mA
 - High efficiency PFM mode @ low I_{OUT}
 - Auto Mode PFM/PWM switch
 - Low inductance 2.2 μH @ 2 MHz clock
 - Dynamic Voltage Scale control
- I²C-compatible interface for the controlling of internal registers
- 20-bump 2.5 x 2.0 mm micro SMD package

Key Specifications

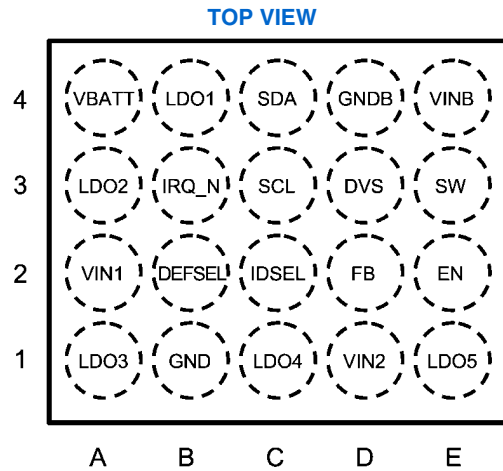
- Programmable V_{out} from 0.8V to 2.3V on DC/DC
- Automatic soft start on DC/DC
- 200 mV typ Dropout Voltage at 300 mA on LDO's
- 2% (typ) Output Voltage accuracy on LDO's

Typical Application Diagram



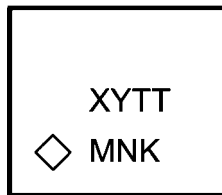
30067501

Device Pin Diagram (Micro SMD 20)



30067502

Package Marking Information



XY = 2 Digit Date Code
 TT = Die Traceability
 NMK = Product Identification
 ◇ = Pin 1A

30067503

Ordering Information

Order Number	Package Type	Product Identification	Supplied as
LP8720TLE	micro SMD	8720	250 Tape & Reel
LP8720TLX	micro SMD	8720	3000 Tape & Reel

Upon request there will be available custom versions – customer can order own default voltages and own startup sequence. For more information please contact local National Semiconductor Corp. sales office.

LP8720 Pin Descriptions

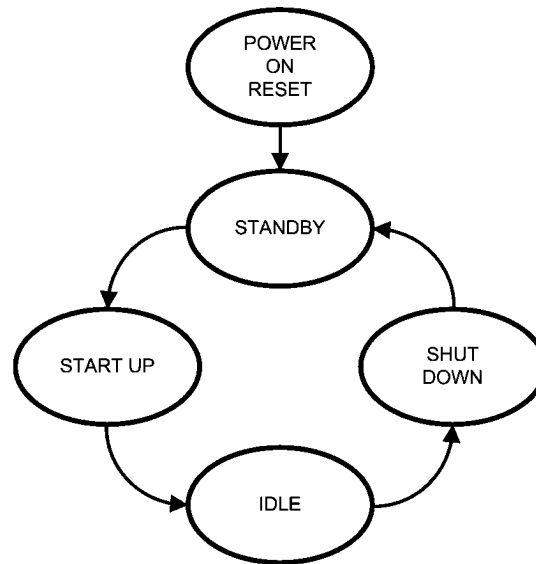
Pin Number	Name	Type	Description
A4	VBATT	P	Battery Input for LDO1 and all internal circuitry.
E4	VINB	P	Battery Input for Buck.
A2	VIN1	P	Battery Input for LDO2 and LDO3.
D1	VIN2	P	Battery Input for LDO4 and LDO5.
B4	LDO1	A	LDO1 Output.
A3	LDO2	A	LDO2 Output.
A1	LDO3	A	LDO3 Output.
C1	LDO4	A	LDO4 Output.
E1	LDO5	A	LDO5 Output.
E3	SW	A	Buck Output.
D2	FB	A	Buck Feedback.
D4	GNDB	G	Power Ground for Buck.
B1	GND	G	IC Ground.
C4	SDA	DI/O	I ² C-compatible Serial Interface Data Input/Output. Open Drain output, external pull up resistor is needed, typ 1.5 k Ω . If not in use then hard wire to GND.
C3	SCL	DI	I ² C-compatible Serial Interface Clock input. External pull up resistor is needed, typ 1.5 k Ω . If not in use then hard wire to GND.
B3	IRQ_N	DO	Interrupt output, active LOW. Open Drain output, external pull up resistor is needed, typ 10 k Ω . If not in use then hard wire to GND or leave floating.
E2	EN	DI	Enable. EN=LO standby. EN=HI power on. Internal pull down resistor 500 k Ω . If not in use then hard wire to VBATT.
B2	DEFSEL	DI	Control input that sets the default voltages and startup sequence. Must be hard wired to BATT or GND or left floating (Hi-Z) for specific application. When DEFSEL= VBATT then setup 1 is used for default voltages and startup sequence. When DEFSEL= GND then setup 2 is used for default voltages and startup sequence. When DEFSEL= floating (Hi-Z) setup 3 is used for default voltages and startup sequence.
C2	IDSEL	DI	Control input that sets the slave address for serial interface. Must be hard wired to BATT or GND or left floating (Hi-Z) for specific application. When IDSEL= VBATT then slave address is 7h'7F When IDSEL= floating (Hi-Z) then slave address is 7h'7C When IDSEL= GND then slave address is 7h'7D
D3	DVS	DI	Dynamical Voltage Scaling. When DVS=HI then Buck voltage set BUCK_V1 is in use. When DVS=LO then Buck voltage set BUCK_V2 is in use. Buck voltage set BUCK_V1 should be higher than Buck voltage set BUCK_V2. If not in use then hard wire to VBATT or GND.

A:	Analog Pin
D	Digital Pin
I	Input Pin
DI/O	Digital Input/Output Pin
G	Ground
O	Output Pin
P	Power Connection

Device Description

OPERATION MODES

- POWER-ON-RESET:** After VBATT gets above POR higher threshold DEFSEL-pin and IDSEL-pin are read. Then all internal registers of LP8720 are reset to the default values and after that LP8720 goes to STANDBY mode. This process duration max is 500 μ s.
- STANDBY:** In STANDBY mode only serial interface is working and all other PMU functions are disabled – PMU is in low power condition. In STANDBY mode LP8720 can be (re)configured via Serial Interface.
- START UP:** START UP sequence is defined by registers contents. START UP sequence starts:
- 1) If rising edge on EN-pin.
 - 2) After cooling down from thermal shutdown event if EN=HI.
- It is not recommended to write to LP8720 registers during START UP. If doing so then current START UP sequence may become undefined.
- IDLE:** PMU will enter into IDLE mode (normal operating mode) after end of START UP sequence. In IDLE mode all LDO's and BUCK can be enabled/disabled via Serial Interface. Also in IDLE mode LP8720 can be (re) configured via Serial Interface.
- SHUT DOWN:** SHUT DOWN sequence is "reverse order of start up sequence" and this is defined by registers contents. SHUT DOWN starts
- 1) If falling edge on EN-pin.
 - 2) If temperature exceeds thermal shutdown threshold TSD +160°C.
- It is not recommended to write to LP8720 registers during SHUT DOWN. If doing so then current SHUT DOWN sequence may become undefined.



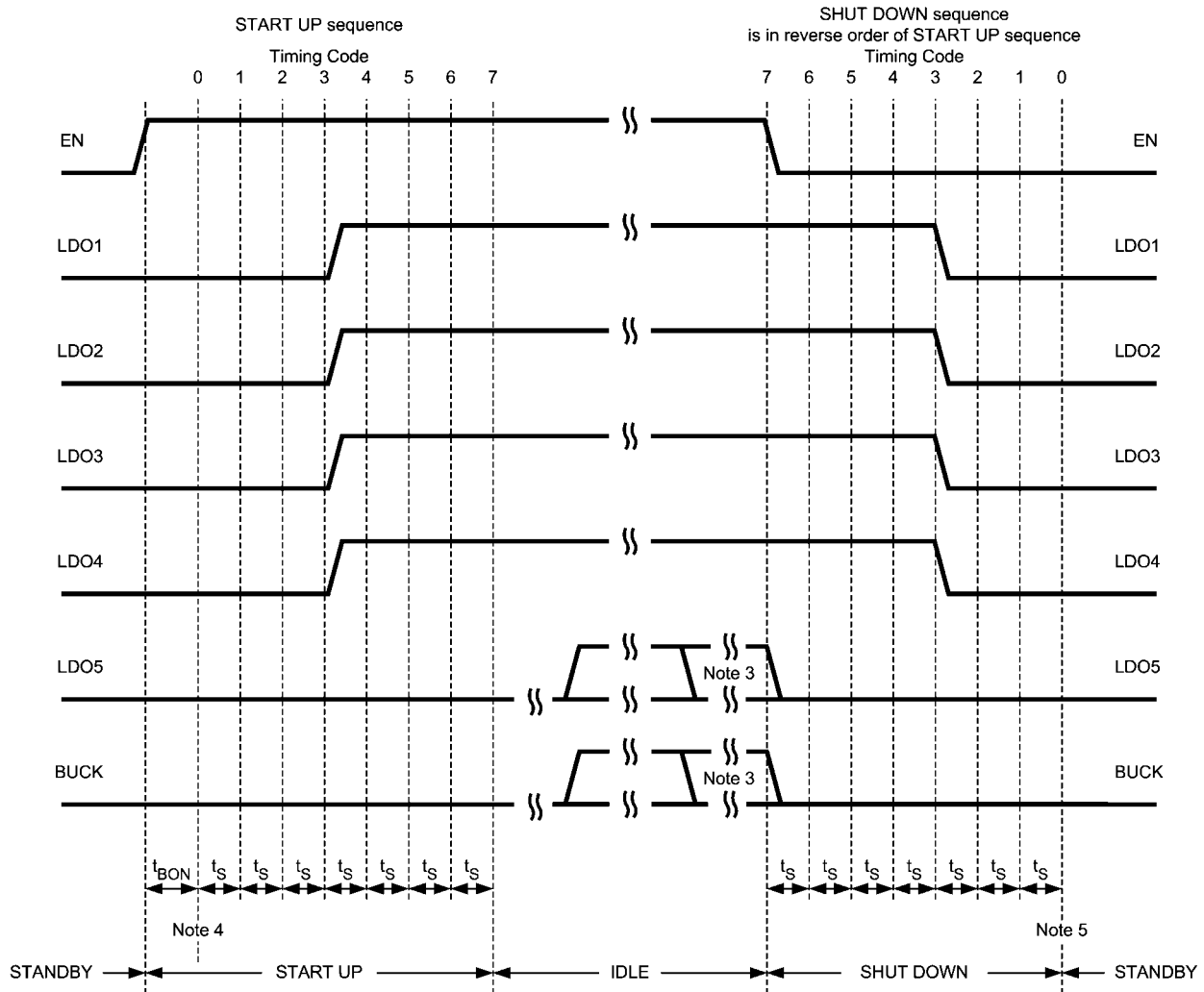
30067504

Additional Functions

- SLEEP:** If sum of all LDO's load currents and BUCK load current is no higher than 5mA then user can put PMU to SLEEP. In SLEEP PMU GND current is minimized. In SLEEP LDO's and BUCK cannot be loaded with big current. There are 2 possibilities to use SLEEP:
- 1) Control via Serial Interface.
 - 2) Control by DVS-pin.
- DVS:** Dynamic Voltage Scaling allows using 2 voltage sets for BUCK. There are 2 possibilities to use DVS:
- 1) Control via Serial Interface.
 - 2) Control by DVS-pin.
- INTERRUPT:** If interrupt is not masked then PMU forces IRQ_N low if temperature crossed TSD_EW limit (thermal shutdown early warning) or/and thermal shutdown event took place. IRQ_N is released by reading Interrupt register.

POWER-ON AND POWER-OFF SEQUENCES

Start Up Sequence if DEFSEL=VBATT or DEFSEL=Hi-Z



30067505

t_{BON} 150 μ s – Reference and bias turn ON. Min 100 μ s max 200 μ s.

t_s 25 μ s – time step. Time step accuracy is defined by OSC frequency accuracy.

Note 1 START UP and SHUT DOWN sequences are defined by registers. Sequences given here are valid if there the registers are not rewritten via Serial Interface.

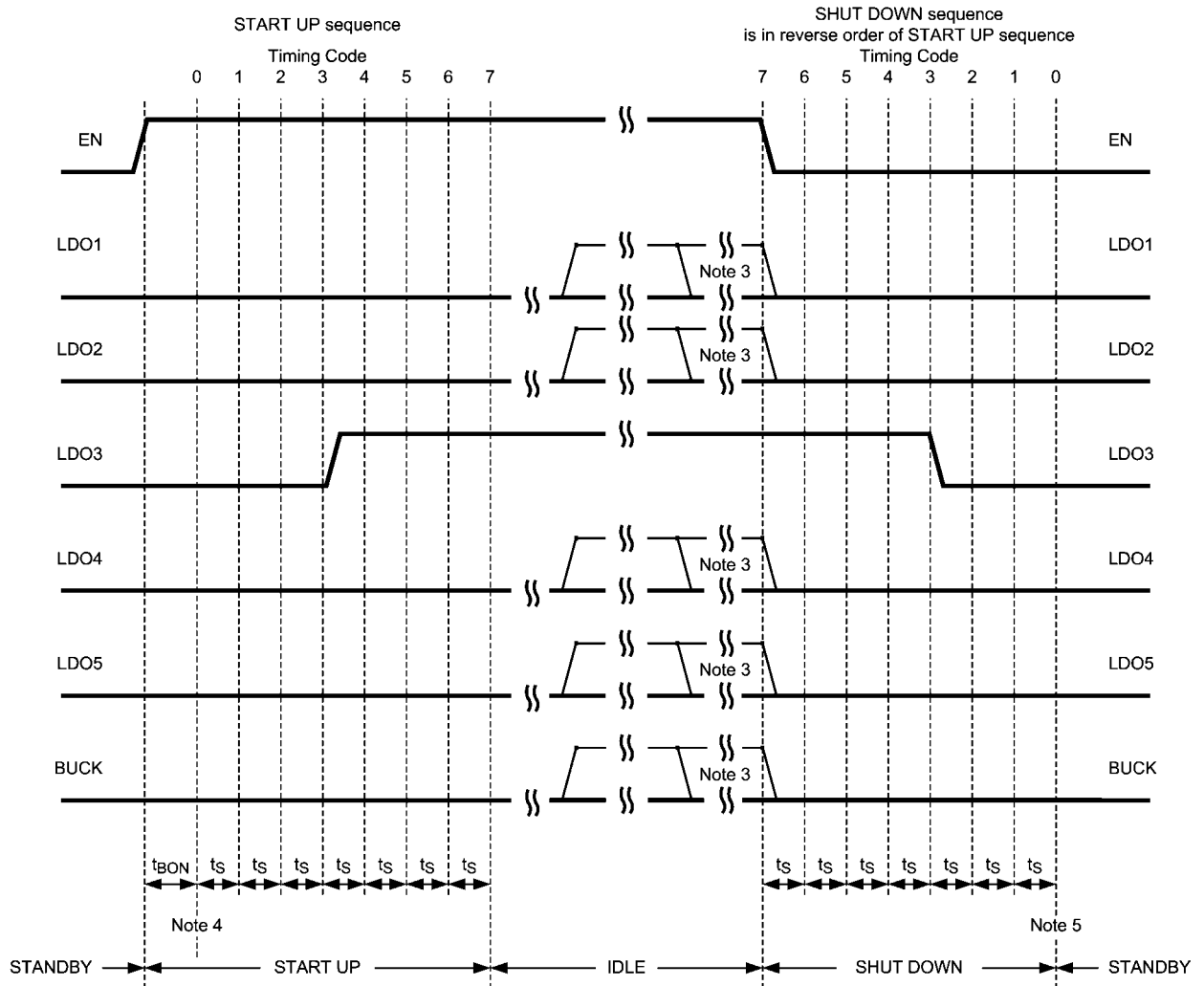
Note 2 The timing showed here define time points when LDO's and BUCK are enabled/disabled. Enabling /disabling process duration depends on loading conditions. Buck startup duration is 140 μ s for no load. LDO startup duration is no more than 35 μ s. For details please see LDO's and BUCK electrical specifications.

Note 3 LDO5 and BUCK are disabled. If LDO5 and/or BUCK are enabled via Serial Interface and startup sequence is not changed via Serial interface, then LDO5 and BUCK are disabled with no delay from falling edge on EN-pin.

Note 4 At this time point registers 0x09 and 0x0C are reset to POR default values.

Note 5 At this time point registers 0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07 and 0x08 are reset to POR default values.

Start Up Sequence if DEFSEL=GND



30067506

t_{BON} 150 μ s – Reference and bias turn ON. Min 100 μ s max 200 μ s.

t_s 25 μ s – time step. Time step accuracy is defined by OSC frequency accuracy.

Note 1 START UP and SHUT DOWN sequences are defined by registers. Sequences given here are valid if there the registers are not rewritten via Serial Interface.

Note 2 The timing showed here define time points when LDO's and BUCK are enabled/disabled. Enabling /disabling process duration depends on loading conditions. Buck startup duration is 140 μ s for no load. LDO startup duration is no more than 35 μ s. For details please see LDO's and BUCK electrical specifications.

Note 3 LDO1, LDO2, LDO4, LDO5 and BUCK are disabled. If LDO1, LDO2, LDO4, LDO5 and/or BUCK are enabled via Serial Interface and startup sequence is not changed via Serial interface, then LDO1, LDO2, LDO4, LDO5 and BUCK are disabled with no delay from falling edge on EN-pin.

Note 4 At this time point registers 0x09 and 0x0C are reset to POR default values.

Note 5 At this time point registers 0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07 and 0x08 are reset to POR default values.

Start Up Sequence

DEFSEL	Start Up Sequence	Shut Down Sequence
VBATT	LDO1, 2, 3, 4 enable same time. LDO5 and BUCK enable via Serial Interface.	In reverse order of start up sequence.
GND	LDO3 enable. LDO1, 2, 4, 5 and BUCK enable via Serial Interface .	In reverse order of start up sequence.
Hi-Z	LDO1, 2, 3, 4 enable same time. LDO5 and BUCK enable via Serial Interface.	In reverse order of start up sequence.

Default Output Voltages

Output	Max Current [mA]	Default output Voltage [V] and default ON/OFF if EN=HI		
		DEFSEL=VBATT	DEFSEL=GND	DEFSEL=Hi-Z
LDO1	300	3.0 ON	3.0 OFF	2.8 ON
LDO2	300	2.6 ON	3.0 OFF	2.6 ON
LDO3	300	1.8 ON	2.6 ON	1.8 ON
LDO4	300	1.0 ON	2.6 OFF	1.2 ON
LDO5	300	3.3 OFF	3.3 OFF	3.3 OFF
BUCK	400	1.0 OFF	1.2/1.3 ¹⁾ OFF	1.2 OFF

Note 1) BUCK voltage is 1.2V if DVS=LO and 1.3V if DVS=HI.

Control Register Map

When IDSEL= VBATT then slave address is 7h7F
 When IDSEL= floating (Hi-Z) then slave address is 7h7C
 When IDSEL= GND then slave address is 7h7D

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR default		
										VBATT	GND	Hi-Z
0x00	GENERAL_SETTINGS						EXT_DVS_CONTROL	EXT_SLEEP_CONTROL	SHORT_TIMESTEP	0000 0001	0000 0101	0000 0001
0x01	LDO1_SETTINGS	LDO1_T[2]	LDO1_T[1]	LDO1_T[0]	LDO1_V[4]	LDO1_V[3]	LDO1_V[2]	LDO1_V[1]	LDO1_V[0]	0111 1101	1111 1101	0111 1001
0x02	LDO2_SETTINGS	LDO2_T[2]	LDO2_T[1]	LDO2_T[0]	LDO2_V[4]	LDO2_V[3]	LDO2_V[2]	LDO2_V[1]	LDO2_V[0]	0111 0101	1111 1101	0111 0101
0x03	LDO3_SETTINGS	LDO3_T[2]	LDO3_T[1]	LDO3_T[0]	LDO3_V[4]	LDO3_V[3]	LDO3_V[2]	LDO3_V[1]	LDO3_V[0]	0110 1100	0111 0101	0110 1100
0x04	LDO4_SETTINGS	LDO4_T[2]	LDO4_T[1]	LDO4_T[0]	LDO4_V[4]	LDO4_V[3]	LDO4_V[2]	LDO4_V[1]	LDO4_V[0]	0110 0011	1111 1010	0110 0101
0x05	LDO5_SETTINGS	LDO5_T[2]	LDO5_T[1]	LDO5_T[0]	LDO5_V[4]	LDO5_V[3]	LDO5_V[2]	LDO5_V[1]	LDO5_V[0]	1111 1111	1111 1111	1111 1111
0x06	BUCK_SETTINGS1	BUCK_T[2]	BUCK_T[1]	BUCK_T[0]	BUCK_V1[4]	BUCK_V1[3]	BUCK_V1[2]	BUCK_V1[1]	BUCK_V1[0]	1110 0101	1110 1011	1110 1001
0x07	BUCK_SETTINGS2			FORCE_PWM	BUCK_V2[4]	BUCK_V2[3]	BUCK_V2[2]	BUCK_V2[1]	BUCK_V2[0]	0000 0101	0000 1001	0000 1001
0x08	ENABLE_BITS	DVS_V2/V1	SLEEP_MODE	BUCK_EN	LDO5_EN	LDO4_EN	LDO3_EN	LDO2_EN	LDO1_EN	1000 1111	1000 0100	1000 1111
0x09	PULLDOWN_BITS	APU_TSD		BUCK_PULLDOWN	LDO5_PULLDOWN	LDO4_PULLDOWN	LDO3_PULLDOWN	LDO2_PULLDOWN	LDO1_PULLDOWN	0011 1111	0011 1111	0011 1111
0x0A	STATUS_BITS							TSD	TSD_EW	0000 0000	0000 0000	0000 0000
0x0B	INTERRUPT_BITS *)							TSD_INT	TSD_EW_INT	0000 0000	0000 0000	0000 0000
0x0C	INTERRUPT_MASK *)							TSD_MASK	TSD_EW_MASK	0000 0011	0000 0011	0000 0011

*) Registers STATUS_BITS 0x0A and INTERRUPT_BITS 0x0B are read only.

Register 0x00

EXT_DVS_CONTROL	<p>1 – DVS-pin control: DVS=HI then BUCK_V1[4:0] DVS=LO then BUCK_V2[4:0]</p> <p>0 – Serial interface control: DVS_V2/V1=1 then BUCK_V1[4:0] DVS_V2/V1=0 then BUCK_V2[4:0]</p>
EXT_SLEEP_CONTROL	<p>1 – DVS-pin control: DVS=HI then normal DVS=LO then SLEEP</p> <p>0 – Serial interface control: SLEEP_MODE=0 then normal SLEEP_MODE=1 then SLEEP</p>
SHORT_TIMESTEP	<p>1 – time step $t_S=25\ \mu\text{s}$</p> <p>0 – time step $t_S=50\ \mu\text{s}$</p> <p>By request time step $100\ \mu\text{s}/200\ \mu\text{s}$ is available.</p>

Registers 0x01 – 0x07

LDO1_V[4:0]	00000 – 1.20V	01000 – 1.60V	10000 – 2.10V	11000 – 2.75V
LDO2_V[4:0]	00001 – 1.25V	01001 – 1.65V	10001 – 2.20V	11001 – 2.80V
LDO3_V[4:0]	00010 – 1.30V	01010 – 1.70V	10010 – 2.30V	11010 – 2.85V
LDO5_V[4:0]	00011 – 1.35V	01011 – 1.75V	10011 – 2.40V	11011 – 2.90V
	00100 – 1.40V	01100 – 1.80V	10100 – 2.50V	11100 – 2.95V
	00101 – 1.45V	01101 – 1.85V	10101 – 2.60V	11101 – 3.00V
	00110 – 1.50V	01110 – 1.90V	10110 – 2.65V	11110 – 3.10V
	00111 – 1.55V	01111 – 2.00V	10111 – 2.70V	11111 – 3.30V
LDO4_V[4:0]	00000 – 0.80V	01000 – 1.35V	10000 – 1.75V	11000 – 2.40V
	00001 – 0.85V	01001 – 1.40V	10001 – 1.80V	11001 – 2.50V
	00010 – 0.90V	01010 – 1.45V	10010 – 1.85V	11010 – 2.60V
	00011 – 1.00V	01011 – 1.50V	10011 – 1.90V	11011 – 2.65V
	00100 – 1.10V	01100 – 1.55V	10100 – 2.00V	11100 – 2.70V
	00101 – 1.20V	01101 – 1.60V	10101 – 2.10V	11101 – 2.75V
	00110 – 1.25V	01110 – 1.65V	10110 – 2.20V	11110 – 2.80V
	00111 – 1.30V	01111 – 1.70V	10111 – 2.30V	11111 – 2.85V
BUCK_V1[4:0] BUCK_V2[4:0]	<p>0000</p> <p>External resistor divider</p> <p>00001 – 0.80V</p> <p>00010 – 0.85V</p> <p>00011 – 0.90V</p> <p>00100 – 0.95V</p> <p>00101 – 1.00V</p> <p>00110 – 1.05V</p> <p>00111 – 1.10V</p>	<p>01000 – 1.15V</p> <p>01001 – 1.20V</p> <p>01010 – 1.25V</p> <p>01011 – 1.30V</p> <p>01100 – 1.35V</p> <p>01101 – 1.40V</p> <p>01110 – 1.45V</p> <p>01111 – 1.50V</p>	<p>10000 – 1.55V</p> <p>10001 – 1.60V</p> <p>10010 – 1.65V</p> <p>10011 – 1.70V</p> <p>10100 – 1.75V</p> <p>10101 – 1.80V</p> <p>10110 – 1.85V</p> <p>10111 – 1.90V</p>	<p>11000 – 1.95V</p> <p>11001 – 2.00V</p> <p>11010 – 2.05V</p> <p>11011 – 2.10V</p> <p>11100 – 2.15V</p> <p>11101 – 2.20V</p> <p>11110 – 2.25V</p> <p>11111 – 2.30V</p>
	BUCK_V1[4:0] should be higher (or equal) than BUCK_V2[4:0].			
LDO1_T[2:0]	000 – start up delay 0		100 – start up delay = 4 * time step t_S	
LDO2_T[2:0]	001 – start up delay = 1 * time step t_S		101 – start up delay = 5 * time step t_S	
LDO3_T[2:0]	010 – start up delay = 2 * time step t_S		110 – start up delay = 6 * time step t_S	
LDO4_T[2:0]	011 – start up delay = 3 * time step t_S		111 – NO startup	
LDO5_T[2:0]	For proper startup operation “111 NO start up” should have corresponding bit in ENABLE_BITS register 0x08 set to 0 (disable).			
BUCK_T[2:0]				
FORCE_PWM	<p>1 – Buck is forced to work in PWM mode</p> <p>0 – Buck works in automatic PFM/PWM selection mode.</p>			

Register 0x08

LDO1_EN LDO2_EN LDO3_EN LDO4_EN LDO5_EN BUCK_EN	In STANDBY mode 1 – During next START UP sequence will be enabled. 0 – During next START UP sequence will be NOT enabled. For proper operation output having “111 NO start up” should have corresponding enable bit 0 (disable).	In IDLE mode the bit has immediate effect. 1 – Enable 0 – Disable
SLEEP_MODE	1 – SLEEP 0 – normal This bit has effect only if EXT_SLEEP_CONTROL=0 (register 0x00)	
DVS_V2/V1	1 – buck voltage is BUCK_V1[4:0] 0 – buck voltage is BUCK_V2[4:0] This bit has effect only if EXT_DVS_CONTROL=0 (register 0x00)	

Register 0x09

LDO1_PULLDOWN LDO2_PULLDOWN LDO3_PULLDOWN LDO4_PULLDOWN LDO5_PULLDOWN BUCK_PULLDOWN	1 – Pull down enabled 0 – Pull down disabled	
APU_TSD	This bit defines either to reset registers or not before LP8720 automatically starts START UP sequence form Thermal Shutdown after cooling down if EN-pin is High. 1 – No change to registers – registers content stays the same as before Thermal Shutdown. 0 – Reset registers to default values before START UP from Thermal Shutdown.	

Register 0x0A (Read Only)

TSD	1 – device is in Thermal Shutdown. 0 – device is NOT in Thermal Shutdown .
TSD_EW	1 – device temperature is higher than Thermal Shutdown Early Warning threshold. 0 – device temperature is lower than Thermal Shutdown Early Warning threshold.

Register 0x0B (Read Only)

TSD_INT	1 – Interrupt that was caused by Thermal Shutdown 0 – No Interrupt that was caused by Thermal Shutdown
TSD_EW	1 – Interrupt that was caused by Thermal Shutdown Early Warning 0 – No Interrupt that was caused by Thermal Shutdown Early Warning

Note 1: all reads from this register are destructive (all bits are reset to 0 after reading).

Note 2: read from this register releases IRQ_N-pin (if was pushed down).

Register 0x0C

TSD_MASK	1 – TSD interrupt is masked 0 – TSD interrupt is NOT masked
TSD_EW_MASK	1 – TSD_EW interrupt is masked 0 – TSD_EW interrupt is NOT masked

Support Functions

REFERENCE

LP8720 has internal reference block creating all necessary references and biasing for all blocks.

OSCILLATOR

There is internal oscillator giving clock to the bucks and to logic control.

$V_{BATT}=3.6V$

Parameter	Typ	Min	Max	Unit
Oscillator frequency	2.0	1.9	2.1	MHz

THERMAL SHUTDOWN

The Thermal Shutdown (TSD) function monitors the chip temperature to protect the chip from temperature damage caused

eg. by excessive power dissipation. The temperature monitoring function has two threshold values TSD and TSD_EW that result in protective actions.

When TSD_EW +125°C is exceeded, then IRQ_N is set to low and "1" is written to TSD_EW bit in both STATUS register and in INTERRUPT register.

If the temperature exceeds TSD +160°C, then PMU initiates Emergency Shutdown.

The POWER UP operation after Thermal Shutdown can be initiated only after the chip has cooled down to the +115°C threshold

Parameter	Typ	Unit
TSD *)	160	°C
TSD_EW *)	125	°C
TSD_EW Hysteresis *)	10	°C

*) Guaranteed by design.

Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

$V_{BATT} = VINB, VBATT$	-0.3V to +6V
VIN1, VIN2	-0.3V to $V_{BATT}+0.15V$, max 6V
All other pins	-0.3V to $V_{BATT}+0.3V$, max 6V
Junction Temperature (T _{J-MAX})	150°C
Storage Temperature	-40 to 150°C
Maximum Continuous Power Dissipation	
P_{D-MAX} (Note 3)	1.75 W
ESD (Note 4)	2 kV HBM 200V MM

Operating Ratings (Note 1, Note 2)

$V_{BATT} = VINB, VBATT$	2.7 to 4.5V
VIN1, VIN2	2.5V to V_{BATT}
All input-only pins	0V to V_{BATT}
Junction Temperature (T _J)	-40 to 125°C
Ambient Temperature (T _A)	-40 to 85°C
Maximum Power Dissipation (TA = 70°C), (Note 5)	1.2 W

Thermal Properties (Note 9)

Junction-to-Ambient Thermal Resistance (θ _{JA}) (Jedec Standard Thermal PCB) Micro SMD 20	45°C/W
---	--------

Current Consumption

Unless otherwise noted, $V_{VBATT}=V_{VINB}=V_{VIN1}=V_{VIN2}=3.6V$, $GND=GNDB=0V$, $C_{VBATT}=C_{VIN1}=C_{VIN2}=2.2 \mu F$, $C_{VINB}=10 \mu F$. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= -40 to +125°C. (Note 6)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
$I_{Q(STANDBY)}$	Battery Standby Current	$V_{BATT} = 3.6V$	0.7		5	μA
$I_{Q(SLEEP)}$	Battery Current in SLEEP Mode @ 0 load	BUCK and all LDO's enabled	190		270	μA
$I_{Q(SLEEP)}$	Battery Current in SLEEP Mode @ 0 load	LDO1, LDO2, LDO3 and LDO4 enabled	170			μA
$I_{Q(SLEEP)}$	Battery Current in SLEEP Mode @ 0 load	LDO3 enabled	100		150	μA
$I_{Q(SLEEP)}$	Battery Current in SLEEP Mode @ 0 load	LDO1 and BUCK enabled	100			μA
I_Q	Battery Current @ 0 load	BUCK and all LDO's enabled	270		400	μA
I_Q	Battery Current @ 0 load	LDO1, LDO2, LDO3 and LDO4 enabled	230			μA
I_Q	Battery Current @ 0 load	LDO3 enabled	120		200	μA
I_Q	Battery Current @ 0 load	LDO1 and BUCK enabled	120			μA

Power on Reset

Unless otherwise noted, $V_{VBATT}=V_{VINB}=V_{VIN1}=V_{VIN2}=3.6V$, $GND=GNDB=0V$, $C_{VBATT}=C_{VIN1}=C_{VIN2}=2.2 \mu F$, $C_{VINB}=10 \mu F$. Typical values and limits appearing in normal type apply for T_J=25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J= -40 to +125°C. (Note 6)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{POR_HI}	POR higher threshold	V_{VBATT} rising	2.2	2.0	2.4	V
V_{POR_LO}	POR lower threshold	V_{VBATT} falling (Note 7)	1.4			V

Logic and Control

Unless otherwise noted, $V_{VBATT}=V_{VINB}=V_{VIN1}=V_{VIN2}=3.6V$, $GND=GNDB=0V$, $C_{VBATT}=C_{VIN1}=C_{VIN2}=2.2\mu F$, $C_{VINB}=10\mu F$. Typical values and limits appearing in normal type apply for $T_J=25^\circ C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_J=-40$ to $+125^\circ C$. (*Note 6*)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
Logic and Control Inputs						
VIL	Input Low Level	EN, SCL, SDA, DVS			0.4	V
VIH	Input High Level	EN, SCL, SDA, DVS		1.2		V
IIL	Input Current	All logic inputs		-5	+5	μA
RPD	Pull Down Resistance	From EN to GND	550	300	900	$k\Omega$
Logic and Control Outputs						
VOL	Output Low Level	IRQ_N, SDA, IOOUT=2mA			0.4	V
VOH	Output High Level	IRQ_N, SDA are Open drain outputs.		NA		μA

Buck Converter

Unless otherwise noted, $V_{VBATT}=V_{VINB}=V_{VIN1}=V_{VIN2}=3.6V$, $GND=GND_B=0V$, $C_{VBATT}=C_{VIN1}=C_{VIN2}=2.2\ \mu F$, $C_{VINB}=10\ \mu F$. Typical values and limits appearing in normal type apply for $T_J=25^\circ C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_J = -40$ to $+125^\circ C$. (*Note 6, Note 10*)

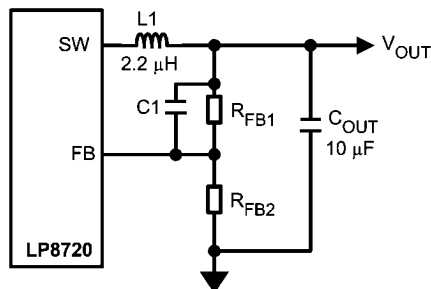
Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{FB}	Feedback Voltage	$3.0V \leq V_{IN} \leq 4.5V$ external resistor divider	0.5	0.485	0.515	V
V_{BUCK}	Output Voltage, PWM Mode	$3.0V \leq V_{IN} \leq 4.5V$	1.2	1.164	1.236	V
$V_{VOUT,PFM}$	Output Voltage regulation in PFM mode relative to regulation in PWM mode	(<i>Note 7</i>)	1.5			%
V_{OUT}	Line Regulation	$3.0V \leq V_{IN} \leq 4.5V$ $I_{OUT} = 10\ mA$	0.14			%/V
V_{OUT}	Load Regulation	$100mA \leq I_{OUT} \leq 300mA$	0.09			%/mA
I_{LIM_PWM}	Switch Peak Current Limit	PWM Mode @ 400 mA $3.0V \leq V_{IN} \leq 4.5V$	900	500		mA
$R_{DSON(P)}$	P channel FET on resistance	$V_{IN} = 3.6V$, $I_D = 100mA$	310		500	m Ω
$R_{DSON(N)}$	N channel FET on resistance		160		300	m Ω
f_{OSC}	Internal Oscillator Frequency	PWM Mode	2	1.9 1.7	2.1 2.3	MHz
Efficiency		$I_{OUT} = 5mA$, PFM-mode $V_{OUT} = 1.2V$ (<i>Note 7</i>)	88			%
		$I_{OUT} = 200mA$, PWM-mode $V_{OUT} = 1.2V$ (<i>Note 7</i>)	90			
T_{STUP}	Start Up Time	$I_{OUT} = 0$, $V_{OUT} = 1.2V$ (<i>Note 7</i>)	140			μs

Buck Output Voltage Programming in Register 0x06 and 0x07

BUCK1_Vx	V_{OUT}	BUCK1_Vx	V_{OUT}
5h'00	External resistor divider	5h'10	1.55
5h'01	0.80	5h'11	1.60
5h'02	0.85	5h'12	1.65
5h'03	0.90	5h'13	1.70
5h'04	0.95	5h'14	1.75
5h'05	1.00	5h'15	1.80
5h'06	1.05	5h'16	1.85
5h'07	1.10	5h'17	1.90
5h'08	1.15	5h'18	1.95
5h'09	1.20	5h'19	2.00
5h'0A	1.25	5h'1A	2.05
5h'0B	1.30	5h'1B	2.10
5h'0C	1.35	5h'1C	2.15
5h'0D	1.40	5h'1D	2.20
5h'0E	1.45	5h'1E	2.25
5h'0F	1.50	5h'1F	2.30

Output Voltage Selection Using External Resistor Divider

Buck1 output voltage can be programmed via the selection of the external feedback resistor network.



30067508

V_{OUT} will be adjusted to make the voltage at FB equal to 0.5V. The resistor from FB to ground R_{FB2} should be around 200 kΩ to keep the current drawn through the resistor network to a minimum but large enough that it is not susceptible to noise. With $R_{FB2}=200$ kΩ and V_{FB} at 0.5V, the current through the resistor feedback network will be 2.5 μA.

The formula for output voltage selection is

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

V_{OUT} – output voltage

V_{FB} – feedback voltage (0.5V)

For any out voltage greater than or equal to 0.8V a transfer function zero should be added by the addition of a capacitor C1. The formula for calculation of C1 is:

$$C1 = \frac{1}{(2 \times \pi \times R_{FB1} \times 45 \times 10^3)}$$

For recommended component values see the table below.

V_{OUT} [V]	R_{FB1} [kΩ]	R_{FB2} [kΩ]	C1 [pF]	L [μH]	C_{OUT} [μF]
1.0	200	200	18	2.2	10
1.2	280	200	12	2.2	10
1.4	360	200	10	2.2	10
1.5	360	180	10	2.2	10
1.6	440	200	8.2	2.2	10
1.85	540	200	6.8	2.2	10

LDO's

There are all together 5 LDO's in LP8720 grouped as

A-type LDO's (LDO 2,3)

D-type LDO's (LDO 1,5)

LO-type LDO (LDO4)

The A-type LDO's are optimized for supplying of analog loads and have ultra low noise (15 μ VRMS) and excellent PSRR (70dB) performance.

The D-type LDO's are optimized for good dynamic performance to supply different fast changing (digital) loads.

The LO-type LDO is optimized for low output voltage and for good dynamic performance to supply different fast changing (digital) loads.

LDO1, 2, 3 and 5 Output Voltage Programming

Data Code LDOx_V	LDOx [V]	Data Code LDOx_V	LDOx [V]
5h'00	1.20	5h'10	2.10
5h'01	1.25	5h'11	2.20
5h'02	1.30	5h'12	2.30
5h'03	1.35	5h'13	2.40
5h'04	1.40	5h'14	2.50
5h'05	1.45	5h'15	2.60
5h'06	1.50	5h'16	2.65
5h'07	1.55	5h'17	2.70
5h'08	1.60	5h'18	2.75
5h'09	1.65	5h'19	2.80
5h'0A	1.70	5h'1A	2.85
5h'0B	1.75	5h'1B	2.90
5h'0C	1.80	5h'1C	2.95
5h'0D	1.85	5h'1D	3.00
5h'0E	1.90	5h'1E	3.10
5h'0F	2.00	5h'1F	3.30

All LDO's can be programmed through serial interface for 32 different output voltage value, which are summarized in the "LDO Output Voltage Programming" tables below.

At the PMU power on, LDO's start up according to the selected startup sequence and the default voltages after start-up sequence depend on startup setup. See section Power-On and Power-Off Sequences for details.

For stability all LDO's have to have connected to output an external capacitor C_{OUT} with recommended value of 1 μ F. It is important to select the type of capacitor which capacitance will in no case (voltage, temperature, etc) be outside of limits specified in the LDO electrical characteristics.

LDO4 Output Voltage Programming

Data Code LDO4_V	LDO4 [V]	Data Code LDO4_V	LDO4 [V]
5h'00	0.80	5h'10	1.75
5h'01	0.85	5h'11	1.80
5h'02	0.90	5h'12	1.85
5h'03	1.00	5h'13	1.90
5h'04	1.10	5h'14	2.00
5h'05	1.20	5h'15	2.10
5h'06	1.25	5h'16	2.20
5h'07	1.30	5h'17	2.30
5h'08	1.35	5h'18	2.40
5h'09	1.40	5h'19	2.50
5h'0A	1.45	5h'1A	2.60
5h'0B	1.50	5h'1B	2.65
5h'0C	1.55	5h'1C	2.70
5h'0D	1.60	5h'1D	2.75
5h'0E	1.65	5h'1E	2.80
5h'0F	1.70	5h'1F	2.85

A-Type LDO Electrical Characteristics

Unless otherwise noted, $V_{VBATT}=V_{VINB}=V_{VIN1}=V_{VIN2}=3.6V$, $GND=GNDB=0V$, $C_{VBATT}=C_{VIN1}=C_{VIN2}=2.2\ \mu F$, $C_{VINB}=10\ \mu F$. Typical values and limits appearing in normal type apply for $T_J=25^\circ C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_J=-40$ to $+125^\circ C$. (Note 6)

Symbol	Parameter	Conditions	LDO#	Typ	Limit		Units
					Min	Max	
V_{OUT}	Output Voltage Accuracy	$I_{OUT} = 1mA$, $V_{OUT} = 2.85V$	2,3		-2	+2	%
					-3	+3	%
I_{SC}	Output Current Limit	$V_{OUT} = 0V$	2,3	600			mA
V_{DO}	Dropout Voltage	$I_{OUT} = I_{MAX}$ (Note 8)	2,3	200		400	mV
ΔV_{OUT}	Line Regulation	$V_{OUT} + 0.5V \leq V_{IN} \leq 4.5V$ $I_{OUT} = I_{MAX}$	2,3	1			mV
	Load Regulation	$1mA \leq I_{OUT} \leq I_{MAX}$	2,3	5			mV
e_N	Output Noise Voltage	$10Hz \leq f \leq 100kHz$ $C_{OUT} = 1\mu F$ (Note 7)	2,3	15			μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	$f=10kHz$, $C_{OUT} = 1\mu F$ $I_{OUT} = 20mA$ (Note 7)	2,3	70			dB
$t_{STARTUP}$	Start-Up Time from Shut-down	$C_{OUT} = 1\mu F$, $I_{OUT} = I_{MAX}$ (Note 7)	2,3	35			μs
$V_{Transient}$	Start-Up Transient Overshoot	$C_{OUT} = 1\mu F$, $I_{OUT} = I_{MAX}$ (Note 7)	2,3			30	mV
C_{OUT}	External output capacitance for stability		2,3	1.0	0.5	20	μF

D-Type and LO-Type LDO Electrical Characteristics

Unless otherwise noted, $V_{VBATT}=V_{VINB}=V_{VIN1}=V_{VIN2}=3.6V$, $GND=GNDB=0V$, $C_{VBATT}=C_{VIN1}=C_{VIN2}=2.2\ \mu F$, $C_{VINB}=10\ \mu F$. Typical values and limits appearing in normal type apply for $T_J=25^\circ C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_J=-40$ to $+125^\circ C$. (Note 6)

Symbol	Parameter	Conditions	LDO#	Typ	Limit		Units
					Min	Max	
V_{OUT}	Output Voltage Accuracy	$I_{OUT} = 1mA$, $V_{OUT} = 2.85V$	1,5		-2	+2	%
					-3	+3	%
		$I_{OUT} = 1mA$, $V_{OUT} = 1.20V$	4		-2	+2	%
					-3	+3	%
		$I_{OUT} = 1mA$, $V_{OUT} = 2.60V$	4		-3	+3	%
					-4	+4	%
I_{SC}	Output Current Limit	$V_{OUT} = 0V$	1,4,5	600			mA
V_{DO}	Dropout Voltage	$I_{OUT} = I_{MAX}$ (Note 8)	1,4,5	190		400	mV
ΔV_{OUT}	Line Regulation	$V_{OUT} + 0.5V \leq V_{IN} \leq 4.5V$ $I_{OUT} = I_{MAX}$	1,4,5	2			mV
	Load Regulation	$1mA \leq I_{OUT} \leq I_{MAX}$	1,4,5	5			mV
e_N	Output Noise Voltage	$10Hz \leq f \leq 100kHz$ $C_{OUT} = 1\mu F$ (Note 7)	1,4,5	100			μV_{RMS}
PSRR	Power Supply Ripple Rejection Ratio	$f=10kHz$, $C_{OUT} = 1\mu F$ $I_{OUT} = 20mA$ (Note 7)	1,4,5	55			dB
$t_{STARTUP}$	Start-Up Time from Shut-down	$C_{OUT} = 1\mu F$, $I_{OUT} = I_{MAX}$ (Note 7)	1,4,5	35			μs
$V_{Transient}$	Start-Up Transient Overshoot	$C_{OUT} = 1\mu F$, $I_{OUT} = I_{MAX}$ (Note 7)	1,4,5			30	mV
C_{OUT}	External output capacitance for stability		1,4,5	1.0	0.5	20	μF

Serial Interface

Unless otherwise noted, $V_{VBATT}=V_{VINB}=V_{VIN1}=V_{VIN2}=3.6V$, $GND=GND_B=0V$, $C_{VBATT}=C_{VIN1}=C_{VIN2}=2.2\ \mu F$, $C_{VINB}=10\ \mu F$. Typical values and limits appearing in normal type apply for $T_J=25^\circ C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_J=-40$ to $+125^\circ C$. (*Note 6*, *Note 7*)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
f_{CLK}	Clock Frequency				400	kHz
t_{BF}	Bus-Free Time between START and STOP			1.3		μs
t_{HOLD}	Hold Time Repeated START Condition			0.6		μs
t_{CLK-LP}	CLK Low Period			1.3		μs
t_{CLK-HP}	CLK High Period			0.6		μs
t_{SU}	Set-Up Time Repeated START Condition			0.6		μs
$t_{DATA-HOLD}$	Data Hold Time			50		ns
$t_{DATA-SU}$	Data Set-Up Time			100		ns
t_{SU}	Set-Up Time for STOP Condition			0.6		μs
t_{TRANS}	Maximum Pulse Width of Spikes that Must Be Suppressed by the Input Filter of Both DATA & CLK Signals		50			ns

Notes to Electrical Characteristics Tables

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula

$$P = (T_J - T_A) / \theta_{JA}, \text{ (eq. 1)}$$

where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 1.75W rating appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, $150^\circ C$ for T_J , $70^\circ C$ for T_A , and $45^\circ C/W$ for θ_{JA} . More power can be dissipated safely at ambient temperatures below $70^\circ C$. Less power can be dissipated safely at ambient temperatures above $70^\circ C$. The Absolute Maximum power dissipation can be increased by 22mW for each degree below $70^\circ C$, and it must be de-rated by 22 mW for each degree above $70^\circ C$.

Note 4: The human-body model is 100 pF discharged through 1.5 k Ω . The machine model is a 200 pF capacitor discharged directly into each pin, MIL-STD-883 3015.7.

Note 5: Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 1.2W rating for Micro SMD 20 appearing under Operating Ratings results from substituting the maximum junction temperature for operation, $125^\circ C$, for T_J , $70^\circ C$ for T_A , and $45^\circ C/W$ for θ_{JA} into (eq. 1) above. More power can be dissipated at ambient temperatures below $70^\circ C$. Less power can be dissipated at ambient temperatures above $70^\circ C$. The maximum power dissipation for operation can be increased by 22mW for each degree below $70^\circ C$, and it must be de-rated by 22 mW for each degree above $70^\circ C$.

Note 6: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with $T_J = 25^\circ C$. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 7: Guaranteed by design.

Note 8: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the 2.5V minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.

Note 9: Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Note 10: Guaranteed for output voltages no less than 1.0V

I²C-Compatible Serial Bus Interface

INTERFACE BUS OVERVIEW

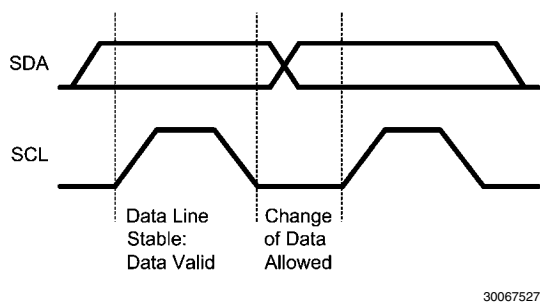
The I²C compatible synchronous serial interface provides access to the programmable functions and registers on the device.

This protocol uses a two-wire interface for bi-directional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor of 1.5 kΩ, and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (SCL).

DATA TRANSACTIONS

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.



30067527

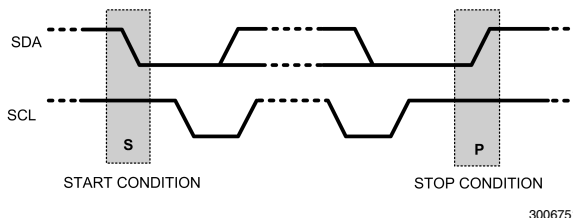
FIGURE 1. Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop

Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

START AND STOP

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.



30067510

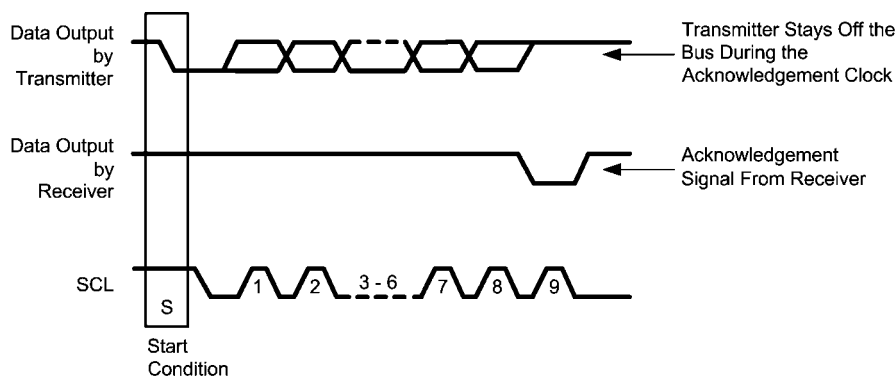
FIGURE 2. Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

ACKNOWLEDGE CYCLE

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.



30067528

FIGURE 3. Bus Acknowledge Cycle

”ACKNOWLEDGE AFTER EVERY BYTE” RULE

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the “acknowledge after every byte” rule.

When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

ADDRESSING TRANSFER FORMATS

Each device on the bus has a unique slave address. The LP8720 operates as a slave device. Slave address is selectable by IDSEL-pin.

When IDSEL= VBATT then slave address is 7h’7F

When IDSEL= floating (Hi-Z) then slave address is 7h’7C

When IDSEL= GND then slave address is 7h’7D

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

CONTROL REGISTER WRITE CYCLE

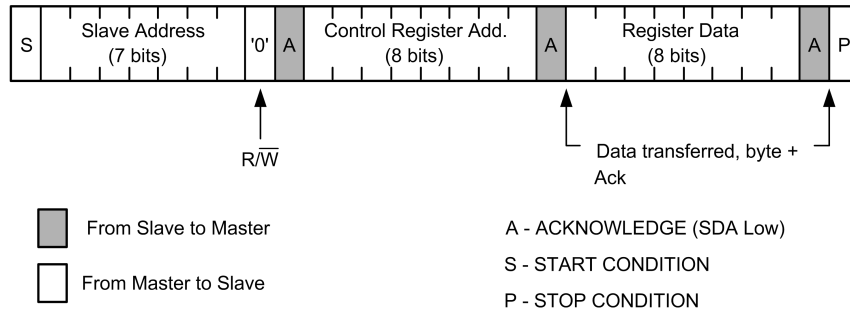
- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = '0').
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

CONTROL REGISTER READ CYCLE

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = '0').
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = "1").
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

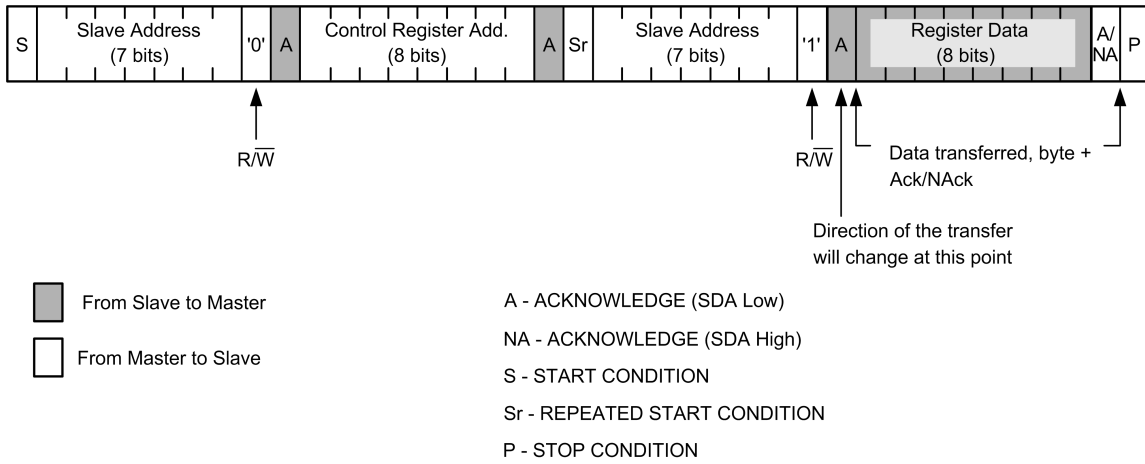
	Address Mode
Data Read	<Start Condition> <Slave Address><r/w = '0'>[Ack] <Register Addr.>[Ack] <Repeated Start Condition> <Slave Address><r/w = '1'>[Ack] [Register Data]<Ack or NAck> ... additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w = '0'>[Ack] <Register Addr.>[Ack] <Register Data>[Ack] ... additional writes to subsequent register address possible <Stop Condition>
< > Data from master [] Data from slave	

REGISTER READ AND WRITE DETAIL



30067529

FIGURE 4. Register Write Format



30067530

FIGURE 5. Register Read Format

Notes

LP8720

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:
www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2009 National Semiconductor Corporation

For the most current product information visit us at www.national.com



National Semiconductor Americas Technical Support Center
 Email: support@nsc.com
 Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
 Email: europe.support@nsc.com

National Semiconductor Asia Pacific Technical Support Center
 Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
 Email: jpn.feedback@nsc.com