NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE (YYMMDD)	Form Approved OMB No. 0704-0188
96-10-29	

2. PROCURING ACTIVITY NO.	
3. DODAAC	

4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code)	5. CAGE CODE	6. NOR NO.
	Defense Supply Center Columbus 3990 East Broad St. Columbus, OH 43216-5000	67268	5962-R043-97
a. TYPED NAME (First, Middle Initial, Last)		7. CAGE CODE 67268	8. DOCUMENT NO. **5962-90692**

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
MICROCIRCUIT, DIGITAL, CMOS, 16-BIT MICROCONTROLLER WITH ON CHIP EPROM, MONOLITHIC SILICON	a. CURRENT B	b. NEW C	N/A

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "C".
Revisions description column; add "Changes in accordance with NOR 5962-R043-97".
Revisions date column; add "96-10-29".
Revision level block; change from "B" to "C".
Rev status of sheets; for sheet 1, 16 change from "B" to "C".

Sheet 16: Change dimensions of Symbol A from: 0.80 min inches, 0.106 max inches, 2.03 min millimeters, 2.69 max millimeters
to: 0.115 min inches, 0.145 max inches, 2.91 min millimeters, 3.68 max millimeters
Change dimensions of Symbol D1 from: 0.935 min inches, 0.424 max inches, 23.75 min millimeters
to: 0.926 min inches, 0.970 max inches, 23.52 min millimeters
Change status of revision level to "C"

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. (X one)		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME (First, Middle Initial, Last)
DSCC-VAC	Monica L. Poelking

d. TITLE	e. SIGNATURE	f. DATE SIGNED (YYMMDD)
Chief, Custom Microelectronics	Monica L. Poelking	96-10-29

15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED (Signature)	c. DATE SIGNED (YYMMDD)s
DSCC-VAC	Thomas M. Hess	96-10-29

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 02 and 03. Editorial changes throughout.	95-03-29	Thomas M. Hess
B	Add device type 04. Editorial changes throughout.	96-02-07	Thomas M. Hess

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS																	
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Christopher A. Rauch

CHECKED BY
Tim Noh

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
91-11-18

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 16-BIT MICROCONTROLLER WITH ON CHIP EPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-90692

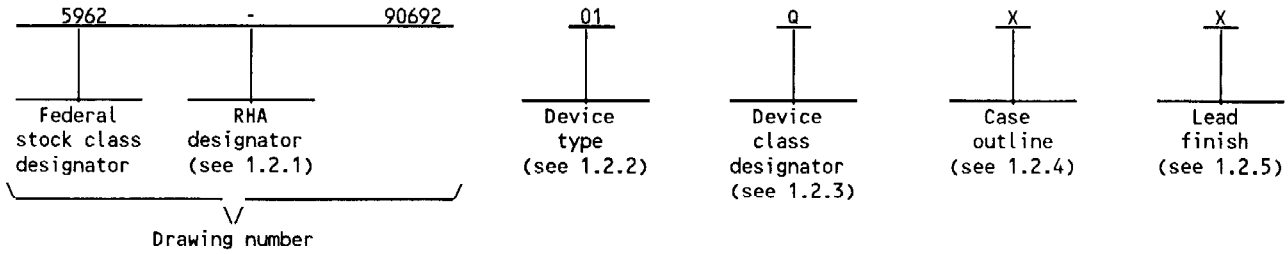
SHEET 1 OF 34

DESC FORM 193
JUL 94

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	87C196KC	16 MHz CHMOS 16-bit, microcontroller with 16 k bytes of on-chip EPROM and 512 byte register file.
02	87C196KD	16 MHz CHMOS 16-bit, microcontroller with 32 k bytes of on-chip EPROM and 1024 byte register RAM.
03	87C196KD	20 MHz CHMOS 16-bit microcontroller with 32 k bytes of on-chip EPROM and 1024 byte register RAM.
04	87C196KC	16 MHz CHMOS 16-bit, microcontroller with 16 k bytes of on-chip EPROM and 512 byte register file. 1/

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA3-P68	68	Pin grid array 2/
Y	See figure 1	68	Ceramic quad flat 2/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Device type 01 and 04 are not 100% interchangeable. Device type 04 is the result of a die mask change, see table I for electrical performance differences.
2/ Lid shall be transparent to permit ultraviolet light erasure.

1.3 Absolute maximum ratings. 3/

Storage temperature range	-65°C to +150°C
Voltage on any pin with respect to ground range	-0.5 V dc to +7.0 V dc
Power dissipation (P_D)	1.5 W
Lead temperature (soldering, 10 seconds)	+265°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	See MIL-STD-1835
Case Y	9.0°C/W
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Supply voltage range V_{CC}	+5.0 V dc ±10%
Analog supply voltage, V_{REF}	+5.0 V dc ±10%
Oscillator frequency, F_{OSC}	
Device 01, 02, 04	3.5 to 16 MHz
Device 03	3.5 to 20 MHz

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	80 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The block diagram shall be as specified on figure 3.

3.2.4 EPROM programming waveforms. The EPROM program programming waveforms shall be as specified in figure 5.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$ 1/		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input low voltage	V_{IL}			1,2,3	All	-0.5 2/	0.8	V
Input high voltage all except RESET, XTALI and EA	V_{IH}					$0.2V_{CC}$ +1.0	V_{CC} 2/	
Input high voltage on XTALI and EA	V_{IH1}					$0.7V_{CC}$	V_{CC} 2/	
Input high voltage on RESET	V_{IH2}				01-03	2.2	V_{CC} 2/	
					04	2.32		
Output low voltage	V_{OL}	I_{OL} = 200 µA I_{OL} = 2.8 mA I_{OL} = 7 mA	V_{CC} = 4.5 V V_{IN} = 0.8 V		All		0.3 0.45 1.50	
Output low voltage in RESET on P2.5	V_{OL1} 3/	I_{OL} = +0.4 mA					0.8	
Output high voltage (std outputs)	V_{OH}	I_{OH} = 200 µA I_{OH} = -3.2 mA I_{OH} = -7 mA				V_{CC}-0.3 V_{CC}-0.7 V_{CC}-1.5		
Output high voltage (Quasi-bidirectional outputs)	V_{OH1}	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA			All	V_{CC}-0.3 V_{CC}-0.7 V_{CC}-1.5		
Output high voltage in RESET on P2.0	V_{OH2} 3/	I_{OH} = -0.8 mA				2.0		
Input leakage current (std inputs except NMI)	I_{LI}	V_{IN} = 0.0 V		1, 2, 3			-10	µA
		V_{IN} = 5.20 V					+10	
Input leakage current (port 0)	I_{LI1}	$0 \le V_{IN} \le V_{REF}$					±3	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$ 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
1 to 0 transition current (QBD pins)	I_{TL}	V_{IN} = 2.0 V	1,2,3	All		-650	µA
Logical 0 input current (QBD pins)	I_{IL}	V_{IN} = 0.45 V				-70	
Logical 1 input current (NMI)	I_{IH}	$V_{IN} = V_{CC}$ - 0.3 V				+250	
Active mode current in reset	I_{CC}	XTAL1 = f_{XTAL} $V_{CC} = V_{PP} = V_{REF}$ = 5.5 V	4,5,6	01-02		75	mA
				03		93	
				04		75	
A/D converter reference current	I_{REF}	$V_{CC} = V_{PP} = V_{REF}$ = 5.5 V	1,2,3	All		5	
Idle mode current	I_{IDLE}	$V_{CC} = V_{PP} = V_{REF}$ = 5.5 V XTAL1 = 16 MHz	4,5,6	01,02,04		30	
		$V_{CC} = V_{PP} = V_{REF}$ = 5.5 V XTAL1 = 20 MHz		03			
Powerdown mode current	I_{PD}	$V_{CC} = V_{PP} = V_{REF}$ = 5.5 V		All		70	µA
Reset pull-up resistor 2/	R_{RST}	V_{CC} = 5.5 V, V_{IN} = 4.0 V	1,2,3		6k	65k	Ω
Pin capacitance 2/ (any pin to V_{SS})	C_S	See 4.4.1c	4			10	pF
Functional testing		See 4.4.1d	7,8				
Address valid to READY set-up	t_{AVYV}	Capacitive load on all pins = 100 pF, F_{OSC} = 16 MHz rise and fall times = 10 ns See figure 4, Ready and bus timing	9,10,11	All		$2t_{OSC}$-75	ns
ALE low to READY set-up	t_{LLYV}			01-03		t_{OSC}-70	
				04		t_{OSC}-75	
READY hold after CLKOUT low 4/	t_{CLYX}			All	0	t_{OSC}-30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$ 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Ready hold after ALE low 4/	t_{LLYX}	Capacitive load on all pins = 100 pF, F_{OSC} = 16 MHz rise and fall times = 10 ns See figure 4, Ready and bus timing	9,10,11	All	t_{OSC}-15	$2t_{OSC}$-40	ns
Address valid to BUSWIDTH set-up	t_{AVGV}					$2t_{OSC}$-75	
ALE low to BUSWIDTH set-up	t_{LLGV}			01-03		t_{OSC}-60	
				04		t_{OSC}-65	
BUSWIDTH hold after CLKOUT low	t_{CLGX}			All	0		
Address valid to input data valid 5/	t_{AVDV}					$3t_{OSC}$-55	
RD active to input data valid 5/	t_{RLDV}			01-03		t_{OSC}-22	
				04		t_{OSC}-26	
CLKOUT low to input data valid	t_{CLDV}			All		t_{OSC}-50	
End of RD to input data float	t_{RHDZ}			01-03		t_{OSC}	
				04		t_{OSC}-5	
Data hold after RD inactive	t_{RXDX}			All	0		
Frequency of XTAL1	f_{XTAL}			01,02 04	3.5	16	MHz
Frequency of XTAL1	f_{XTAL}			03	3.5	20	MHz
$1/f_{XTAL}$	t_{OSC}			01,02 04	62.5	286	ns
$1/f_{XTAL}$	t_{OSC}			03	50	286	
XTAL1 high to CLKOUT high or low	t_{XHCH}			All	10	110	
CLKOUT cycle time 2/	t_{CLCL}				$2t_{OSC}$	$2t_{OSC}$	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$ 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLKOUT high period set-up	t_{CHCL}	Capacitive load on all pins = 100 pF, F_{OSC} = 16 MHz rise and fall times = 10 ns See figure 4, Ready and bus timing	9,10,11	All	t_{OSC}-10	t_{OSC}+20	ns
CLKOUT falling edge to ALE rising	t_{CLLH}				-5	15	
ALE falling edge to CLKOUT rising	t_{LLCH}			01-03	20	+15	
				04	-29	+15	
ALE cycle time 2/ 5/	t_{LHLH}			All	$4t_{OSC}$	$4t_{OSC}$	
ALE high period	t_{LHLL}			01-03	t_{OSC}-10	t_{OSC}+10	
				04	t_{OSC}-10	t_{OSC}+15	
Address set-up to ALE falling edge	t_{AVLL}			All	t_{OSC}-15		
Address hold after ALE falling edge	t_{LLAX}			01-03	t_{OSC}-40		
				04	t_{OSC}-49		
ALE falling edge to RD falling edge	t_{LLRL}			01-03	t_{OSC}-30		
				04	t_{OSC}-36		
RD low to CLKOUT falling edge	t_{RLCL}			All	0	30	
RD low period 5/	t_{RLRH}				t_{OSC}-5		
RD rising edge to ALE rising edge 6/	t_{RHLH}				t_{OSC}	t_{OSC}+25	
RD low to address float	t_{RLAZ}			01		10	
				02,03		30	
				04		15	
ALE falling edge to WR falling edge	t_{LLWL}			All	t_{OSC}-10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$ 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLKOUT low to WR falling edge	t_{CLWL}	Capacitive load on all pins = 100 pF, F_{OSC} = 16 MHz rise and fall times = 10 ns See figure 4, Ready and bus timing	9,10,11	All	0	25	ns
Data stable to WR rising edge	t_{QVWH}				$t_{OSC}-23$		
CLKOUT high to WR rising edge	t_{CHWH}				-10	15	
WR low period 5/	t_{WLWH}				$t_{OSC}-30$		
Data hold after WR rising edge	t_{WHQX}			01-03	$t_{OSC}-25$		
				04	$t_{OSC}-30$		
WR rising edge to ALE rising edge 6/	t_{WHLH}			All	$t_{OSC}-10$	$t_{OSC}+15$	
BHE, INST after WR rising edge	t_{WHBX}				$t_{OSC}-10$		
AD8-15 hold after WR rising 7/	t_{WHAX}				$t_{OSC}-50$		
BHE, INST after RD rising edge	t_{RHBX}				$t_{OSC}-10$		
AD8-15 hold after RD rising 7/	t_{RHAX}				$t_{OSC}-25$		
HOLD set-up 8/	t_{HVCH}	See figure 4, HOLD/HLDA timings			55		
CLKOUT low to HLDA low	t_{CLHAL}				-15	15	
CLKOUT low to BREQ low 2/	t_{CLBRL}				-15	15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$ 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
HLDA low to address float	t_{HALAZ}	See figure 4, HOLD/HLDA timings	9,10,11	All		10	
HLDA low to BHE, INST, RD, WR weakly driven	t_{HALBZ}			01-03		10	
				04		15	
CLKOUT low to HLDA high	t_{CLHAH}			All	-15	15	
CLKOUT low to BREQ high 2/	t_{CLBRH}				-15	15	
HLDA high to address no longer float	t_{HAHAX}			01=03	-10		
				04	-15		
HLDA high to BHE, INST, RD, WR valid	t_{HAHBV}			All	-10		
CLKOUT low to ALE high	t_{CLLH}				-5	15	
Oscillator frequency	$1/t_{XLXL}$	See figure 4, External clock drive timings	9, 10, 11	01,02 04	3.5	16	MHz
				03	3.5	20	
Oscillator period	t_{XLXL}			01,02 04	62.5	286	ns
				03	50	286	
High time	t_{XHXX}			01,02 04	22		
				03	17		
Low time	t_{XLXX}			01,02 04	22		
				03	17		
Rise time 2/	t_{XLXH}			All		10	
Fall time 2/	t_{XHXL}					10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$ 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Serial port clock period (BRR≥8002H)	t_{XLXL}	See figure 4, 2/ Serial port waveform shift register mode timings	9,10,11	All	$6t_{OSC}$		ns
Serial port clock falling edge to rising edge (BBR≥8002H)	t_{XLXH}				$4t_{OSC}\pm50$		
Serial port clock period (BBR≥8001H)	t_{XLXL}				$4t_{OSC}$		
Serial port clock falling edge to rising (BRR=8001H)	t_{XLXH}				$2t_{OSC}\pm50$		
Output data set-up to clock rising edge	t_{QVXH}				$2t_{OSC}-50$		
Output data hold after clock rising edge	t_{XHQX}				$2t_{OSC}-50$		
Next output data valid after clock rising edge	t_{XHQV}					$2t_{OSC}+50$	
Input data set-up to clock rising edge	t_{DVXH}				$t_{OSC}+50$		
Input data hold after clock rising edge	t_{XHDX}				0		
Last clock rising to output float	t_{XHQZ}					$1t_{OSC}$	
Resolution		10-bit A/D converter characteristics	4, 5, 6	All	1024	1024	levels
					10	10	bits
Absolute error					0	±8	LSBs
Full scale error					0	±3	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$ 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Zero offset error		10-bit A/D converter characteristics	4, 5, 6	All	0	±3	LSBs
Nonlinearity					0	±8	
Differential nonlinearity error					>-1	+2	
Channel to channel matching					0	+1	
Repeatability		10-bit converter 9/ characteristics				±0.25	
Temperature coefficients: offset, full scale, differential nonlinearity						0.009	LSB/°C
Off isolation		DC to 100 KHz Device 01, 04 only			-60		dB
Feedthrough						-60	
V_{CC} power supply rejection						-60	
Input resistance					750	1.2 k	Ω
DC input leakage					0	3.0	μA
Sample time: prescaler on prescaler off					16 8		states

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$ 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance		10-bit converter 9/ characteristics	4, 5, 6	All		3.0	pH
Resolution		8-bit A/D converter 9/ characteristics			256 8	256 8	Levels bits
Absolute error					0	±2	LSBs
Full scale error					0	±1	
Zero offset error					0	±2	
Nonlinearity					0	±2	
Differential nonlinearity error					>-1	+1	
Channel to channel matching					0	+1	
Repeatability						±0.25	
Temperature coefficients: offset, full scale, differential nonlinearity						0.003	LSB/°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ The following pins are active low: $\overline{AVD}$ of ALE/$\overline{AVD}$, $\overline{BHE}$/$\overline{WRH}$, $\overline{EA}$, $\overline{RD}$, $\overline{RESET}$, $\overline{WR}$/$\overline{WRL}$. QBD (Quasi-bidirectional) pins include Port 1, P2.6, and P2.7. Standard outputs include AD0-15, RD.WR, ALE, BHE, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open drain outputs. Standard inputs include HSI pins, $\overline{EA}$, READY, BUSWIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3, and T2RST/P2.4. Testing performed at 3.5 MHz. However, the device is static by design and will typically operate below 1 Hz. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45 V or V_{OH} is held below V_{CC} -0.7 V:

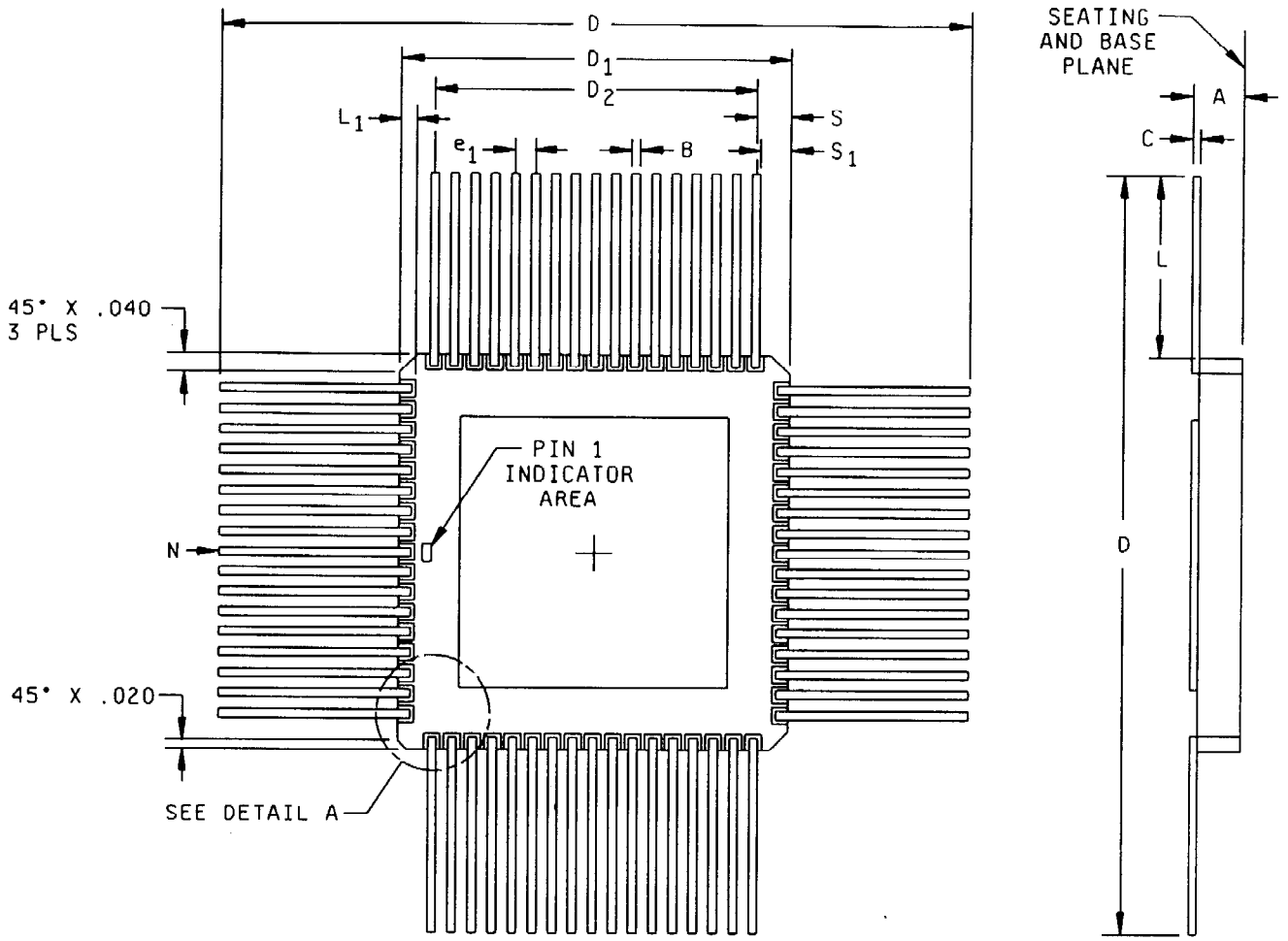
I_{OL} on output pins: 10 mA
I_{OH} on quasi-bidirectional pins: self limiting
I_{OH} on standard output pins: 10 mA

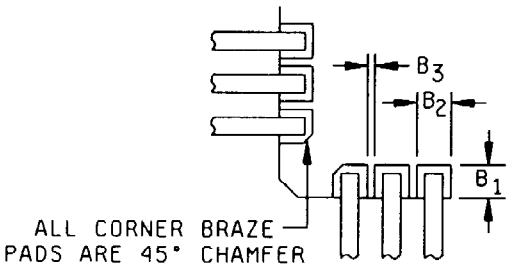
During normal (nontransient) conditions the follow total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, RESET	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, WR, BHE	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0-AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
RD, ALE, INST-CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

Unless otherwise specified, all test conditions shall be worst conditions.
2/ Test initially and at process and design changes. Thereafter guaranteed. If not tested to the limits specified in table I.
3/ Violating these specifications in RESET may cause the part to enter test modes.
4/ If maximum is exceeded, additional wait states will occur.
5/ If wait states are used, add 2 TOSC*N, where N = number of wait states.
6/ Assuming back-to-back bus cycles.
7/ 8-bit bus only.
8/ To guarantee recognition at next clock.
9/ An LSB is rated as approximately 20 mV.

Case Y





DETAIL A

FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90692
		REVISION LEVEL	SHEET 15

Case Y

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.80	0.106	2.03	2.69
B	0.016	0.020	0.41	0.51
B1	0.040	0.060	1.02	1.52
B2	0.030	0.040	0.76	1.02
B3	0.005	0.020	0.13	0.51
C	0.008	0.012	0.20	0.31
D	1.640	1.870	41.66	47.50
D1	0.935	0.424	23.75	24.64
D2	0.800 BSC		20.32 BSC	
e1	0.050 BSC		1.27 BSC	
L	0.375	0.450	9.52	11.43
L1	0.040	0.060	1.02	1.52
N	68		68	
S	0.066	0.087	1.68	2.21
S1	0.050	---	1.27	---

FIGURE 1. Case outline - Continued.

Device types All					
Case outline X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A02	ACH5/P0.5	C11	HS0.1	I10	$\overline{WR}/WRL$
A03	ANGND	D01	ACH1/P0.1	I11	$\overline{BHE}/WRH$
A04	V_{SS}	D02	ACH3/P0.3	J01	$\overline{RD}$
A05	$\overline{RESET}$	D10	P1.5	J02	AD1/P3.1
A06	TXD/P2.0	D11	P1.6	J03	AD3/P3.3
A07	P1.1	E01	NMI	J04	AD5/P3.5
A08	P1.3	E02	$\overline{EA}$	J05	AD7/P3.7
A09	HSI.0	E10	P1.7	J06	AD9/P4.1
A10	HS0.4/HSI.2	E11	T2UP-DN/P2.6	J07	AD11/P4.3
B01	ACH7/P0.7	F01	V_{CC}	J08	AD13/P4.5
B02	ACH6/P0.6	F02	V_{SS}	J09	AD15/P4.7
B03	ACH4/P0.4	F10	HS0.2	J10	T2RST/P2.4/$\overline{AINC}$
B04	V_{REF}	F11	HS0.3	J11	READY
B05	EXTINT/P2.2	G01	XTAL1	K02	AD0/P3.0
B06	RXD/P2.1	G02	XTAL2	K03	AD2/P3.2
B07	P1.0	G10	V_{SS}	K04	AD4/P3.4
B08	P1.2	G11	V_{PP}	K05	AD6/P3.6
B09	P1.4	H01	CLKOUT	K06	AD8/P4.0
B10	HSI.1	H02	BUSWIDTH	K07	AD10/P4.2
B11	HS0.5/HSI.3	H10	T2CAPTURE/P2.7/$\overline{PACT}$	K08	AD12/P4.4
C01	ACH2/P0.2	H11	PWM/P2.5	K09	AD14/P4.6
C02	ACH0/P0.0	I01	INST	K10	T2CLK/P2.3
C10	HS0.0	I02	ALE/$\overline{ADV}$		

FIGURE 2. Terminal connections.

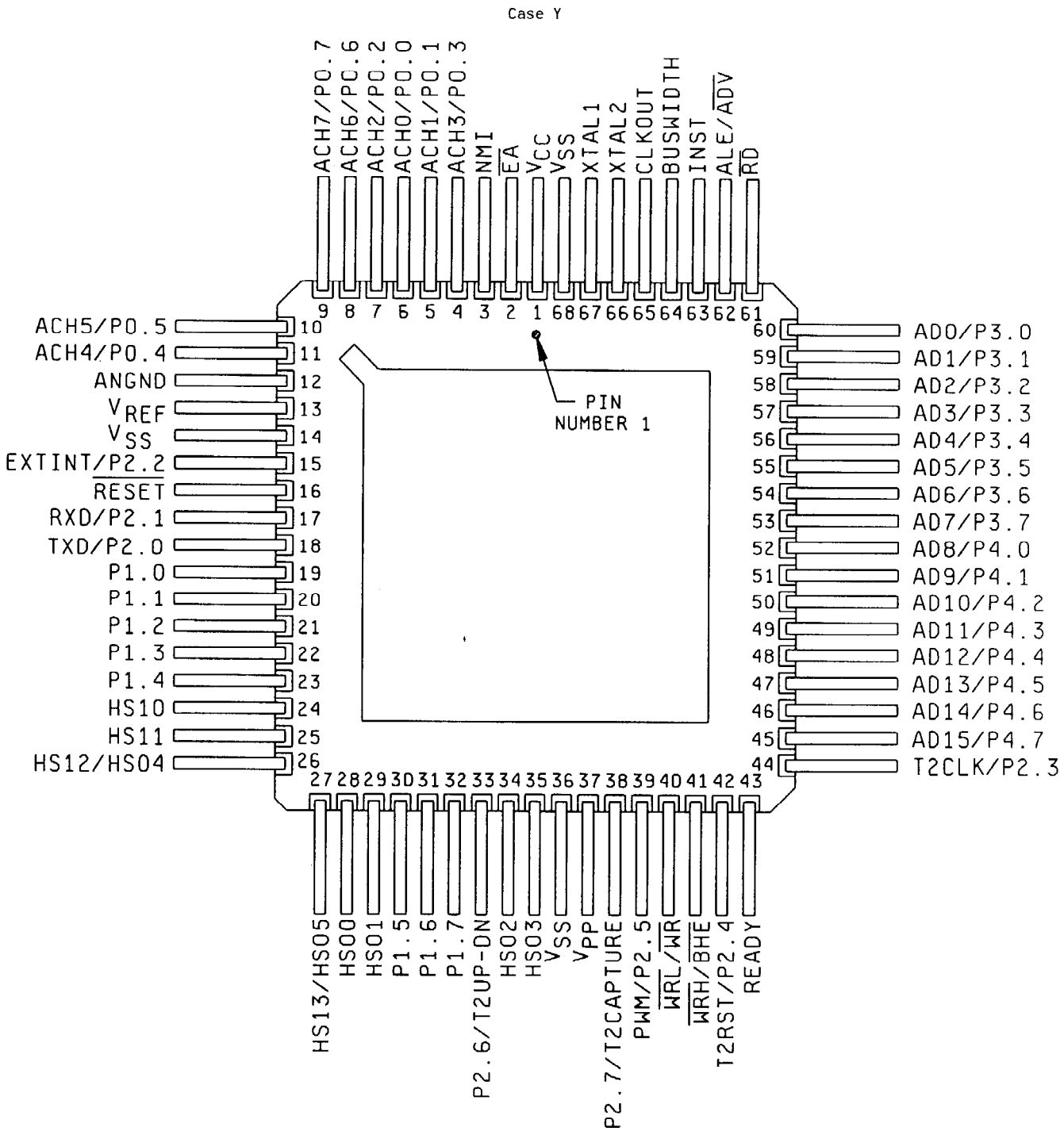


FIGURE 2. Terminal connections - Continued.

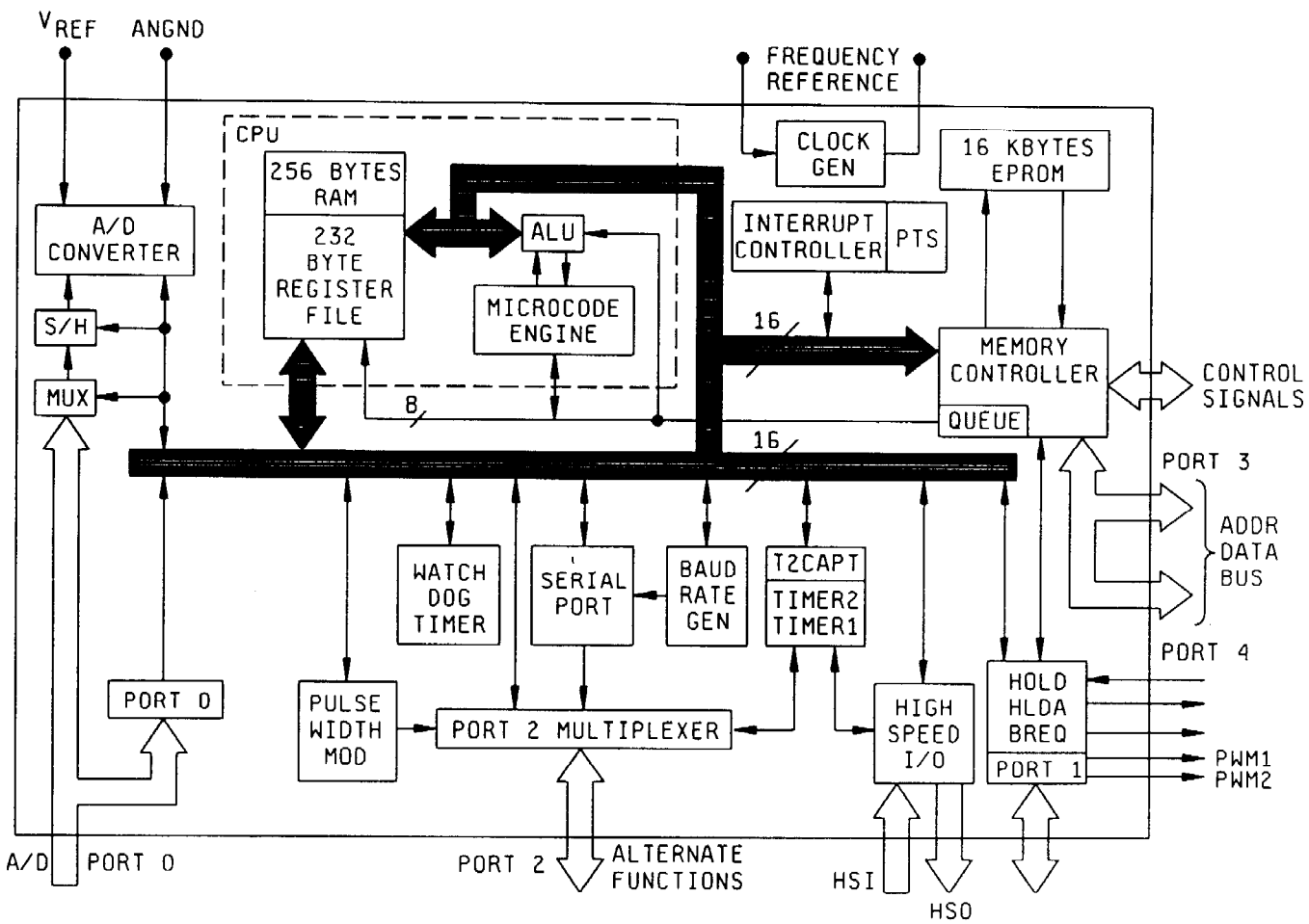


FIGURE 3. Functional block diagram.

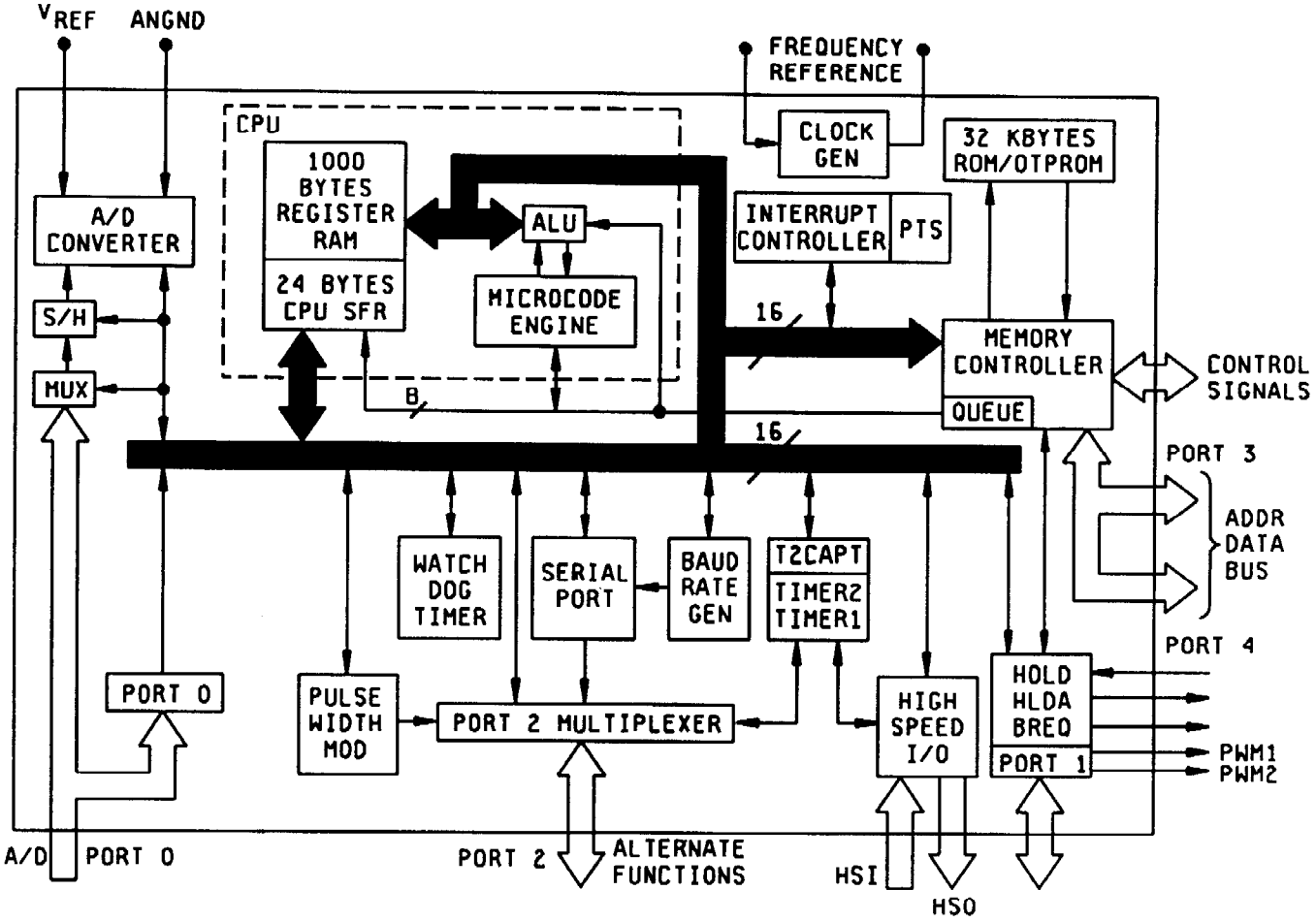


FIGURE 3. Functional block diagram - Continued.

System bus timings

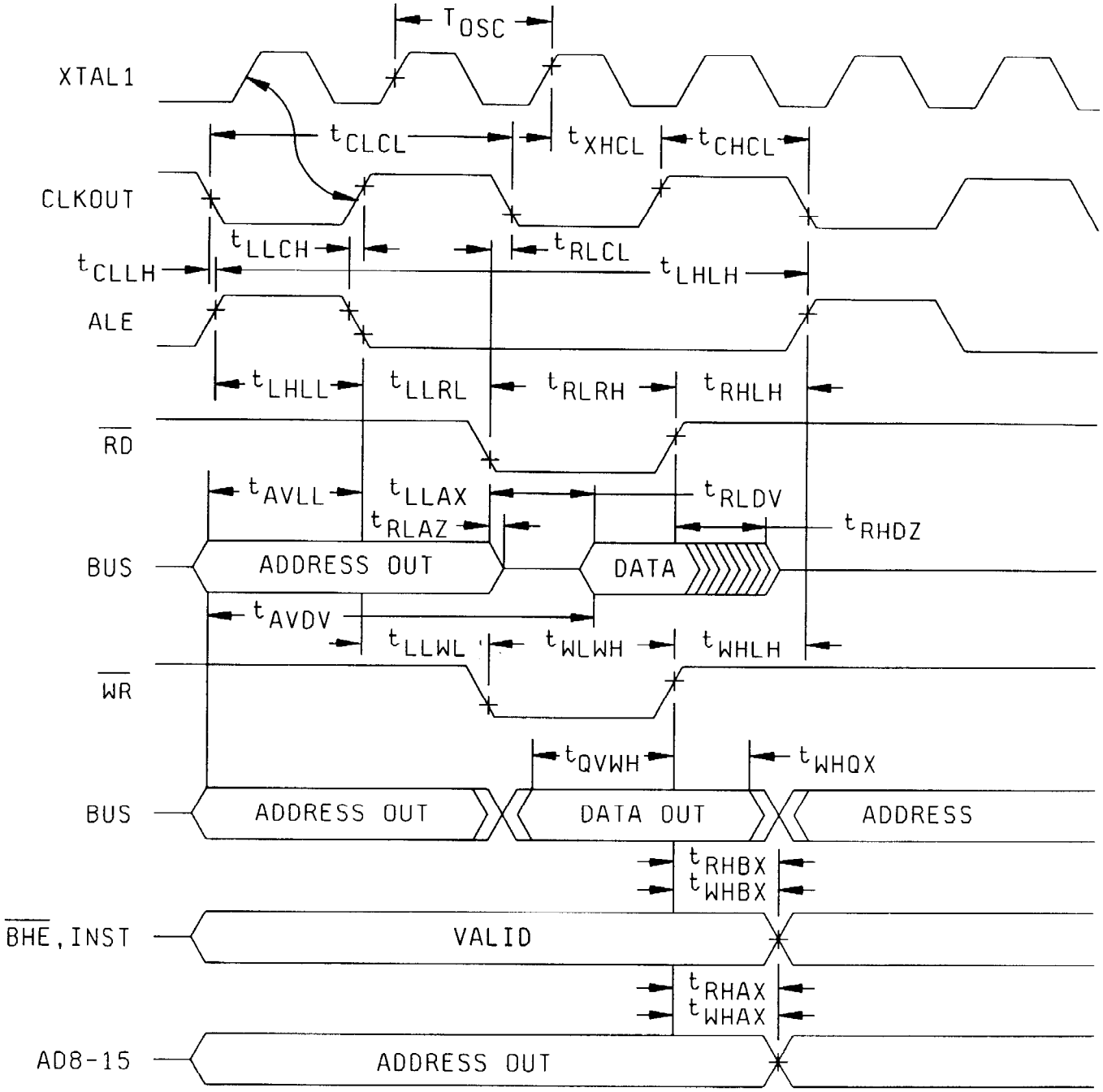
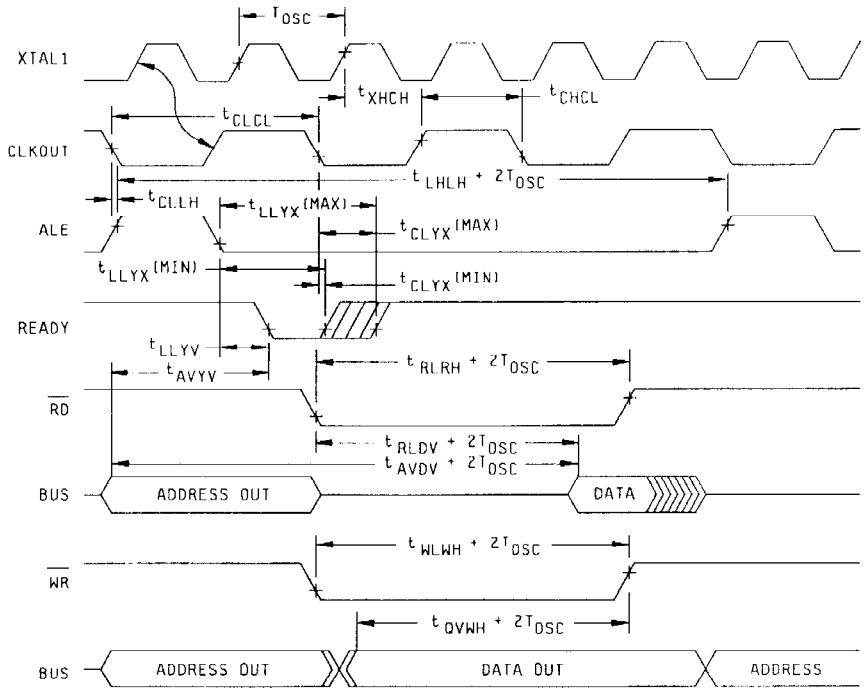


FIGURE 4. Test circuit and switching waveforms.

Ready timings (one waitstate)



Buswidth timings

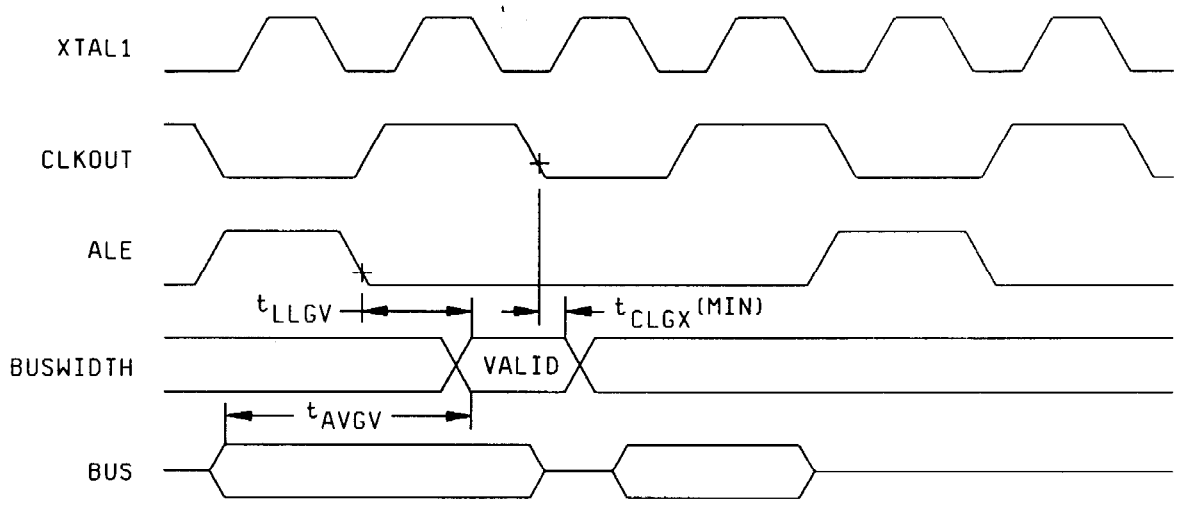
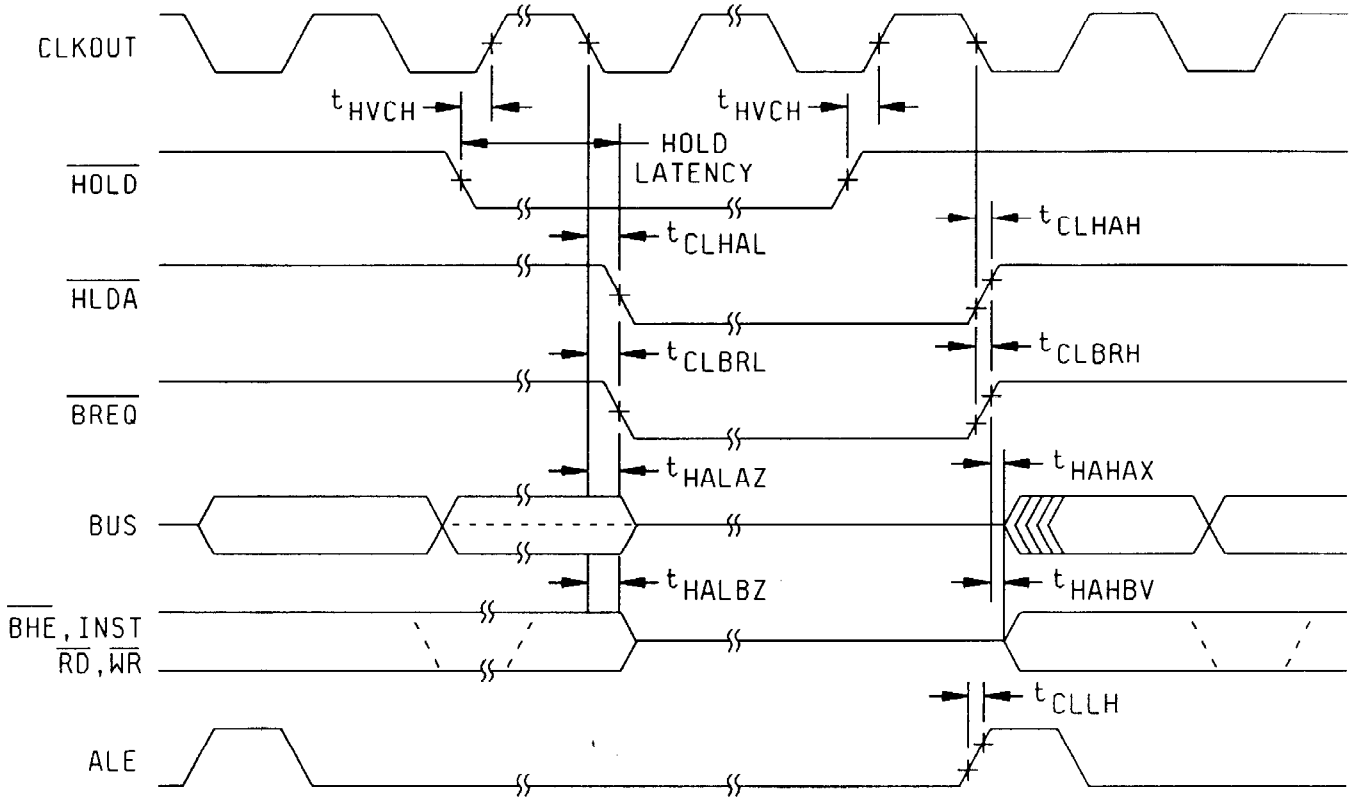


FIGURE 4. Test circuit and switching waveforms - Continued.

HOLD/HLDA timings



External clock driven waveforms

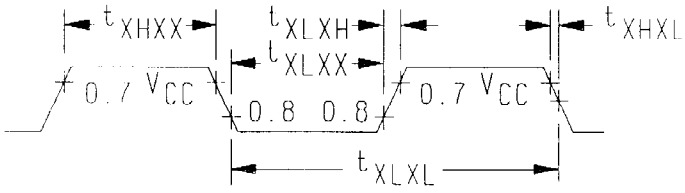
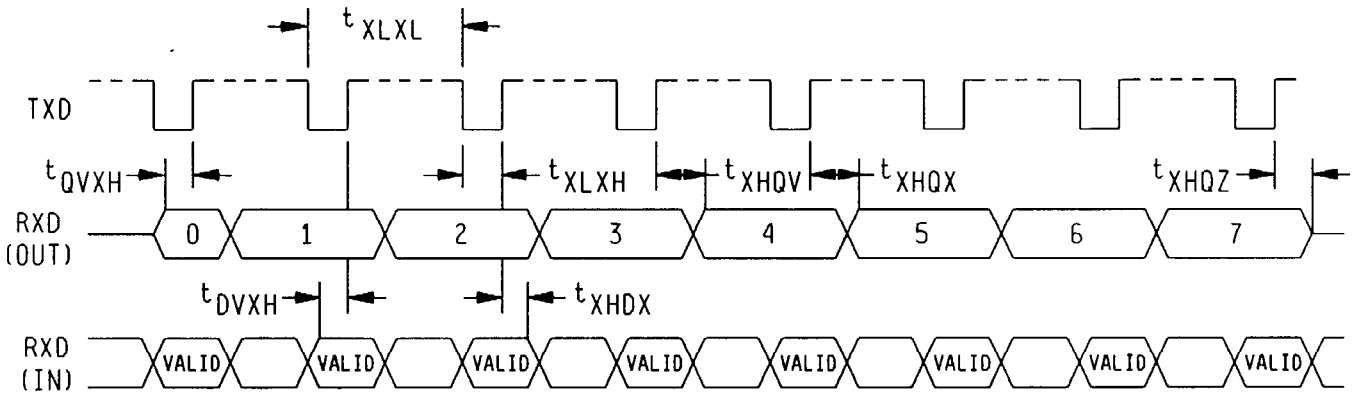


FIGURE 4. Test circuit and switching waveforms - Continued.

Serial port waveform - shift register mode



A.C. testing input, output waveform

Float waveform

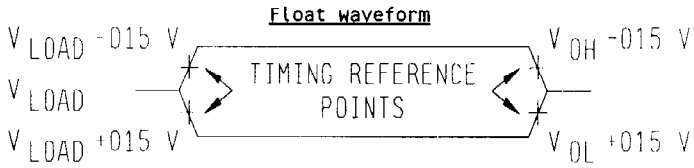
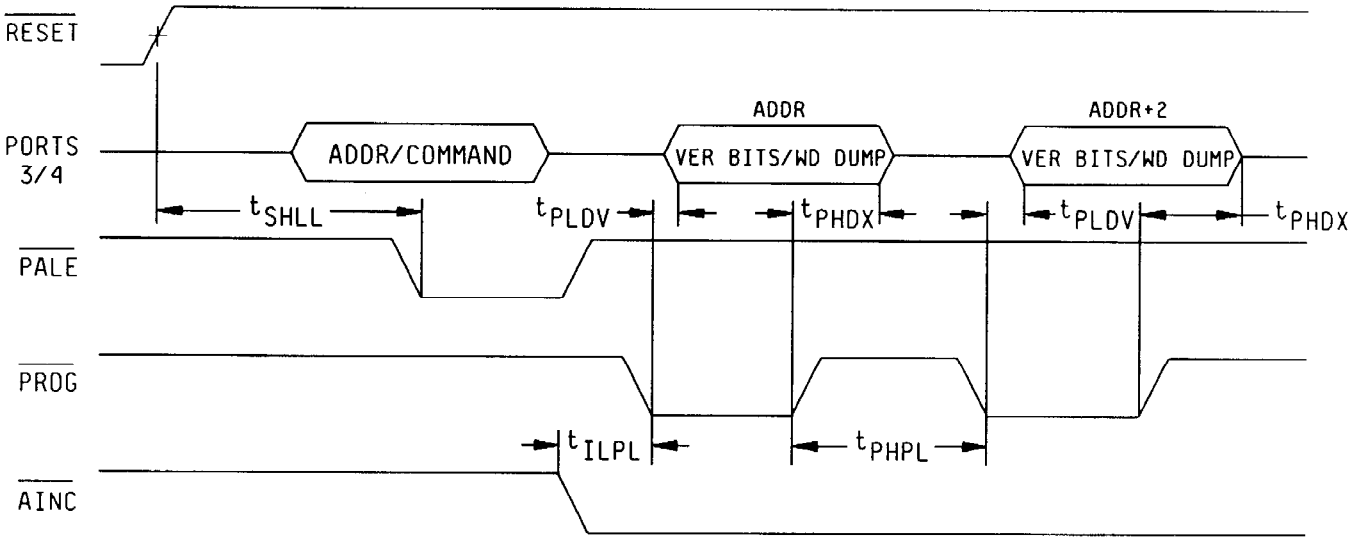


FIGURE 4. Test circuit and switching waveforms - Continued.

Slave program mode in word dump with auto increment



Slave programming mode data program mode with single program pulse

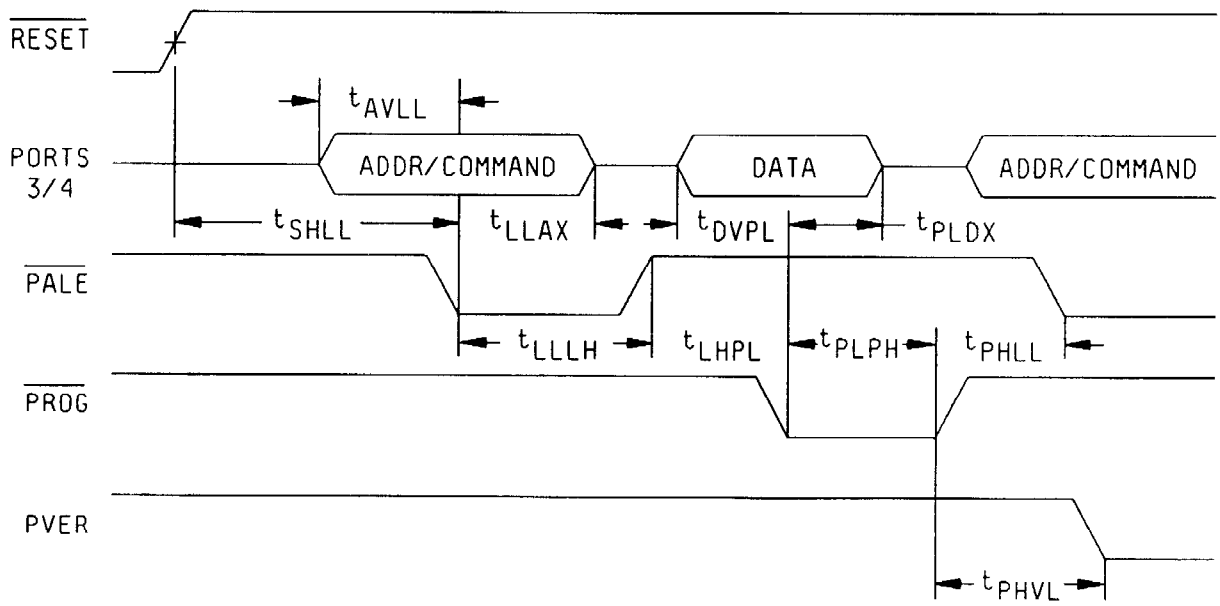
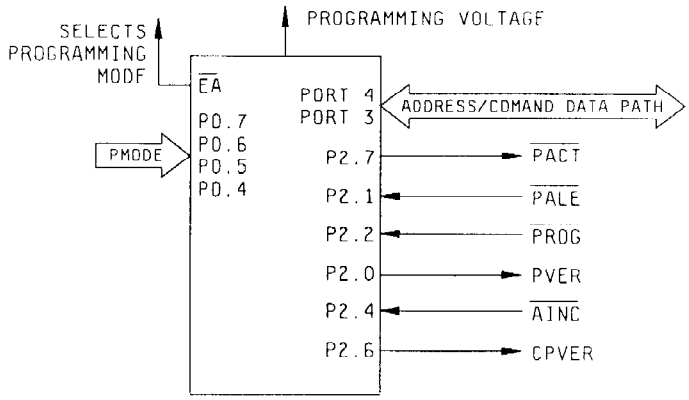


FIGURE 5. EPROM programming configuration waveforms.

Programming and verification configuration



Slave programming mode timing in data program with repeated PROG pulse and auto increment

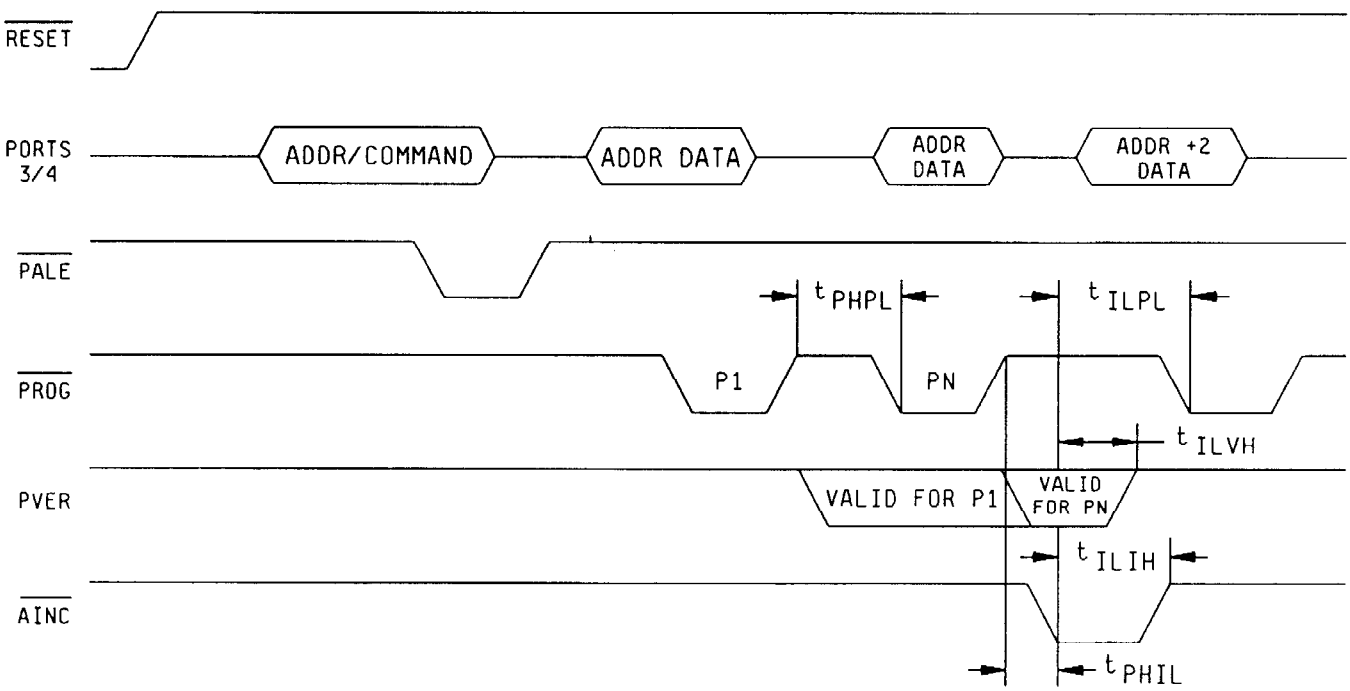


FIGURE 5. EPROM programming configuration waveforms - Continued.

3.11.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6 and table III.

3.12.3 Verification of erasure programmability of EPROMS. When specified, devices shall be verified as either programmed to the specification pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.11.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using V_M = +5.9 V at +25°C using loose timing (i.e., T_{ACC} > 1 µs).

(4) Perform dynamic burn-in (see 4.2.1a).

(5) Margin at V_M = 5.9 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.11.1), except devices submitted for groups A, B, C and D testing.

(8) Verify erasure (see 3.11.3).

Margin test method B.

(1) Program at +25°C, 100 percent of the bits.

(2) Bake, unbiased, for 24 hours at +250°C.

(3) Perform margin test at V_M = 5.9 V.

(4) Erase (see 3.11.1).

(5) Perform interim electrical tests in accordance with table II.

(6) Program 100 percent of the bits and verify (see 3.11.3).

(7) Perform burn-in (see 4.2.1a).

(8) One-hundred percent test at +25°C (group A, subgroups 1 and 7). V_M = 5.9 V with loose timing, apply PDA.

(9) Perform remaining final electrical subgroups and group A testing.

(10) Erase, devices may be submitted for groups B, C, and D at this time.

(11) Verify erasure (see 3.11.3). Steps 1 through 4 are performed at wafer level.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall consist of verifying the EPROM pattern specified and the instruction set. The instruction set forms a part of the vendors test tape and shall be maintained and available from the approved source of supply. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_S and C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. All devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased an verified (except devices submitted for groups C and D testing).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1, 7
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 1/	1, 2, 3, 4, 5, 6 7, 8, 9, 10, 1/ 11	1, 2, 3, 4, 5, 6, 7, 2/ 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 5, 7, 8, 10
Group D end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 5, 7,8, 10
Group E end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 5, 8, 10

1/ PDA applies to subgroup 1. (I_{CC} only)
2/ PDA applies to subgroups 1 and 7.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Erasing procedure. The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 W/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

4.6 Programming procedures. The programming characteristics in table III and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration (see figure 5) for programming. The waveforms of figure 5 and programming characteristics of table III shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to and "H" by ultraviolet light erasure (see 4.5).

TABLE III. Programming characteristics

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Reset high to first PALE low	t_{SHLL}	EPROM programming and verification characteristics Load capacity = 150 pF V_{CC}, V_{REF} = 5 V V_{SS}, ANGND = 0 V V_{PP} = 12.5 V ± 0.25 V $\overline{EA}$ = 12.5 V ± 0.25 V T_A = +25°C ± 5°C See figure 5 1/		All	1100 t_{OSC}		ns
PALE pulse width	t_{LLLH}			All	50 t_{OSC}		ns
Address setup time	t_{AVLL}			All	0		ns
Address hold time	t_{LLAX}			All	100 t_{OSC}		ns
PROG low to word dump valid	t_{PLDV}			All		50 t_{OSC}	ns
Word dump data hold	t_{PHDX}			All		50 t_{OSC}	ns
Data setup time	t_{DVPL}			All	0		ns
Data hold time	t_{PLDX}			All	400 t_{OSC}		ns
PROG pulse width 2/	t_{PLPH}			All	50 t_{OSC}		ns
PROG high to next PALE low	t_{PHLL}			All	220 t_{OSC}		ns
PALE high to PROG low	t_{LHPL}			All	220 t_{OSC}		ns
PROG high to next PROG low	t_{PHPL}			All	220 t_{OSC}		ns
PROG high to AINC low	t_{PHIL}			All	0		ns

TABLE III. Programming characteristics

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AINC pulse width	t_{ILIH}	EPROM programming and verification characteristics Load capacity = 150 pF V_{CC}, V_{REF} = 5 V V_{SS}, ANGND = 0 V V_{PP} = 12.5 V ± 0.25 V EA = 12.5 V ± 0.25 V T_A = +25°C ± 5°C See figure 5 1/		All	240 t_{OSC}		ns
PVER hold after AINC low	t_{ILVH}			All	50 t_{OSC}		ns
AINC low to PROG low	t_{ILPL}			All	170 t_{OSC}		ns
PROG high to PVER low	t_{PHVL}			All		220 t_{OSC}	ns
VPP supply current when	I_{PP}			All		100	mA

1/ AINC = Auto increment
2/ This specification is for Word Dump Mode. For programming pulses, use 300 T_{OSC} + 100 μs.
3/ Tested initially and at process and design changes. Thereafter guaranteed, if not tested, to the limits specified in table III.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and as follows:

Pin symbol	Description
ACH1 thru ACH7	Analog channel
AD0 thru AD15	Address/data pins
ALE/$\overline{\text{ADV}}$	Address latch enable or address valid output, as selected by CCR. Both pin options provide a signal to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$ it goes inactive high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
ANGND	References ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus high enable or write high output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte of the data bus. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 =0, $\overline{\text{BHE}}$ = 1), to the high byte only (A0 = 1, $\overline{\text{BHE}}$ = 0), or both bytes (A0 = 0, $\overline{\text{BHE}}$ = 0). If the $\overline{\text{WRH}}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is valid only during 16-bit external memory write cycles.
$\overline{\text{BREQ}}$	Bus request output activatied when the bus controller has a pending external memory cycle.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1 an 16-bit cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is 1/2 the oscillator frequency. For device type 02, CLKOUT may be disabled.
$\overline{\text{EA}}$	Input for memory select (External access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 5FFFH to be directed to on-chip EPROM. EA equal to a TTL-low causes accesses to those locations to be directed to off-chip memory.
EXTINT	External interrupt.
$\overline{\text{HLDA}}$	Bus-hold acknowledge output indicating release of the bus.
$\overline{\text{HOLD}}$	Bus-hold input requesting control of the bus.
HSI.0 through HSI.3	Inputs to high speed input unit. HSI.2 and HSI.3 are shared with the HSO unit.
HSI.0 through HSI.5	Outputs from high speed input unit. HSI.4 and HSI.5 are shared with the HSI unit.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
NMI	A positive transition causes a vector through 203EH.
$\overline{\text{PACT}}$	Programming active. Used in the auto programming mode to indicate when programming activity is complete.
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port.

Pin symbol	Description - Continued.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in device 01.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pull-ups.
PWM0 through PWM2	Pulse width modulator.
$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads.
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. When the external memory is not being used, READY has no effect.
$\overline{RESET}$	Reset input to the chip.
RXD	Serial port receive.
TXD	Serial port transmit.
T2CAPTURE	Timer 2 capture enable.
T2CLK	Timer 2 clock source.
T2RST	Timer 2 reset source.
T2UP-DN	Timer 2 count up or down.
V_{CC}	Main supply voltage (5.0).
V_{PP}	Timing pin for the return from powerdown circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 M Ohm resistor to V_{CC}. If this function is not used V_{PP} may be tied to V_{CC}. This pin is the programmming voltage on the EPROM device.
V_{REF}	Reference voltage for the A/D converter (5.0). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
V_{SS}	Digital circuit ground (0.0 V). There are three V_{SS} pins, all of which must be connected.
$\overline{WR}/\overline{WRL}$	Write and write low ouput to external memory, as selected by the CCR. $\overline{WR}$ will go low for every external write. while WRL will go low only for external writes where an even byte is being written. $\overline{WR}$/WRL is activated only during external memory writes.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-02-07

Approved sources of supply for SMD 5962-90692 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9069201MXA	34649	MG87C196KC
5962-9069201MYA	34649	MQ87C196KC
5962-9069202QXA	34649	MG87C196KD16
5962-9069202QYA	34649	MQ87C196KD16
5962-9069203QXA	34649	MG87C196KD20
5962-9069203QYA	34649	MQ87C196KD20
5962-9069204QXA	34649	MG87C196KC
5962-9069204QYA	34649	MQ87C196KC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation Robert Noyce Building FS001 2200 Mission College Blvd PO Box 58119 Santa Clara CA 95052-8119 Point of contact: 5000 W Chandler Boulevard Chandler AZ 85226