

## 54AC377 • 54ACT377 Octal D Flip-Flop with Clock Enable

### General Description

The 'AC/'ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ( $\overline{CE}$ ) is LOW.

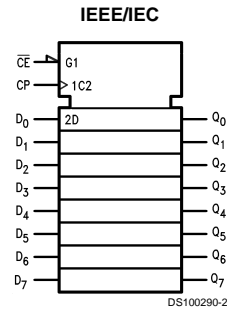
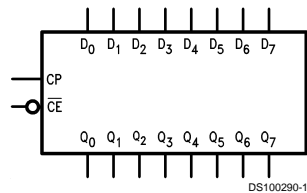
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The  $\overline{CE}$  input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

### Features

- $I_{CC}$  reduced by 50%

- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See '273 for master reset version
- See '373 for transparent latch version
- See '374 for TRI-STATE® version
- 'ACT377 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
  - 'AC377: 5962-88702
  - 'ACT377: 5962-87697

### Logic Symbols

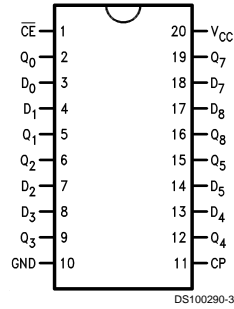


Pin Names	Description
D <sub>0</sub> –D <sub>7</sub>	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q <sub>0</sub> –Q <sub>7</sub>	Data Outputs
CP	Clock Pulse Input

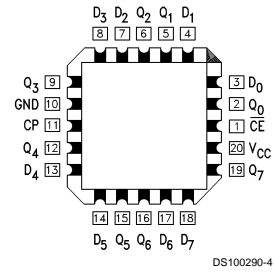
TRI-STATE® is a registered trademark of National Semiconductor Corporation.  
FACT® is a registered trademark of Fairchild Semiconductor Corporation.

## Connection Diagrams

Pin Assignment  
for DIP and Flatpak



Pin Assignment  
for LCC

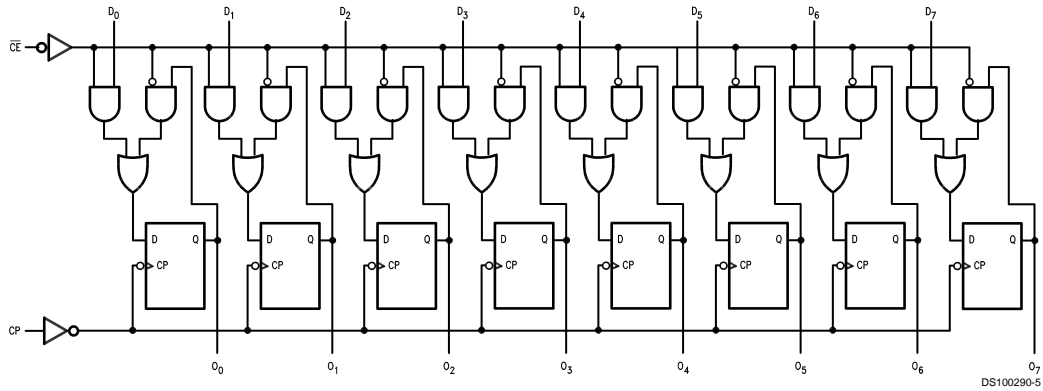


## Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	$D_n$	$Q_n$
Load '1'	↗	L	H	H
Load '0'	↗	L	L	L
Hold (Do Nothing)	↗	H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
↗ = LOW-to-HIGH Clock Transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
CDIP	175°C

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'AC Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

**Note 2:** See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

## DC Characteristics for 'AC Family Devices

Symbol	Parameter	$V_{CC}$ (V)	54AC	Units	Conditions	
			$T_A =$ -55°C to +125°C			
			Guaranteed Limits			
$V_{IH}$	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	3.15			
		5.5	3.85			
$V_{IL}$	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	1.35			
		5.5	1.65			
$V_{OH}$	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.4			
		5.5	5.4			
			3.0	2.4	V	(Note 3) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
			4.5	3.7		
			5.5	4.7		
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.1			
		5.5	0.1			
			3.0	0.50	V	(Note 3) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
			4.5	0.50		
			5.5	0.50		
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}, GND$	

### DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	54AC	Units	Conditions
			T <sub>A</sub> = -55°C to +125°C		
			Guaranteed Limits		
I <sub>OLD</sub>	(Note 4) Minimum Dynamic Output Current	5.5	50	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>		5.5	-50	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0	µA	V <sub>IN</sub> = V <sub>CC</sub> or GND

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:** I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

### DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	54ACT	Units	Conditions
			T <sub>A</sub> = -55°C to +125°C		
			Guaranteed Limits		
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	2.0		
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	0.8		
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.4	V	I <sub>OUT</sub> = -50 µA
		5.5	5.4		
		4.5	3.70	V	(Note 6) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA
		5.5	4.70		
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.1	V	I <sub>OUT</sub> = 50 µA
		5.5	0.1		
		4.5	0.50	V	(Note 6) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA
		5.5	0.50		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	±1.0	µA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	1.6	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	(Note 7) Minimum Dynamic Output Current	5.5	50	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>		5.5	-50	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0	µA	V <sub>IN</sub> = V <sub>CC</sub> or GND

**Note 6:** \*All outputs loaded; thresholds on input associated with output under test.

**Note 7:** †Maximum test duration 2.0 ms, one output loaded at a time.

**Note 8:** I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

### AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	54AC		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	3.3 5.0	75 95		MHz	
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub>	3.3 5.0	1.0 1.5	14.0 10.0	ns	
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>	3.3 5.0	1.0 1.5	15.0 11.0	ns	

**Note 9:** Voltage Range 3.3 is 3.3V ±0.3V  
Voltage Range 5.0 is 5.0V ±0.5V

### AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> (V) (Note 10)	54AC		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	3.3 5.0	7.5 6.0		ns	
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	3.3 5.0	1.5 2.5		ns	
t <sub>s</sub>	Setup Time, HIGH or LOW $\overline{CE}$ to CP	3.3 5.0	9.5 6.0		ns	
t <sub>h</sub>	Hold Time, HIGH or LOW $\overline{CE}$ to CP	3.3 5.0	1.0 2.0		ns	
t <sub>w</sub>	CP Pulse Width HIGH or LOW	3.3 5.0	6.5 5.0		ns	

**Note 10:** Voltage Range 3.3 is 3.0V ±0.3V  
Voltage Range 5.0 is 5.0V ±0.5V

### AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 11)	54ACT		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	5.0	85		MHz	
t <sub>PLH</sub>	Propagation Delay CP to Q <sub>n</sub>	5.0	1.5	11.0	ns	
t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>	5.0	1.5	12.0	ns	

**Note 11:** Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements

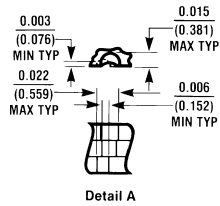
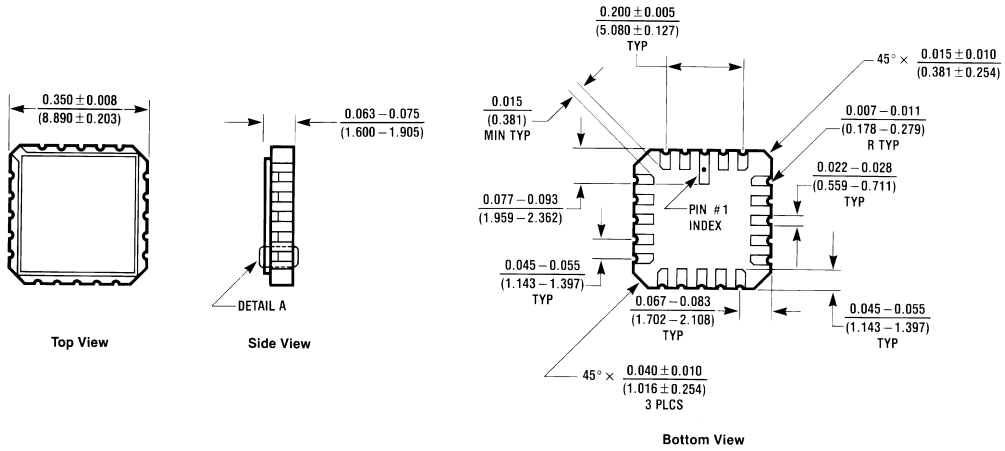
Symbol	Parameter	V <sub>CC</sub> (V) (Note 12)	54ACT	Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		
			Guaranteed Minimum		
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	5.0	7.0	ns	
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	1.0	ns	
t <sub>s</sub>	Setup Time, HIGH or LOW CE to CP	5.0	7.0	ns	
t <sub>h</sub>	Hold Time, HIGH or LOW CE to CP	5.0	1.0	ns	
t <sub>w</sub>	CP Pulse Width HIGH or LOW	5.0	5.5	ns	

**Note 12:** Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

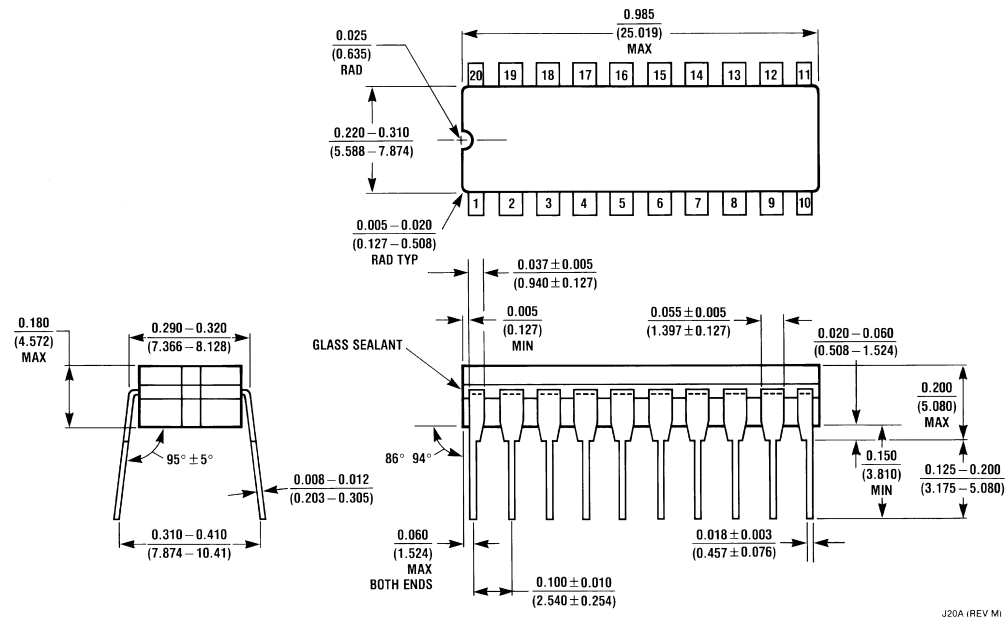
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	90.0	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20 Terminal Ceramic Leadless Chip Carrier (L)**  
 NS Package Number E20A

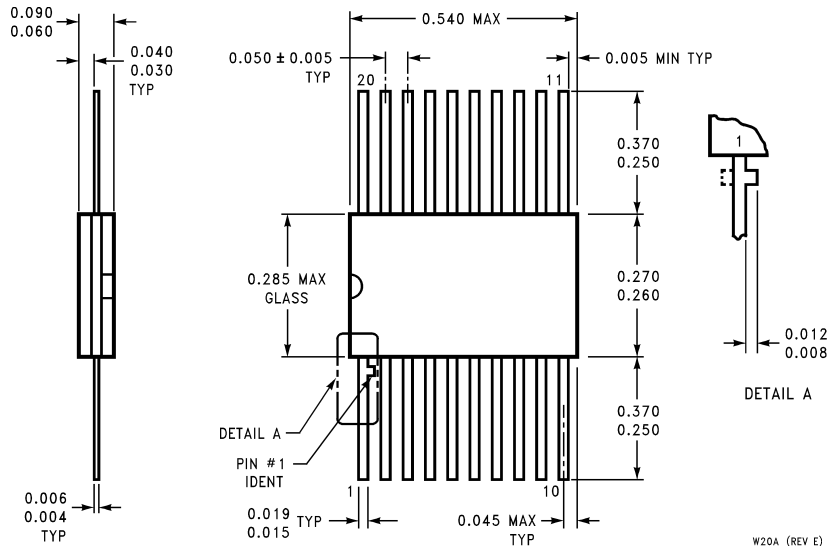
E20A (REV D)



**20 Lead Ceramic Dual-In-Line Package (D)**  
 NS Package Number J20A

J20A (REV M)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20 Lead Ceramic Flatpak (F)  
NS Package Number W20A**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com

**National Semiconductor Europe**  
Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 1 80-530 85 85  
English Tel: +49 (0) 1 80-532 78 32  
Français Tel: +49 (0) 1 80-532 93 58  
Italiano Tel: +49 (0) 1 80-534 16 80

**National Semiconductor Asia Pacific Customer Response Group**  
Tel: 65-2544466  
Fax: 65-2504466  
Email: sea.support@nsc.com

**National Semiconductor Japan Ltd.**  
Tel: 81-3-5639-7560  
Fax: 81-3-5639-7507

www.national.com



[See Die Products](#)[Products](#) > [Military/Aerospace](#) > [Logic](#) > [FACT AC](#) > [54AC377](#)

# 54AC377 Product Folder

## Octal D Flip-Flop with Clock Enable

[General Description](#)[Features](#)[Datasheet](#)[Package & Models](#)[Samples & Pricing](#)

### Datasheet

Title	Size in Kbytes	Date	<a href="#">View Online</a>	<a href="#">Download</a>	<a href="#">Receive via Email</a>
54AC377 54ACT377 Octal D Flip-Flop with Clock Enable	177 Kbytes	2-Feb-99	<a href="#">View Online</a>	<a href="#">Download</a>	<a href="#">Receive via Email</a>
54AC377 Mil-Aero Datasheet MN54AC377-X	15 Kbytes		<a href="#">View Online</a>	<a href="#">Download</a>	<a href="#">Receive via Email</a>

If you have trouble printing or viewing PDF file(s), see [Printing Problems](#).

### Package Availability, Models, Samples & Pricing

Part Number	Package			Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size	<a href="#">Package Marking</a>
	Type	Pins	MSL		SPICE	IBIS		Qty	\$US each		
5962-88702012A (54AC377LMQB)	<a href="#">LCC</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A	<a href="#">Buy Now</a>	50+	\$11.0000	rail of 50	[logo]cZcSc4cA 54AC377 LMQB /QcMSE 5962- 88702012A
5962-8870201RA (54AC377DMQB)	<a href="#">CERDIP</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A	<a href="#">Buy Now</a>	50+	\$8.6000	rail of 20	[logo]cZcSc4cASE 54AC377DMQB /QcM 5962-8870201RA
5962-8870201SA (54AC377FMQB)	<a href="#">CERPACK</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$11.0000	rail of 19	[logo]cZcSc4cASE 54AC377FMQB QcM 5962- 8870201SA
JM54AC377B2A-RH	<a href="#">LCC</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A				rail of N/A	[logo] JM38510 R75603B2A 27014 QS cZcSc4cASE
JM38510/75603B2	<a href="#">LCC</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$13.6000	rail of 50	[logo] JM38510 /75603B2A 27014 QS cZcSc4cASE
JM54AC377BRA-RH	<a href="#">CERDIP</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A				rail of N/A	[logo]cZcSc4cASE JM38510R75603BRA 27014 QS

JM38510/75603BS	<a href="#">CERPACK</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$13.6000	rail of 19	[logo]cZcSc4cASE JM38510/75603BSA 27014 QS
R75603BSA	<a href="#">CERPACK</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$73.0000	rail of 19	[logo]cZcSc4cASE JM38510R 75603BSA 27014 QS
JM54AC377S2A-RH	<a href="#">LCC</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A				rail of N/A	[logo]cZcSc4cA 27014 QSE JM38510R 75603S2A
JM54AC377SRA-RH	<a href="#">CERDIP</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A				rail of N/A	[logo]cZcSc4cASE JM38510R75603SRA 27014 Q
RM54AC377SSA	<a href="#">CERPACK</a>	20	<a href="#">MSL</a>	Preliminary	N/A	N/A				rail of N/A	[logo]cZcSc4cASE RM54AC377 SSA WAFER # cR
JM38510/75603SS	<a href="#">CERPACK</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$138.0000	rail of 19	[logo]cZcSc4cASE 27014 JM38510/75603SSA Q
JM38510R75603SS	<a href="#">CERPACK</a>	20	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$138.0000	rail of 19	[logo]cZcSc4cASE 27014 JM38510R 75603SSA Q

## General Description

The 'AC/'ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (CE#) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The CE# input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

## Features

- I<sub>CC</sub> reduced by 50%
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See '273 for master reset version
- See '373 for transparent latch version
- See '374 for TRI-STATE version
- 'ACT377 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD) -'AC377: 5962-88702 -'ACT377: 5962-87697

[Information as of 5-Aug-2002]

[Search](#)

[Design](#)

[Purchasing](#)

[Quality](#)

[Company](#)

[Home](#)

[About Languages](#) . [Website Guide](#) . [About "Cookies"](#) . National is [QS 9000 Certified](#) . [Privacy/Security Statement](#) .

[Contact Us](#) . [Site Terms & Conditions of Use](#) . Copyright 2002 © National Semiconductor Corporation . [My Preferences](#) .

[Feedback](#)