STANDARD MICROSYSTEMS CORPORATION

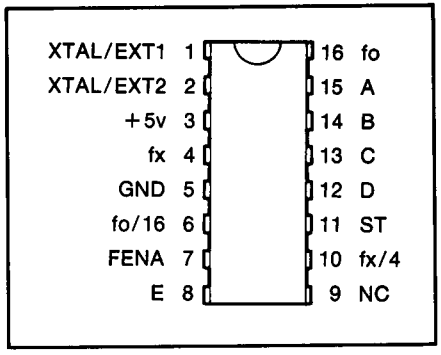
COM 8046
COM 8046T

Baud Rate Generator
Programmable Divider

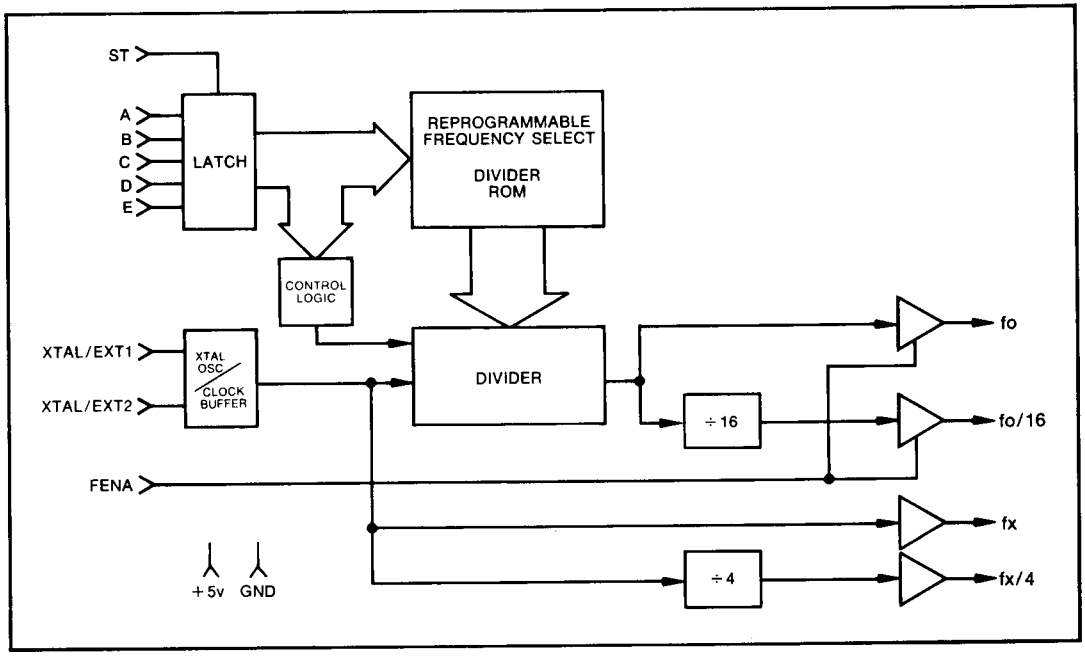
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 32 output frequencies
- ☐ 32 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatible
- ☐ 1X Clock via fo/16 output
- ☐ Crystal frequency output via fx and fx/4 outputs
- ☐ Output disable via FENA

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The Standard Microsystems COM 8046 is an enhanced version of the COM 5046 Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8046 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 1X, 16X and 32X UART/USRT/ASTRO/USYNRT devices.

The COM 8046 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 2. Parts suitable for use only with an external TTL reference are marked COM 8046T. TTL outputs used to drive the COM 8046 or COM 8046T should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The reference frequency (fx) is used to provide two high frequency outputs: one at fx and the other at fx/4. The fx/4 output will drive one standard 7400 load, while the fx output will drive two 74LS loads.

The output of the oscillator/buffer is applied to the divider for generation of the output frequency f_O. The divider is capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period. The output of the divider is also divided internally by 16 and made available at the $f_O/16$ output pin. The $f_O/16$ output will drive one and the f_O output will drive two standard 7400 TTL loads. Both the f_O and $f_O/16$ outputs can be disabled by supplying a low logic level to the FENA input pin. Note that the FENA input has an internal pull-up which will cause the pin to rise to approximately V_{CC} if left unconnected.

The divisor ROM contains 32 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology. This process permits reduction of turn-around-time for ROM patterns.

The five divisor select bits are held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the five divisor select bits; strobe activity is not required. This feature may be disabled through a CLASP® programming option causing new frequency initiation to be delayed until the end of the current f_O half-cycle All five data inputs have pull-ups identical to that of the FENA input, while the strobe input has no pull-up.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt supply
4	f_x	f_x	Crystal/clock frequency reference output
5	GND	Ground	Ground
6	$f_O/16$	$f_O/16$	1X clock output
7	FENA	Enable	A low level at this input causes the f_O and $f_O/16$ outputs to be held high. An open or a high level at the FENA input enables the f_O and $f_O/16$ outputs.
8	E	E	Most significant divisor select data bit. An open at this input is equivalent to a logic high.
9	NC	NC	No connection
10	$f_x/4$	$f_x/4$	¼ crystal/clock frequency reference output.
11	ST	Strobe	Divisor select data strobe. Data is sampled when this input is high, preserved when this input is low.
12-15	D,C,B,A	D,C,B,A	Divisor select data bits. A=LSB. An open circuit at these inputs is equivalent to a logic high.
16	f_O	f_O	16X clock output

For electrical characteristics, see page 281.