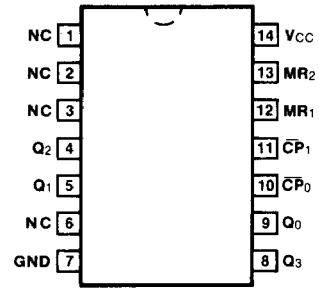
54/74293 54LS/74LS293

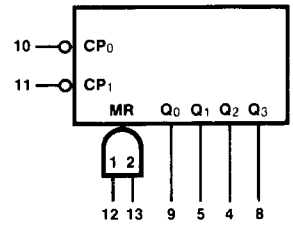
MODULO-16 BINARY COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '293 is a 4-stage ripple counter containing a high speed flip-flop acting as a divide-by-two and three flip-flops acting as a divide-by-eight. HIGH signals on the Master Reset (MR) inputs override the clocks and force all outputs to the LOW state. The '293 is the same circuit as the '93 except that it has corner power pins and is therefore recommended for new designs. For detail specifications, truth tables and functional description, please refer to the '93 data sheet.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 1, 2, 3, 6

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74293PC, 74LS293PC		9A
Ceramic DIP (D)	A	74293DC, 74LS293DC	54293DM, 54LS293DM	6A
Flatpak (F)	A	74293FC, 74LS293FC	54293FM, 54LS293FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP}_0$	÷2 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/1.5
$\overline{CP}_1$	÷8 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/1.0
MR_1, MR_2	Asynchronous Master Reset Inputs (Active HIGH)	1.0/1.0	0.5/0.25
Q_0	÷2 Flip-flop Output*	20/10	10/5.0 (2.5)
Q_1 — Q_3	÷8 Flip-flop Outputs	20/10	10/5.0 (2.5)

*The Q_0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP}_1$ input.