

DATA SHEET

74ABT16373B

16-bit transparent latch (3-State)

Product data

2004 Feb 27

Replaces 74ABT16373B/74ABTH16373B of 1998 Feb 27

16-bit transparent latch (3-State)

74ABT16373B

FEATURES

- 16-bit transparent latch
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-State
- Live insertion/extraction permitted
- Power-up reset
- 3-State output buffers
- Output capability: +64 mA/-32 mA
- I_{CCL} -19 mA maximum
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16373B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

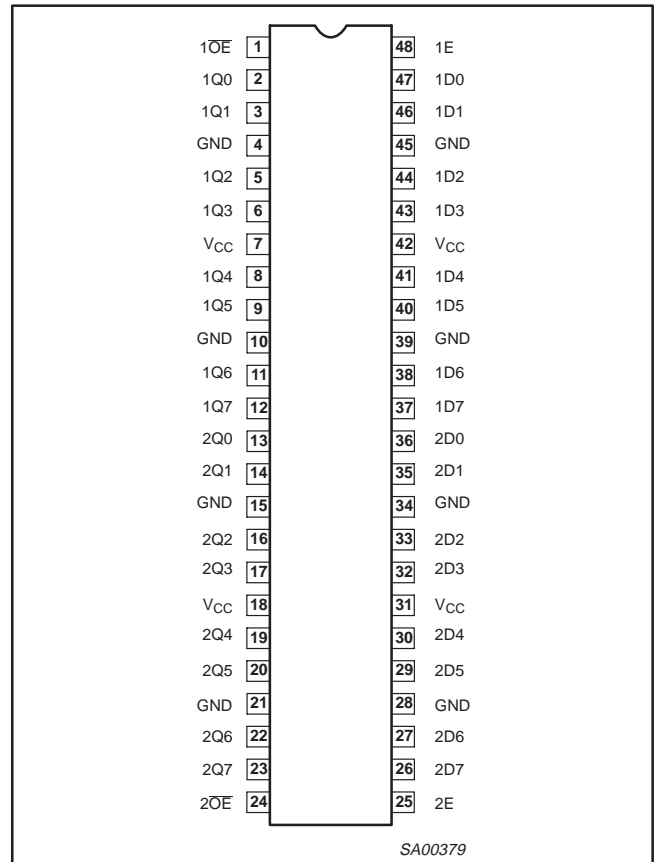
The 74ABT16373B device is a dual octal transparent latch coupled to two sets of eight 3-State output buffers. The two sections of the device are controlled independently by Enable (nE) and Output Enable (nOE) control gates.

The data on each set of D inputs are transferred to the latch outputs when the Latch Enable (nE) input is HIGH. The latch remains transparent to the data inputs while nE is HIGH, and stores the data that is present one set-up time before the HIGH-to-LOW enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-LOW Output Enable (nOE) controls eight 3-State buffers independent of the latch operation.

When nOE is LOW, the latched or transparent data appears at the outputs. When nOE is HIGH, the outputs are in the high-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
		$T_{amb} = 25\text{ }^{\circ}\text{C}; \text{GND} = 0\text{ V}$		
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	$C_L = 50\text{ pF}; V_{CC} = 5\text{ V}$	2.5 2.0	ns
C_{IN}	Input capacitance	$V_I = 0\text{ V or } V_{CC}$	4	pF
C_{OUT}	Output capacitance	$V_O = 0\text{ V or } V_{CC}; \text{3-State}$	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{ V}$	500	μA
I_{CCL}		Outputs low; $V_{CC} = 5.5\text{ V}$	8	mA

ORDERING INFORMATION

$T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$

Type number	Package		Version
	Name	Description	
74ABT16373BDL	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74ABT16373BDGG	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

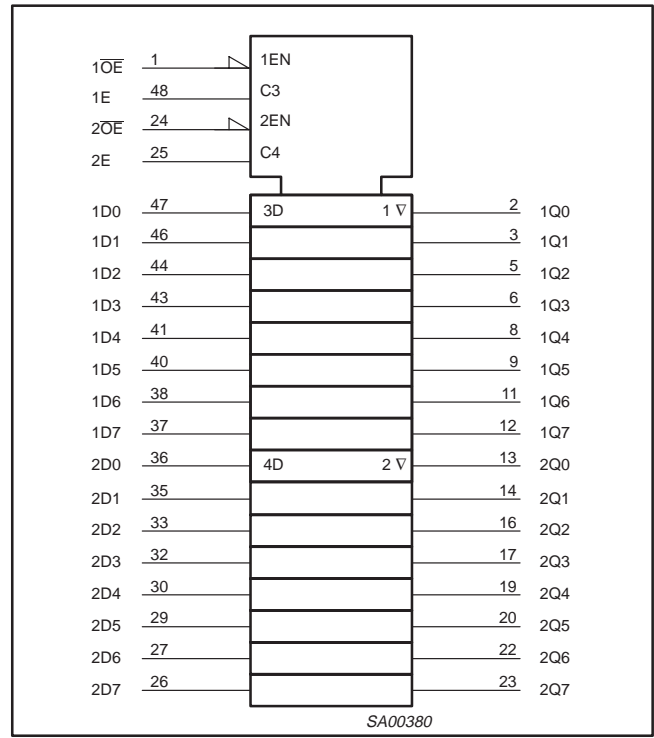
16-bit transparent latch (3-State)

74ABT16373B

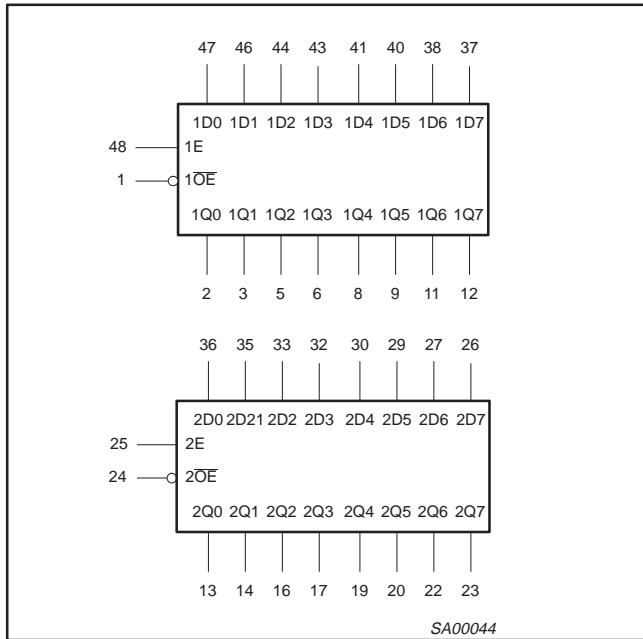
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	1OE, 2OE	Output enable inputs (active-LOW)
48, 25	1E, 2E	Enable inputs (active-HIGH)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0 V)
7, 18, 31, 42	V _{CC}	Positive supply voltage

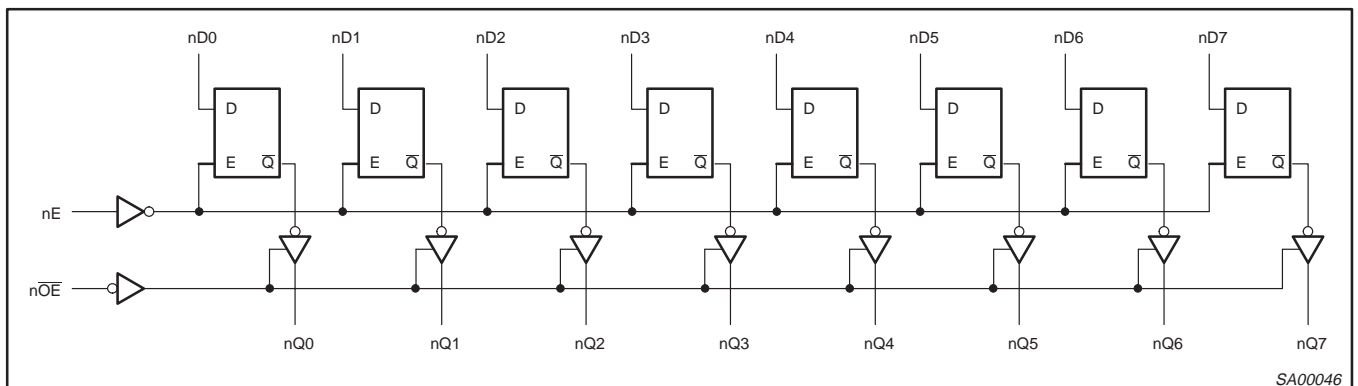
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



LOGIC DIAGRAM



16-bit transparent latch (3-State)

74ABT16373B

FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
nOE	nE	nDx		nQ0 – nQ7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	i h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW E transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the HIGH-to-LOW E transition

NC= No change

X = Don't care

Z = High-impedance "off" state

↓ = HIGH-to-LOW E transition

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0 V	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0 V	-50	mA
V _{OUT}	DC output voltage ³	output in Off or HIGH state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in LOW state	128	mA
		output in HIGH state	-64	
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	HIGH-level input voltage	2.0	-	V
V _{IL}	LOW-level Input voltage	-	0.8	V
I _{OH}	HIGH-level output current	-	-32	mA
I _{OL}	LOW-level output current	-	64	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

16-bit transparent latch (3-State)

74ABT16373B

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25 °C			T _{amb} = -40 °C to +85 °C		
			MIN	TYP	MAX	MIN	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 4.5 V; I _{IK} = -18 mA	-	-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH}	2.5	2.9	-	2.5	-	V
		V _{CC} = 5.0 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH}	3.0	3.4	-	3.0	-	V
		V _{CC} = 4.5 V; I _{OH} = -32 mA; V _I = V _{IL} or V _{IH}	2.0	2.4	-	2.0	-	V
V _{OL}	Low-level output voltage	V _{CC} = 4.5 V; I _{OL} = 64 mA; V _I = V _{IL} or V _{IH}	-	0.42	0.55	-	0.55	V
V _{RST}	Power-up output voltage ³	V _{CC} = 5.5 V; I _O = 1 mA; V _I = GND or V _{CC}	-	0.13	0.55	-	0.55	V
I _I	Input leakage current	V _{CC} = 5.5 V; V _I = V _{CC} or GND	-	±0.01	±1	-	±1	µA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0 V; V _O or V _I ≤ 4.5 V	-	±5.0	±100	-	±100	µA
I _{PU} /I _{PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1 V; V _O = 0.5 V; V _I = GND or V _{CC} ; V _{OE} = GND	-	±5.0	±50	-	±50	µA
I _{OZH}	3-State output HIGH current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = V _{IL} or V _{IH}	-	0.5	10	-	10	µA
I _{OZL}	3-State output LOW current	V _{CC} = 5.5 V; V _O = 0.0 V; V _I = V _{IL} or V _{IH}	-	-0.5	-10		-10	µA
I _O	Output current ¹	V _{CC} = 5.5 V; V _O = 2.5 V	-50	-70	-180	-50	-180	mA
I _{CEX}	Output HIGH leakage current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC}	-	0.1	50	-	50	µA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5 V; Outputs HIGH; V _I = GND or V _{CC}	-	0.5	2	-	2	mA
I _{CCL}		V _{CC} = 5.5 V; Outputs Low; V _I = GND or V _{CC}	-	8	19	-	19	mA
I _{CCZ}		V _{CC} = 5.5 V; Outputs 3-State; V _I = GND or V _{CC}	-	0.5	2	-	2	mA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5 V; one input at 3.4 V, other inputs at V _{CC} or GND	-	5	100	-	100	µA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4 V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 msec. From V_{CC} = 2.1 to V_{CC} = 5 V ± 10% a transition time of up to 100 µsec is permitted.
- Unused pins at V_{CC} or GND.

16-bit transparent latch (3-State)

74ABT16373B

AC CHARACTERISTICS

GND = 0 V, $t_R = t_F = 2.5$ ns, $C_L = 50$ pF, $R_L = 500 \Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{amb} = +25 \text{ }^\circ\text{C}$ $V_{CC} = +5.0 \text{ V}$			$T_{amb} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$ $V_{CC} = +5.0 \text{ V} \pm 0.5 \text{ V}$		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	1.5 1.1	2.5 2.0	3.8 3.1	1.5 1.1	4.4 3.8	ns
t_{PLH} t_{PHL}	Propagation delay nE to nQx	1	1.6 1.3	2.5 2.1	3.8 3.1	1.6 1.3	4.4 3.6	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	4 5	1.2 1.3	2.3 2.3	3.5 3.5	1.2 1.3	4.6 4.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level	4 5	1.9 1.7	3.1 2.6	4.5 3.8	1.9 1.7	5.3 4.2	ns

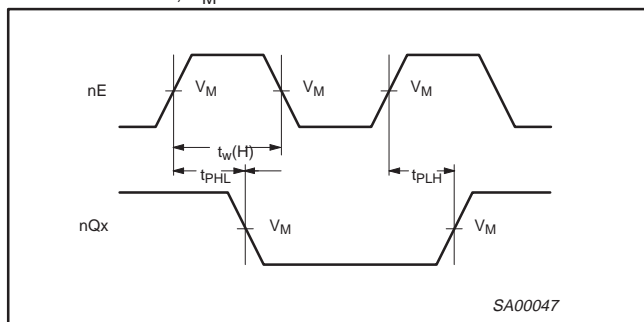
AC SET-UP REQUIREMENTS

GND = 0 V, $t_R = t_F = 2.5$ ns, $C_L = 50$ pF, $R_L = 500 \Omega$

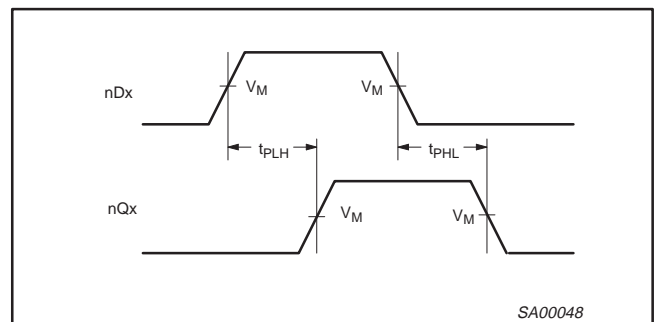
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{amb} = +25 \text{ }^\circ\text{C}$ $V_{CC} = +5.0 \text{ V}$		$T_{amb} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$ $V_{CC} = +5.0 \text{ V} \pm 0.5 \text{ V}$	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW nDx to nE	3	1.0 1.0	0.0 0.3	1.0 1.0	ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW nDx to nE	3	0.5 0.5	-0.2 0.0	0.5 0.5	ns
$t_w(H)$	Enable pulse width HIGH	1	2.5	1.0	2.5	ns

AC WAVEFORMS

For all waveforms, $V_M = 1.5$ V.



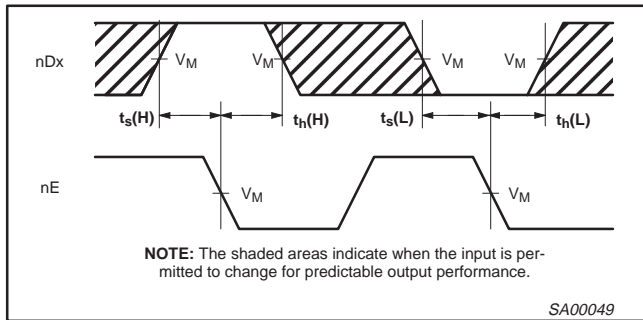
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



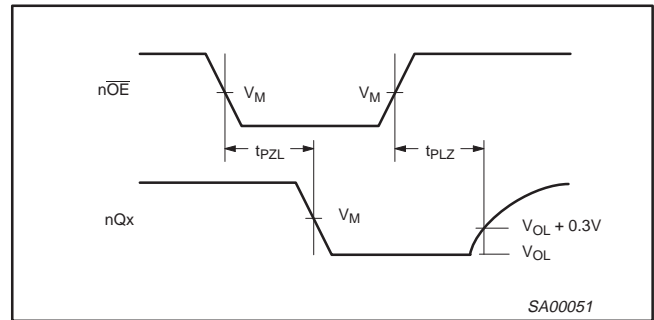
Waveform 2. Propagation Delay for Data to Outputs

16-bit transparent latch (3-State)

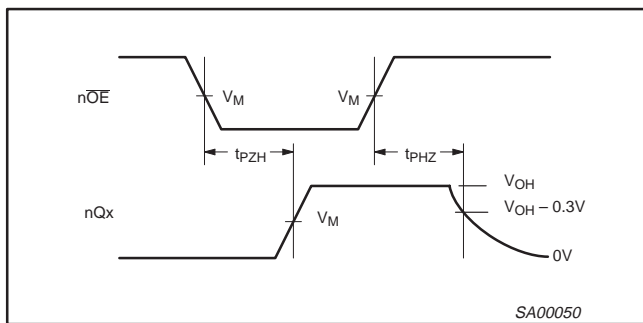
74ABT16373B



Waveform 3. Data Set-up and Hold Times



Waveform 5. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level



Waveform 4. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level

TEST CIRCUIT AND WAVEFORM

Test Circuit for 3-State Outputs

Input Pulse Definition

$V_M = 1.5\text{ V}$

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0 V	1 MHz	500 ns	2.5 ns	2.5 ns

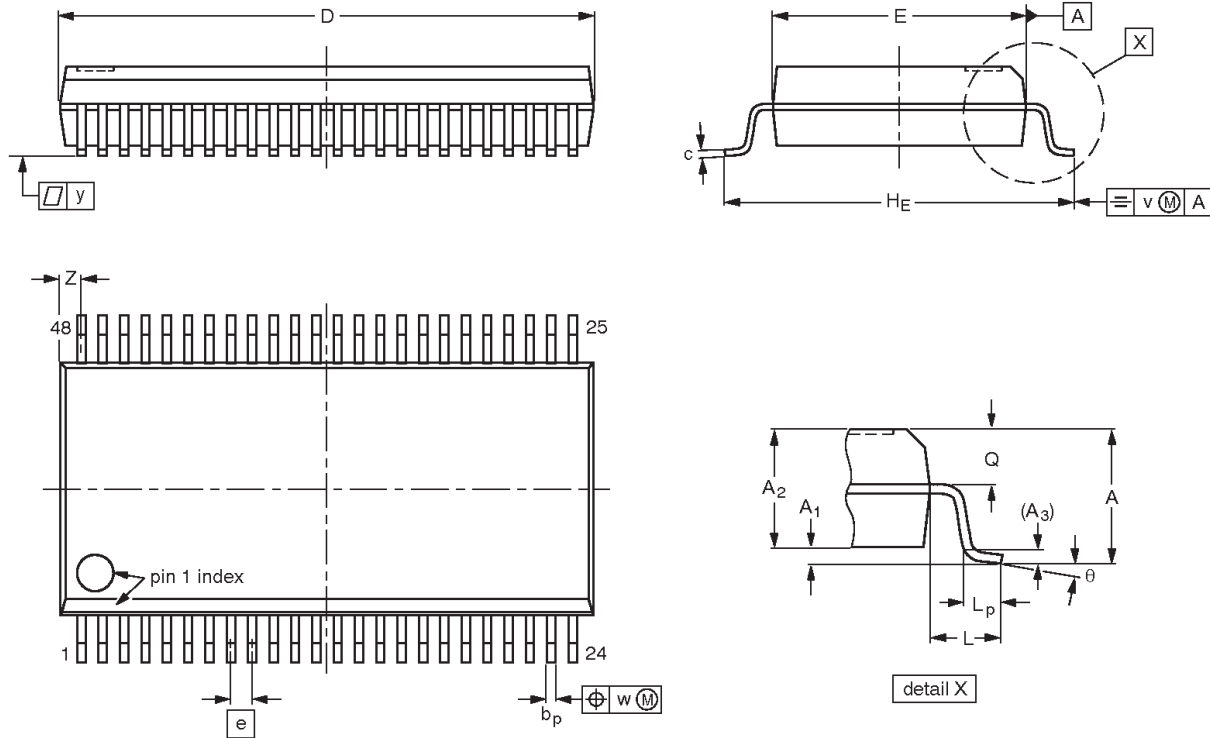
SA00654

16-bit transparent latch (3-State)

74ABT16373B

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

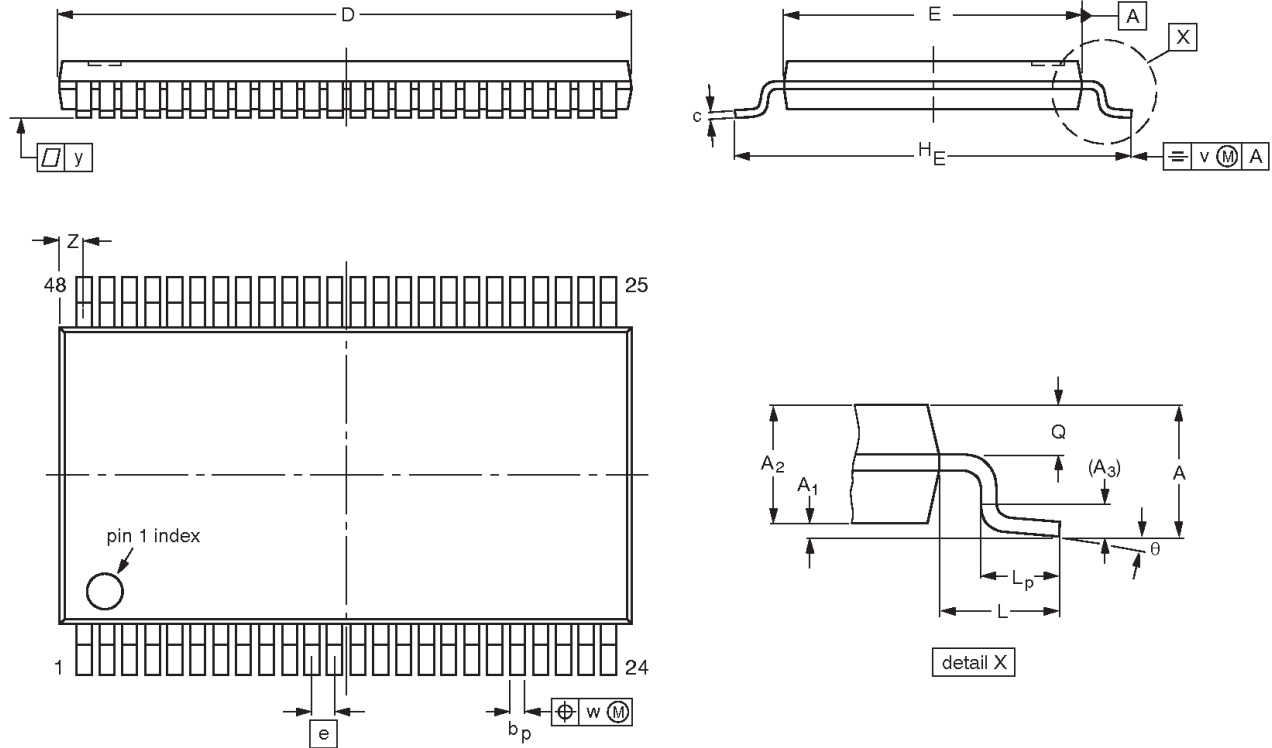
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				99-12-27 03-02-19

16-bit transparent latch (3-State)

74ABT16373B

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				-99-12-27 03-02-19

16-bit transparent latch (3-State)

74ABT16373B

REVISION HISTORY

Rev	Date	Description
_3	20040227	Product data (9397 750 12821); 853-1751 ECN 01-A15429 of 27 January 2004. Replaces data sheet 74ABT_H16373B_2 of 1998 Feb 27 (9397 750 03491). Modifications: <ul style="list-style-type: none">• Delete all references to 74ABTH16373B (product discontinued).
_2	19980227	Product specification (9397 750 03491); ECN 853-1751 19027 of 27 February 1998. Supersedes data of 1995 Aug 03.
_1	19950803	

16-bit transparent latch (3-State)

74ABT16373B

Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products—including circuits, standard cells, and/or software—described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Contact information

For additional information please visit
<http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

© Koninklijke Philips Electronics N.V. 2004
 All rights reserved. Printed in U.S.A.

Date of release: 01-04

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com

Document order number: 9397 750 12985

Let's make things better.