

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 8-bit, voltage output, digital-to-analog converter with output amplifier and double-buffered interface logic. No external trims are required to achieve full specified performance for the part.

1.2 Part Number.

The complete part numbers per Tables 1 and 2 of this specification are as follows:

| Device | Part Number ¹ |
|--------|--------------------------|
| - 1 | AD7224T(X)/883B |
| - 2 | AD7224U(X)/883B |

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

| (X) | Package | Description |
|-----|---------|----------------|
| Q | Q-18 | 18-Pin Cerdip |
| E | E-20A | 20-Contact LCC |

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| | |
|------------------------------------|---|
| V_{DD} to AGND | -0.3V, +17V |
| V_{DD} to DGND | -0.3V, +17V |
| V_{SS} to AGND | -7V, V_{DD} |
| V_{SS} to DGND | -7V, V_{DD} |
| V_{DD} to V_{SS} | -0.3V, +24V |
| AGND to DGND | -0.3V, V_{DD} |
| Digital Input Voltage to DGND | -0.3V, V_{DD} |
| V_{REF} to AGND | -0.3V, V_{DD} |
| V_{OUT} to AGND | V_{SS} , V_{DD} |
| Power Dissipation | |
| Up to $+75^\circ\text{C}$ | 450mW |
| Derates above $+75^\circ\text{C}$ | 6mW/ $^\circ\text{C}$ |
| Operating Temperature Range | -55°C to $+125^\circ\text{C}$ |
| Storage Temperature | -65°C to $+150^\circ\text{C}$ |
| Lead Temperature (Soldering 10sec) | $+300^\circ\text{C}$ |

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for Q-18 and E-20A

$\theta_{JA} = 120^\circ\text{C}/\text{W}$ for Q-18 and E-20A

AD7224—SPECIFICATIONS

Table 1.

| Test | Symbol | Device | Design Limit $T_{min}-T_{max}$ | Sub Group 1 | Sub Group 2, 3 | Sub Group 4 | Test Condition ¹ | Units |
|---|-------------|--------|-----------------------------------|-------------|----------------|-------------|---|----------------|
| Resolution | RES | -1, 2 | 8 | | | | | Bits |
| Relative Accuracy | RA | -1 | 1 | 1 | 1 | | $V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$ | ± LSB max |
| | | -2 | 1/2 | 1 | 1/2 | 1/2 | | |
| Total Unadjusted Error | E_T | -1 | 2 | 2 | 2 | | $V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$ | ± LSB max |
| | | -2 | 1 | 2 | 1 | | | |
| Differential Nonlinearity | DNL | -1, 2 | 1 | 1 | 1 | | Guaranteed Monotonic to 8-Bits | ± LSB max |
| Full-Scale Error | A_E | -1 | 3/2 | 3/2 | 3/2 | | $V_{DD} = +14V; V_{SS} = -5V; V_{REF} = +10V$ | ± LSB max |
| | | -2 | 1 | 3/2 | 1 | 1 | | |
| Zero Code Error | A_{ZCE} | -1 | 30 | 30 | 30 | | $V_{DD} = 16.5V, 11.4V$ and $14V; V_{SS} = -5V; V_{REF} = V_{DD} - 4$ | ± mV max |
| | | -2 | 20 | 30 | 20 | 20 | | |
| Full-Scale Temp Coefficient | dA_E/dT | -1, 2 | 20 | | | | $V_{DD} = 14V$ to $16.5V, V_{REF} = +10V$ | ± ppm/°C max |
| Voltage Output Settling Time ² | t_{SL} | -1, 2 | 5 | | | | Positive Full-Scale Change | µs max |
| | | | 7 | | | | Negative Full-Scale Change | |
| Voltage Output Slew Rate | t_{SR} | -1, 2 | 2.5 | | | | | V/µs min |
| Minimum Load Resistance | R_{L-MIN} | -1, 2 | 2 | | | | $V_{OUT} = +10V; V_{DD} = +14V$ | kΩ min |
| Reference Voltage Range | V_{REF} | -1, 2 | 2 to ($V_{DD} - 4$) | | | | | V min to V max |
| Reference Input Resistance | R_I | -1, 2 | 8 | 8 | 8 | | $V_{DD} = 14V$ | kΩ min |
| Reference Input Capacitance | C_I | -1, 2 | 100 | | | | Occurs When DAC Is Loaded with All 1's | pF min |
| Digital Input High Voltage | V_{IH} | -1, 2 | 2.4 | 2.4 | 2.4 | | $V_{DD} = 11.4V; V_{REF} = V_{DD} - 4$ | V min |
| Digital Input Low Voltage | V_{IL} | -1, 2 | 0.8 | 0.8 | 0.8 | | $V_{DD} = 11.4V; V_{REF} = V_{DD} - 4$ | V max |
| Digital Input Leakage Current | I_{IN} | -1, 2 | 1 | 1 | 1 | | $V_{IN} = 0V$ or $V_{DD}; V_{DD} = 11.4V$ | ± µA max |
| Digital Input Capacitance | C_I | -1, 2 | 8 | | | | | pF max |
| Chip Select/Load DAC Pulse Width | t_{LD} | -1, 2 | 200 | | | | | ns min |
| Write/Reset Pulse Width | t_{WR} | -1, 2 | 200 | | | | | ns min |
| Chip Select/Load DAC to Write Setup Time | t_{CS} | -1, 2 | 0 | | | | | ns min |
| Chip Select/Load DAC to Write Hold Time | t_{CH} | -1, 2 | 0 | | | | | ns min |
| Data Valid to Write Setup Time | t_{DS} | -1, 2 | 100 | | | | | ns min |
| Data Valid to Write Hold Time | t_{DH} | -1, 2 | 10 | | | | | ns min |
| Power Supply Voltage Range | V_{DD} | -1, 2 | 11.4 | | | | For Specified Performance | + V min |
| | | | 16.5 | | | | | + V max |
| | V_S | -1, 2 | 4.5 | | | | For Specified Performance | - V min |
| | | | 5.5 | | | | | - V max |
| Power Supply Current | I_{DD} | -1, 2 | 6 | 4 | 6 | | Output Unloaded: $V_{IN} = V_{IL}$ or V_{IH} $V_{DD} = 16.5V; V_{SS} = -5.5V; V_{REF} = 12.5V$ | mA max |
| | I_{SS} | -1, 2 | 5 | 3 | 5 | | | |

NOTE: DUAL SUPPLY OPERATION

¹ $V_{DD} = +11.4V$ to $16.5V; V_{SS} = -5V \pm 10\%$; AGND = DGND = 0V; $V_{REF} = +2V$ to $(V_{DD} - 4V)$ unless otherwise stated.

² $V_{REF} = +10V$; settling time to $\pm 1/2$ LSB.

Table 2.

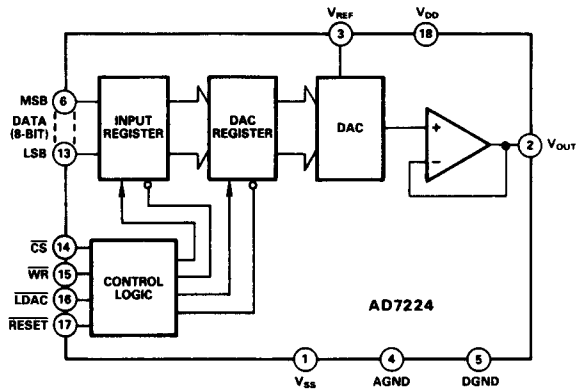
| Test | Symbol | Device | Design Limit $T_{min}-T_{max}$ | Sub Group 1 | Sub Group 2, 3 | Sub Group 4 | Test Condition ¹ | Units |
|---|---------------|--------|-----------------------------------|-------------|----------------|-------------|--|-----------------|
| Resolution | RES | -1,2 | 8 | | | | | Bits |
| Total Unadjusted Error | E_T | -1,2 | 2 | 2 | 2 | | $V_{DD} = +14V$ | \pm LSB max |
| Differential Nonlinearity | DNL | -1,2 | 1 | 1 | 1 | | $V_{DD} = +14V$; Guaranteed Monotonic to 8-Bits | \pm LSB max |
| Voltage Output Settling Time ² | t_{SI} | -1,2 | 5 | | | | Positive Full-Scale Change | μs max |
| | | | 20 | | | | Negative Full-Scale Change | |
| Voltage Output Slew Rate | t_{SR} | -1,2 | 2 | | | | | V/ μs min |
| Minimum Load Resistance | $R_{L_{MIN}}$ | -1,2 | 2 | 2 | 2 | | $V_{OUT} = +10V$; $V_{DD} = +15V$ | k Ω min |
| Reference Input Resistance | R_I | -1,2 | 8 | | | | $V_{DD} = 14.25V$ | k Ω min |
| Reference Input Capacitance | C_I | -1,2 | 100 | | | | Occurs When DAC Is Loaded with All 1's | pF max |
| Digital Input High Voltage | V_{IH} | -1,2 | 2.4 | 2.4 | 2.4 | | $V_{DD} = 14.25V$ | V min |
| Digital Input Low Voltage | V_{IL} | -1,2 | 0.8 | 0.8 | 0.8 | | $V_{DD} = 14.25V$ | V max |
| Digital Input Leakage Current | I_{IN} | -1,2 | 1 | | | | $V_{IN} = 0V$ or V_{DD} ; $V_{DD} = 14.25V$ | $\pm \mu A$ max |
| Digital Input Capacitance | C_I | -1,2 | 8 | | | | | pF max |
| Chip Select/Load DAC Pulse Width | t_{LD} | -1,2 | 200 | | | | | ns min |
| Write/Reset Pulse Width | t_{WR} | -1,2 | 200 | | | | | ns min |
| Chip Select/Load DAC to Write Setup Time | t_{CS} | -1,2 | 0 | | | | | ns min |
| Chip Select/Load DAC to Write Hold Time | t_{CH} | -1,2 | 0 | | | | | ns min |
| Data Valid to Write Setup Time | t_{DS} | -1,2 | 100 | | | | | ns min |
| Data Valid to Write Hold Time | t_{DH} | -1,2 | 10 | | | | | ns min |
| Power Supply Voltage Range | V_{DD} | -1,2 | 14.25 | | | | For Specified Performance | + V min |
| | | | 15.75 | | | | | + V max |
| Power Supply Current | I_{DD} | -1,2 | 6 | | | | Outputs Unloaded; $V_{IN} = V_{IL}$ or V_{IH} $V_{DD} = 15.75V$ | mA max |

NOTE: SINGLE SUPPLY OPERATION

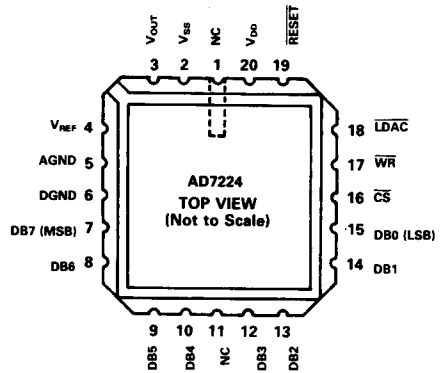
¹ $V_{DD} = +15V \pm 5\%$; $V_{SS} = AGND = DGND = 0V$; $V_{REF} = +10V$ unless otherwise stated.²Settling time to $\pm 1/2LSB$.

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3.2.1 Functional Block Diagram and Terminal Assignments.



E Package (LCC)

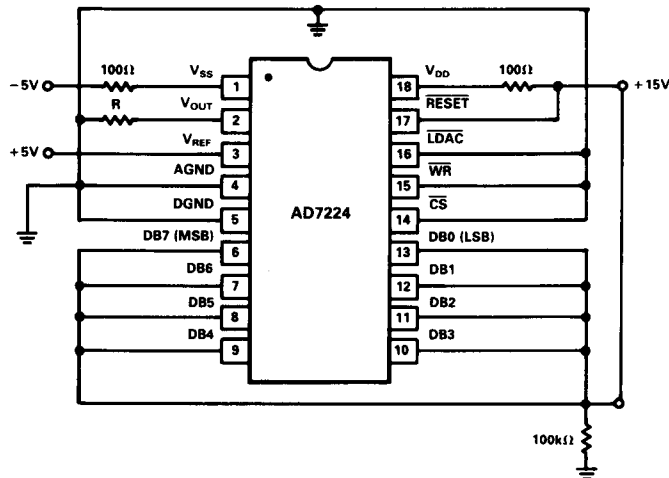


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTE:
V_{DD} IS TURNED ON FIRST, THEN V_{SS}
FOLLOWED BY V_{REF}.

Table 3. AD7224 Truth Table

| RESET | LDAC | WR | CS | Function |
|-------|------|----|----|---|
| H | L | L | L | Both Registers are Transparent |
| H | X | H | X | Both Registers are Latched |
| H | H | X | H | Both Registers are Latched |
| H | H | L | L | Input Register Transparent |
| H | H | | L | Input Register Latched |
| H | L | L | H | DAC Register Transparent |
| H | L | | H | DAC Register Latched |
| L | X | X | X | Both Registers Loaded With All Zeros |
| | H | H | H | Both Register Latched With All Zeros and Output Remains at Zero |
| | L | L | L | Both Registers are Transparent and Output Follows Input Data |

H = High State, L = Low State, X = Don't Care

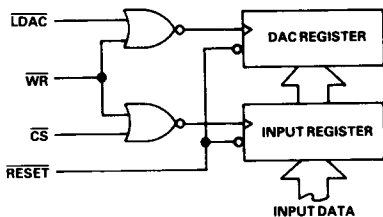
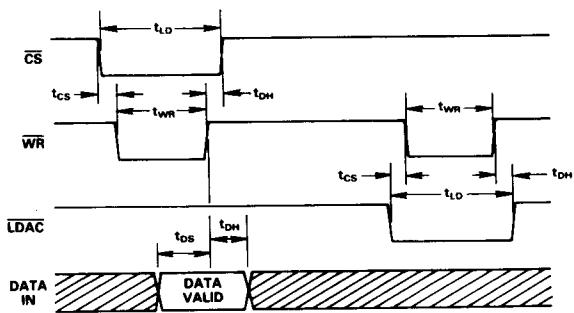


Figure 1. Input Control Logic



NOTES

1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD} .
 $t_r = t_f = 20\text{ns}$ OVER V_{DD} RANGE
2. TIMING MEASUREMENT REFERENCE LEVEL IS

$$\frac{V_{RH} + V_{RL}}{2}$$

Figure 2. Write Cycle Timing Diagram