HARRIS SEMICONDUCTOR

HI-506, HI-507 HI-508, HI-509

Single 16 and 8/Differential 8 and 4 Channel CMOS Analog Multiplexers

December 1993

Features

- Low On Resistance 180Ω
- Wide Analog Signal Range ±15V
- TTL/CMOS Compatible
- Access Time 250ns
- 44V Maximum Power Supply
- Break-Before-Make Switching
- No Latch-Up
- Replaces DG506A/DG506AA and DG507A/DG507AA
- Replaces DG508A/DG508AA and DG509A/DG509AA

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

The HI-506/HI-507 and HI-508/HI-509 monolithic CMOS multiplexers each include an array of sixteen and eight analog switches respectively, a digital decoder circuit for channel selection, voltage reference for logic thresholds, and an enable input for device selection when several multiplexers are present. The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latchup. DI also offers much lower substrate leakage and parasitic capacitance than conventional junction isolated CMOS (see Application Note AN521).

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for logic "1" and maximum 0.8V for logic "0". This allows direct interface without pullup resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and diode clamp to each supply.

The HI-506 is a single 16 channel, the HI-507 is an 8 channel differential, the HI-508 is a single 8 channel and the HI-509 is a 4 channel differential multiplexer. The HI-506/HI-507 are available in a 28 pin ceramic or plastic DIP, 28 pad leadless chip carrier (LCC), 28 pin plastic leaded chip carrier (PLCC) and 28 lead SOIC packages. The HI-508/HI-509 are available in a 16 pin plastic or ceramic DIP, a 20 pin plastic leaded chip carrier (PLCC), 20 pad ceramic leadless chip carrier (LCC) and 16 lead SOIC packages.

If input overvoltages are present the HI-546/HI-547/HI-548/HI-549 multiplexers are recommended. For further information see Application Notes AN520 and AN521. The HI-506/HI-507/HI-508/HI-509 is offered in both commercial and military grades. For additional High Reliability Screening including 160 hour burn-in specify the "-8" suffix. For Mil-Std-883 compliant parts, request the HI-506/883, HI-507/883, HI-508/883 or HI-509/883 datasheet

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3142**

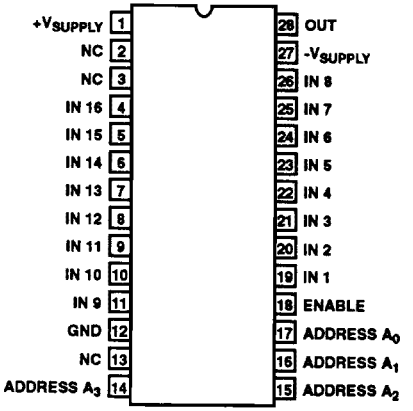
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0506/883	-55°C to +125°C	28 Lead Ceramic DIP
HI1-0506-8	Hi-Rel Processing with Burn-In	28 Lead Ceramic DIP
HI1-0506-9	-40°C to +85°C	28 Lead Ceramic DIP
HI4-0506/883	-55°C to +125°C	28 Lead Ceramic LCC
HI1-0507/883	-55°C to +125°C	28 Lead Ceramic DIP
HI9P0506-9	-40°C to +85°C	28 Lead SOIC
HI3-0506-5	0°C to +75°C	28 Lead Plastic DIP
HI1-0506-7	0°C to +75°C + 96 Hour Burn-In	28 Lead Ceramic DIP
HI9P0506-5	0°C to +75°C	28 Lead SOIC
HI40506-5	0°C to +75°C	28 Lead PLCC
HI1-0506-5	0°C to +75°C	28 Lead Ceramic DIP
HI1-0506-4	-25°C to +85°C	28 Lead Ceramic DIP
HI1-0506-2	-55°C to +125°C	28 Lead Ceramic DIP
HI1-0507-8	Hi-Rel Processing with Burn-In	28 Lead Ceramic DIP
HI1-0507-9	-40°C to +85°C	28 Lead Ceramic DIP
HI4-0507/883	-55°C to +125°C	28 Lead Ceramic LCC
HI1-0507-4	-25°C to +85°C	28 Lead Ceramic DIP
HI4P0507-5	0°C to +75°C	28 Lead PLCC
HI9P0507-5	0°C to +75°C	28 Lead SOIC
HI1-0507-5	0°C to +75°C	28 Lead Ceramic DIP
HI3-0507-5	0°C to +75°C	28 Lead Plastic DIP
HI1-0507-7	0°C to +75°C + 96 Hour Burn-In	28 Lead Ceramic DIP
HI9P0507-9	-40°C to +85°C	28 Lead SOIC
HI1-0507-2	-55°C to +125°C	28 Lead Ceramic DIP

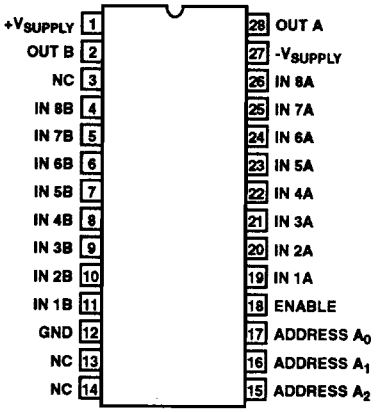
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0508/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0508-8	Hi-Rel Processing with Burn-In	16 Lead Ceramic DIP
HI1-0508-9	-40°C to +85°C	16 Lead Ceramic DIP
HI4-0508/883	-55°C to +125°C	20 Lead Ceramic LCC
HI1-0509/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0508-5	0°C to +75°C	16 Lead Ceramic DIP
HI3-0508-5	0°C to +75°C	16 Lead Plastic DIP
HI1-0508-4	-25°C to +85°C	16 Lead Ceramic DIP
HI1-0508-2	-55°C to +125°C	16 Lead Ceramic DIP
HI4P0508-5	0°C to +75°C	20 Lead PLCC
HI1-0508-7	0°C to +75°C + 96 Hour Burn-In	16 Lead Ceramic DIP
HI9P0508-9	-40°C to +85°C	16 Lead SOIC (N)
HI9P0508-5	0°C to +75°C	16 Lead SOIC (N)
HI1-0509-8	Hi-Rel Processing with Burn-In	16 Lead Ceramic DIP
HI1-0509-9	-40°C to +85°C	16 Lead Ceramic DIP
HI4-0509/883	-55°C to +125°C	20 Lead Ceramic LCC
HI9P0509-5	0°C to +75°C	16 Lead SOIC (N)
HI9P0509-9	-40°C to +85°C	16 Lead SOIC (N)
HI1-0509-4	-25°C to +85°C	16 Lead Ceramic DIP
HI1-0509-5	0°C to +75°C	16 Lead Ceramic DIP
HI3-0509-5	0°C to +75°C	16 Lead Plastic DIP
HI4P0509-5	0°C to +75°C	20 Lead PLCC
HI1-0509-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0509-7	0°C to +75°C + 96 Hour Burn-In	16 Lead Ceramic DIP

Pinouts

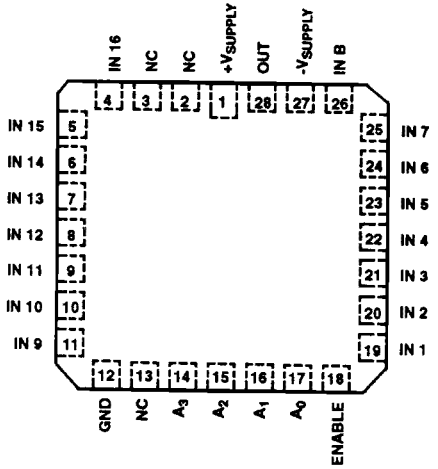
HI-506
(PDIP, CDIP, SOIC)
TOP VIEW



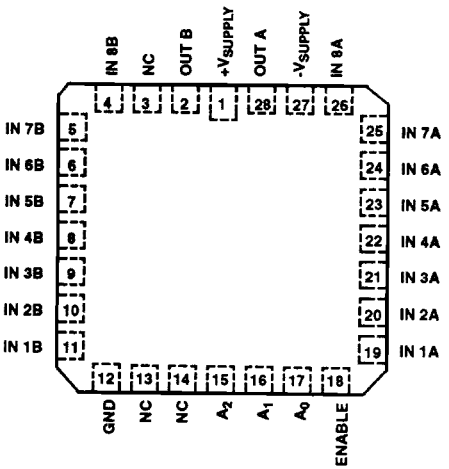
HI-507
(PDIP, CDIP, SOIC)
TOP VIEW



HI-506
(LCC, PLCC)
TOP VIEW

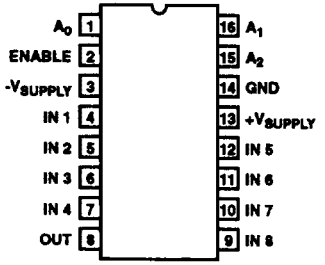


HI-507
(LCC, PLCC)
TOP VIEW

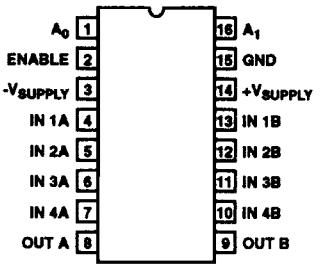


Pinouts (Continued)

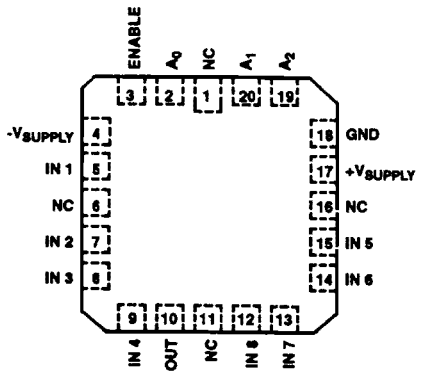
HI-508
(PDIP, CDIP, SOIC)
TOP VIEW



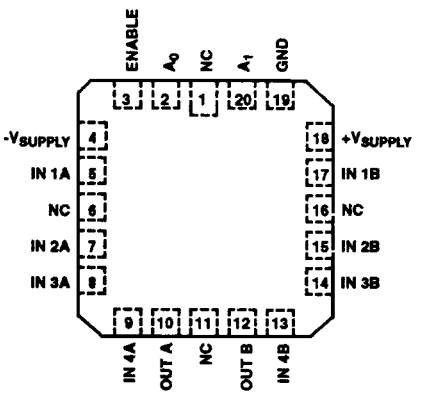
HI-509
(PDIP, CDIP, SOIC)
TOP VIEW



HI-508
(LCC, PLCC)
TOP VIEW

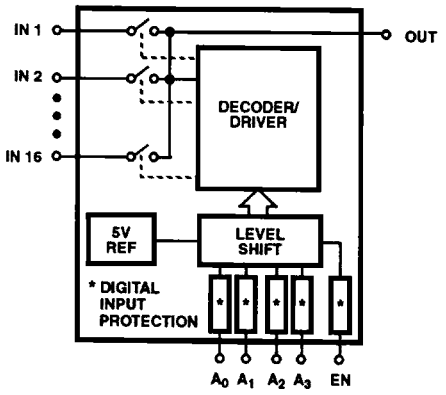


HI-509
(LCC, PLCC)
TOP VIEW

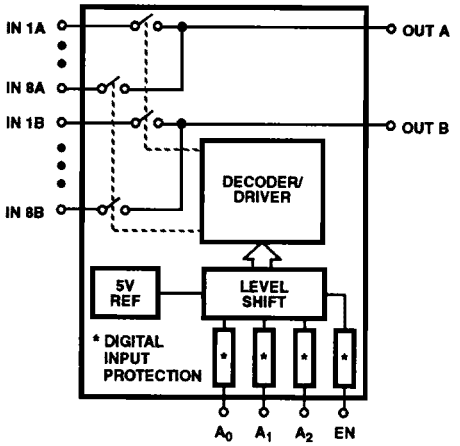


Functional Diagrams

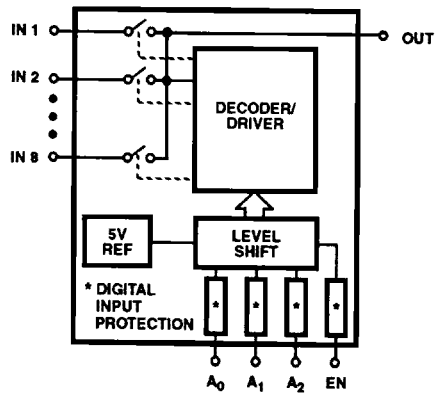
HI-506



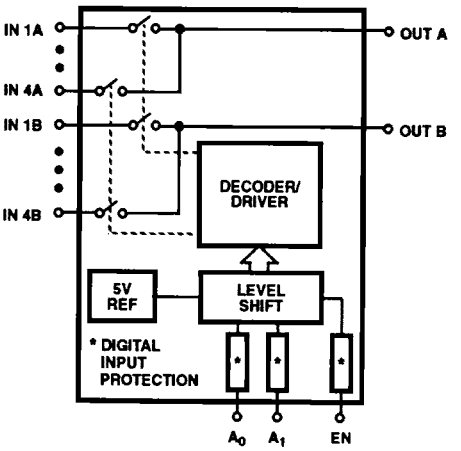
HI-507



HI-508

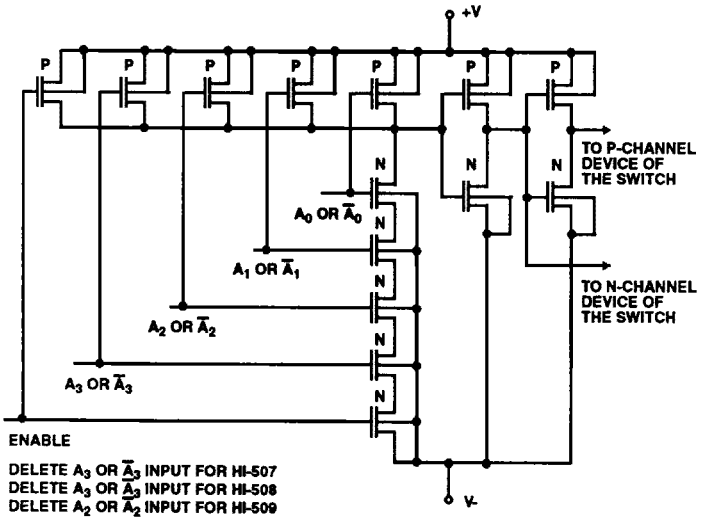


HI-509



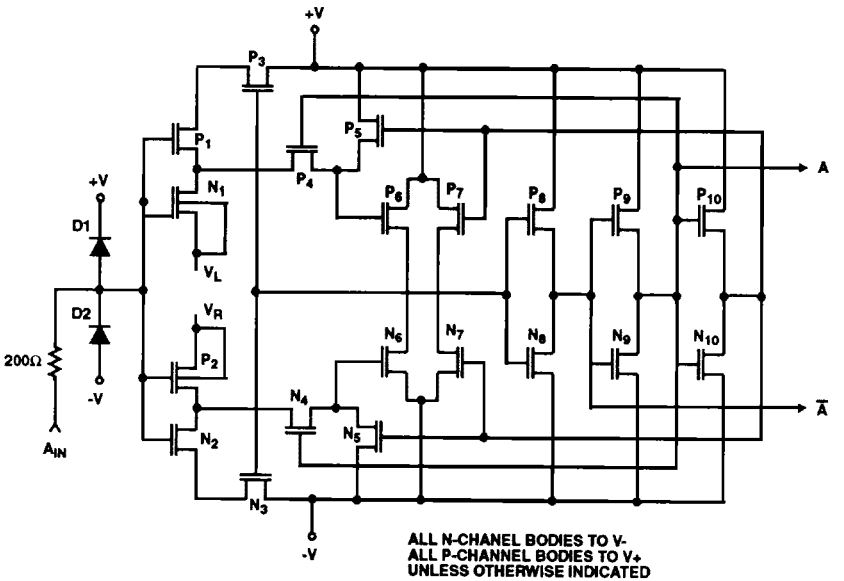
Schematic Diagrams

ADDRESS DECODER



DELETE A_3 OR $\overline{A}_3$ INPUT FOR HI-507
DELETE A_3 OR $\overline{A}_3$ INPUT FOR HI-508
DELETE A_2 OR $\overline{A}_2$ INPUT FOR HI-509

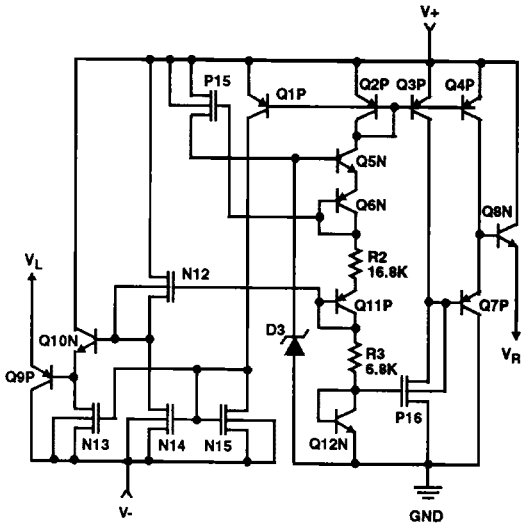
ADDRESS INPUT BUFFER
LEVER SHIFTER



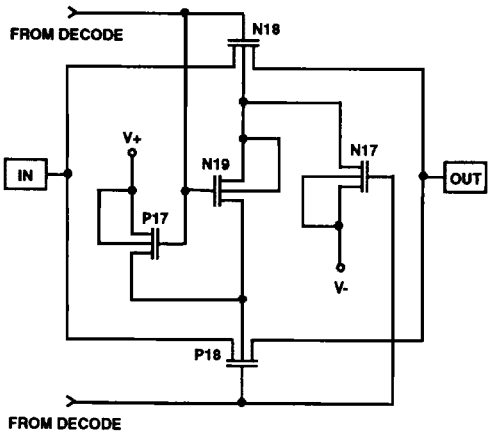
ALL N-CHANEL BODIES TO V-
ALL P-CHANNEL BODIES TO V+
UNLESS OTHERWISE INDICATED

Schematic Diagrams (Continued)

TTL REFERENCE CIRCUIT



MULTIPLEX SWITCH



Absolute Maximum Ratings

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ ..... +44V
$V_{SUPPLY(+)}$ to GND ..... +22V
$V_{SUPPLY(-)}$ to GND ..... -25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage (Note 7)
$+V_S$ ..... $+V_{SUPPLY}$ +2V
$-V_S$ ..... $-V_{SUPPLY}$ -2V
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
(Pulsed at 1ms, 10% duty cycle max)
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
16 Lead Ceramic DIP Packages	80°C/W	24°C/W
16 Lead SOIC Packages	115°C/W	-
16 Lead Plastic DIP	100°C/W	-
20 Lead Ceramic LCC Packages	75°C/W	20°C/W
20 Lead PLCC	80°C/W	-
28 Lead Ceramic DIP Packages	55°C/W	20°C/W
28 Lead Plastic DIP Package	60°C/W	-
28 Lead SOIC Package	70°C/W	-
28 Lead Ceramic LCC Packages	60°C/W	11°C/W
28 Lead PLCC Packages	70°C/W	-

Operating Temperature Ranges
HI-506/507/508/509-2, -8 ..... -55°C to +125°C
HI-506/507/508/509-4 ..... -25°C to +85°C
HI-506/507/508/509-5 ..... -65°C to +150 °C
Junction Temperature
Ceramic ..... +175°C
Plastic ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves.

PARAMETER	TEST CONDITIONS	TEMP	HI-5XX-2, HI-5XX-8			HI-5XX-4, HI-5XX-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Access Time, t_A	(Note 1)	+25°C	-	250	500	-	250	-	ns
		Full	-	-	1000	-	-	1000	ns
Break-Before-Make Delay, t_{OPEN}	(Note 1)	+25°C	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$	(Note 1)	+25°C	-	250	500	-	250	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$	(Note 1)	+25°C	-	250	500	-	250	-	ns
		Full	-	-	1000	-	-	1000	ns
Settling Time to 0.1%, t_S (HI-506 and HI-507)		+25°C	-	1.2	-	-	1.2	-	µs
Settling Time to 0.01%, t_S (HI-506 and HI-507)		+25°C	-	2.4	-	-	2.4	-	µs
Settling Time to 0.1%, t_S (HI-508 and HI-509)		+25°C	-	360	-	-	360	-	ns
Settling Time to 0.01%, t_S (HI-508 and HI-509)		+25°C	-	600	-	-	600	-	ns
"Off Isolation"	(Note 5)	+25°C	50	68	-	50	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		+25°C	-	10	-	-	10	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-506)		+25°C	-	52	-	-	52	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-507)		+25°C	-	30	-	-	30	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-508)		+25°C	-	17	-	-	17	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-509)		+25°C	-	12	-	-	12	-	pF
Digital Input Capacitance, C_A		+25°C	-	6	-	-	6	-	pF

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP	HI-5XX-2, HI-5XX-8			HI-5XX-4, HI-5XX-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input to Output Capacitance, $C_{DS(OFF)}$		+25°C	-	0.08	-	-	0.08	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL}	(Note 1)	Full	-	-	+0.8	-	-	+0.8	V
Input High Threshold, V_{AH}	(Note 1)	Full	+2.4	-	-	+2.4	-	-	V
Input Leakage Current (High or Low), I_A	(Notes 1, 4)	Full	-	-	1.0	-	-	1.0	µA
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_S		Full	-15	-	+15	-15	-	+15	V
On Resistance, R_{ON}	(Notes 1, 2)	+25°C	-	180	300	-	180	400	Ω
ΔR_{ON}, (Any Two Channels)		+25°C	-	5	-	-	5	-	%
Off Input Leakage Current, $I_{S(OFF)}$	(Note 3)	+25°C	-	0.03	-	-	0.03	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$	(Note 3)	+25°C	-	0.3	-	-	0.3	-	nA
HI-506		Full	-	-	300	-	-	300	nA
HI-507		Full	-	-	200	-	-	200	nA
HI-508		Full	-	-	200	-	-	200	nA
HI-509		Full	-	-	100	-	-	100	nA
On Channel Leakage Current, $I_{D(ON)}$	(Note 3)	+25°C	-	0.3	-	-	0.3	-	nA
HI-506		Full	-	-	300	-	-	300	nA
HI-507		Full	-	-	200	-	-	200	nA
HI-508		Full	-	-	200	-	-	200	nA
HI-509		Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current, I_{DIFF} (HI-507, HI-509 Only)	(Note 1)	Full	-	-	50	-	-	50	nA
POWER REQUIREMENTS									
Current, I+, Pin 1 HI-506/HI-507	(Note 6)	Full	-	1.5	3.0	-	1.5	3.0	mA
Current, I+, HI-508/HI-509	(Note 6)	Full	-	1.5	2.4	-	1.5	2.4	mA
Current, I-, Pin 27 HI-506/HI-507	(Note 6)	Full	-	0.4	1.0	-	0.4	1.0	mA
Current, I-, HI-508/HI-509	(Note 6)	Full	-	0.4	1.0	-	0.4	1.0	mA
Power Dissipation, P_D									
HI-506/HI-507		Full	-	-	60	-	-	60	mW
HI-508/HI-509		Full	-	-	51	-	-	51	mW

NOTES:

1. 100% tested for Dash 8. Leakage currents not tested at -55°C.
2. $V_{OUT} = \pm 10V$, $I_{OUT} = \mp 1mA$.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at +25°C.
5. $V_{EN} = 0.8V$, $R_L = 1K$, $C_L = 15pF$, $V_S = 7V_{RMS}$, $f = 100kHz$.
6. V_{EN}, $V_A = 0V$ or 2.4V.
7. Signal voltage at any analog input or output (S or D) will be clamped to the supply rail by internal diodes. Limit the resulting current as shown under absolute maximum ratings. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the Harris HI-546/HI-547/HI-548/HI-549 multiplexers are recommended.

Performance Curves T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V, Unless Otherwise Specified

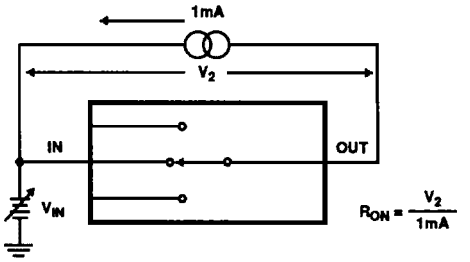


FIGURE 1A. TEST CIRCUIT

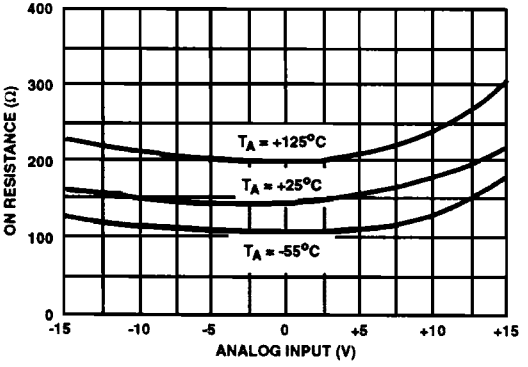


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE, TEMPERATURE

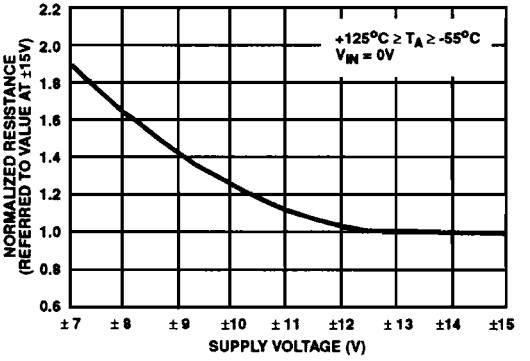


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

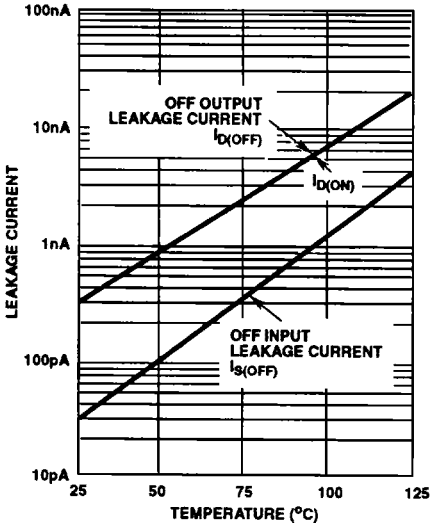


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

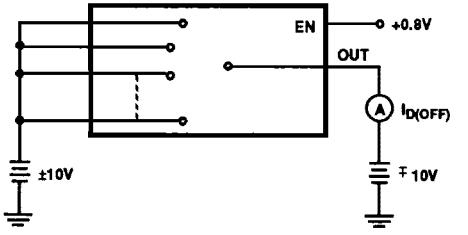


FIGURE 2B. $I_{D(OFF)}$ TEST CIRCUIT

Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$, Unless Otherwise Specified (Continued)

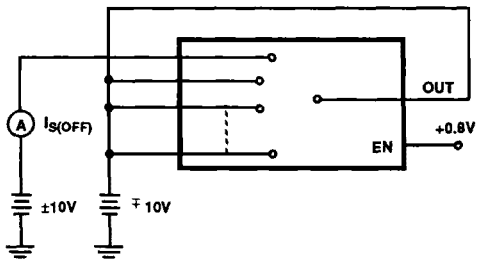


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT

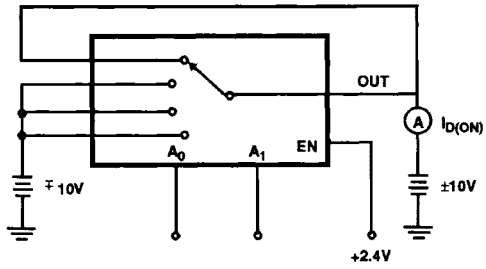


FIGURE 2D. $I_{D(ON)}$ TEST CIRCUIT

FIGURE 2. ON RESISTANCE

NOTE:

1. Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$ +10V/-10V and -10V/+10V)

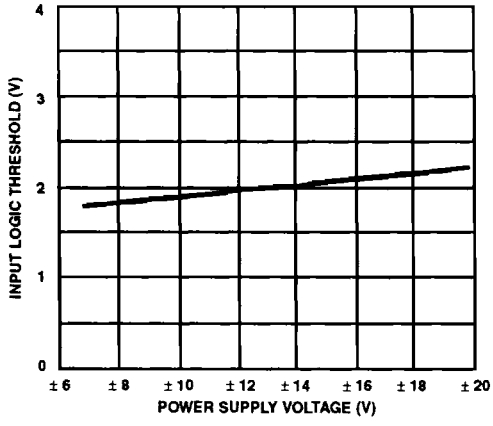


FIGURE 3. LOGIC THRESHOLD vs POWER SUPPLY VOLTAGE

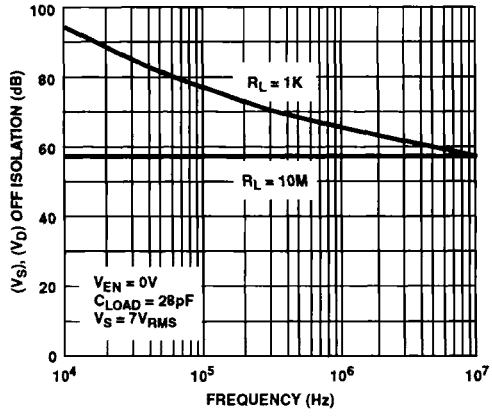


FIGURE 4. OFF ISOLATION vs FREQUENCY

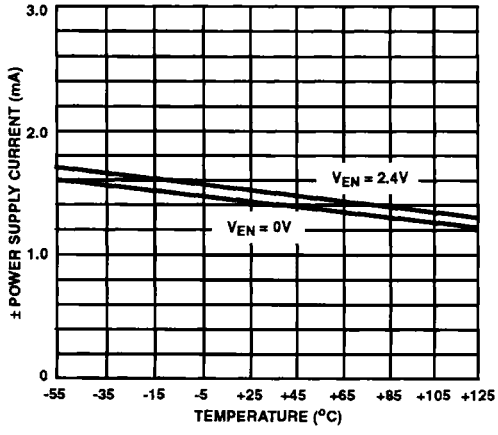


FIGURE 5A. HI-506/HI-507

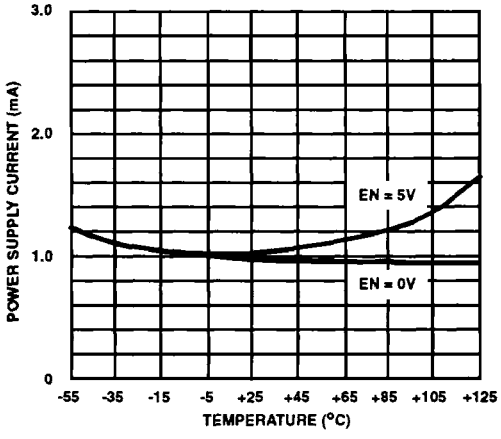


FIGURE 5B. HI-508/HI-509

FIGURE 5. POWER SUPPLY CURRENT vs TEMPERATURE

Performance Curves T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V, Unless Otherwise Specified (Continued)

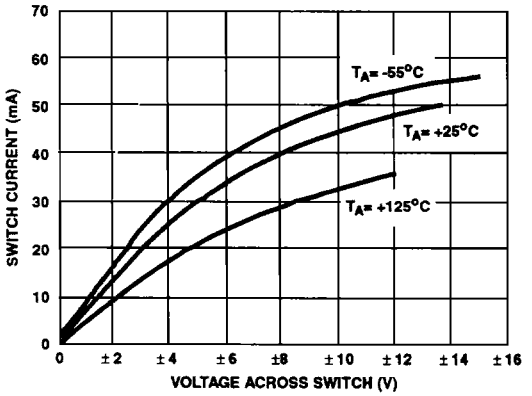


FIGURE 6A. ON CHANNEL CURRENT vs VOLTAGE

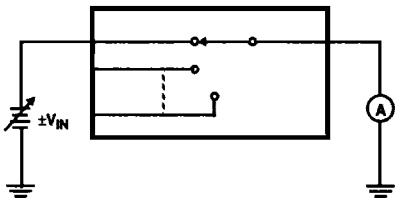


FIGURE 6B. TEST CIRCUIT

FIGURE 6. ON CHANNEL CURRENT vs VOLTAGE

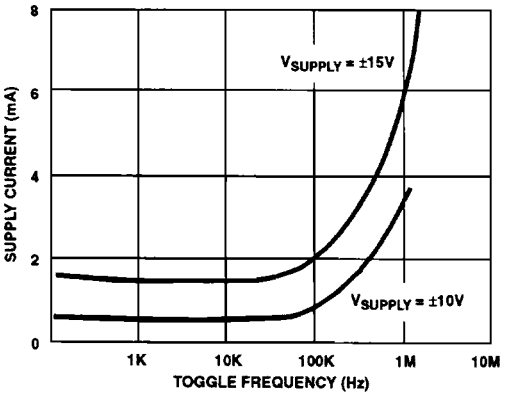


FIGURE 7A. SUPPLY CURRENT vs TOGGLE FREQUENCY

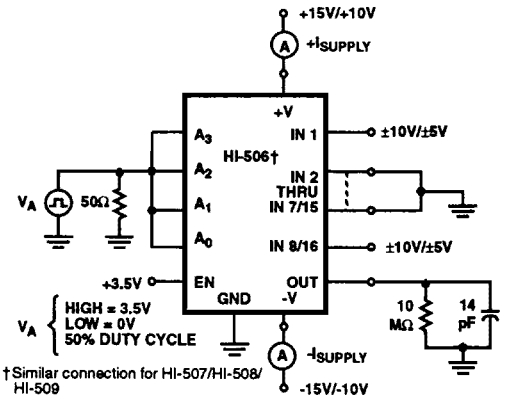


FIGURE 7B. TEST CIRCUIT

FIGURE 7. SUPPLY CURRENT

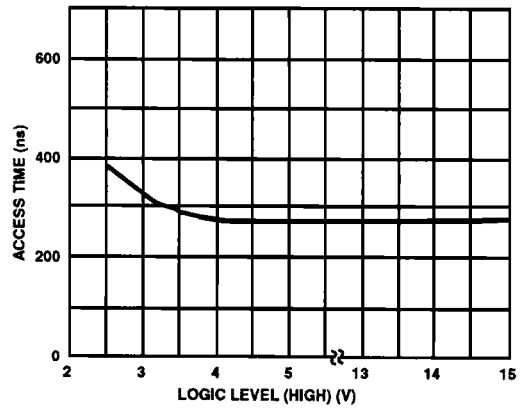


FIGURE 8A. ACCESS TIME vs LOGIC LEVEL (HIGH)

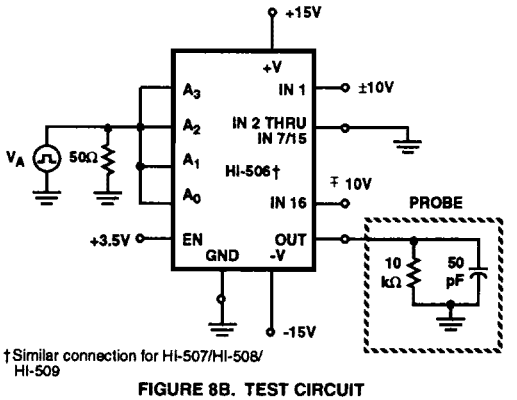


FIGURE 8B. TEST CIRCUIT

Switching Waveforms

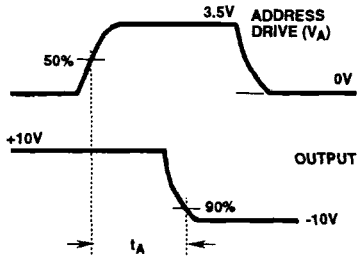


FIGURE 8C. WAVEFORMS

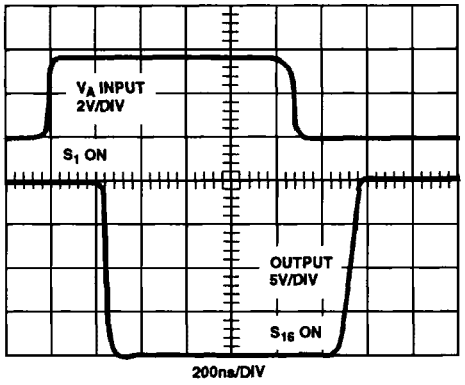
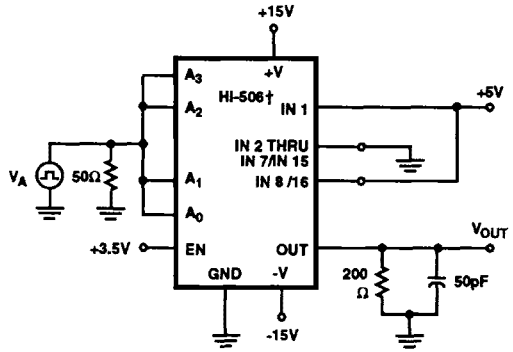


FIGURE 8D. ACCESS TIME

FIGURE 8. ACCESS TIME



†Similar connection for HI-507/HI-508/HI-509

FIGURE 9A. TEST CIRCUIT

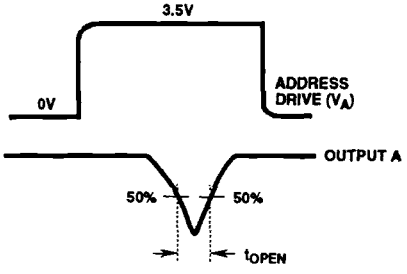


FIGURE 9B. WAVEFORMS

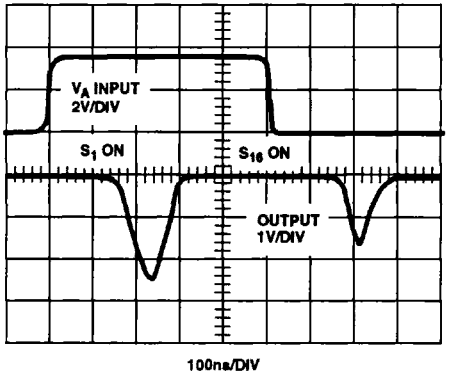
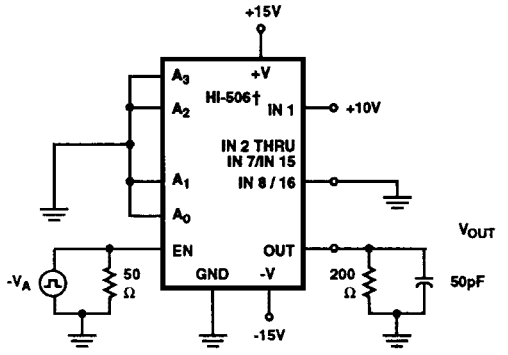


FIGURE 9C. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

FIGURE 9. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

Switching Waveforms (Continued)



†Similar connection for HI-507/HI-508/HI-509

FIGURE 10A. TEST CIRCUIT

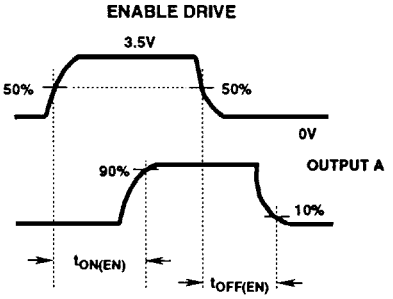


FIGURE 10B. WAVEFORMS

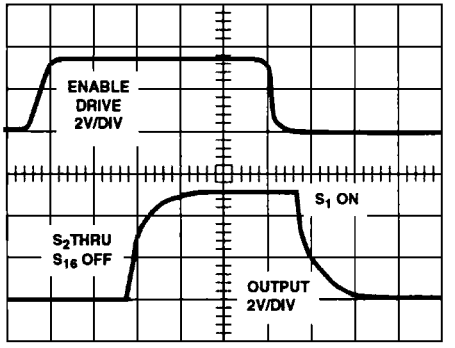


FIGURE 10C. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

FIGURE 10. ENABLE DELAY

Truth Tables

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-508

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Die Characteristics

DIE DIMENSIONS:
129 mils x 82 mils

METALLIZATION:
Type: CuAl
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride/Silox
Nitride Thickness: 3.5kÅ ± 1kÅ
Silox Thickness: 12kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$1.4 \times 10^5 A/cm^2$

TRANSISTOR COUNT: 421

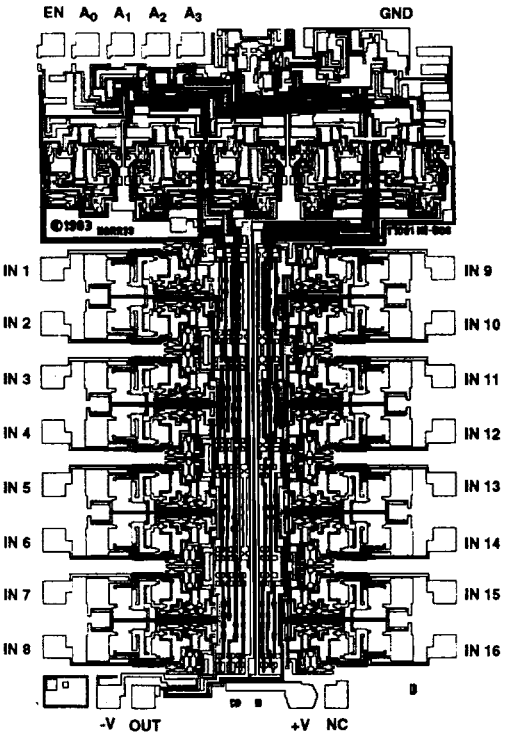
PROCESS: CMOS-DI

SUBSTRATE POTENTIAL*: $-V_{SUPPLY}$

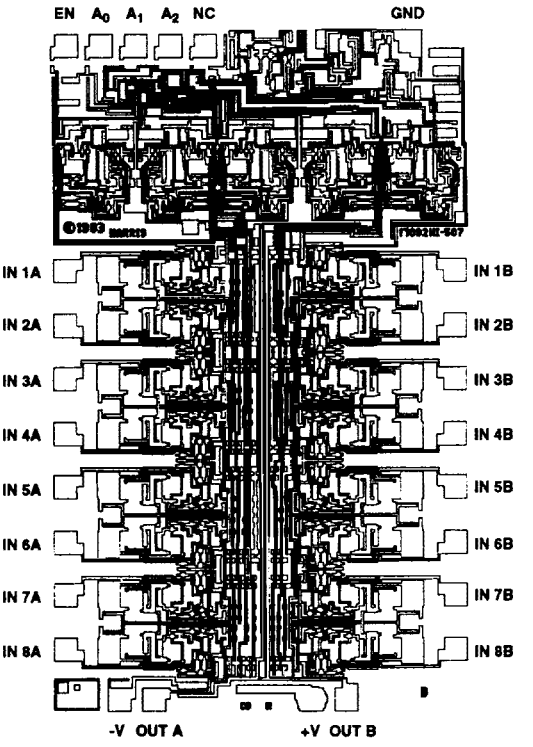
* The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential

Metallization Mask Layout

HI-506



HI-507



NOTE: Pad numbers correspond to DIP pin numbers only.

Die Characteristics

DIE DIMENSIONS:
81.9 mils x 90.2 mils

METALLIZATION:
Type: CuAl
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride/Silox
Nitride Thickness: 3.5kÅ ± 1kÅ
Silox Thickness: 12kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$1.4 \times 10^5 A/cm^2$

TRANSISTOR COUNT: 234

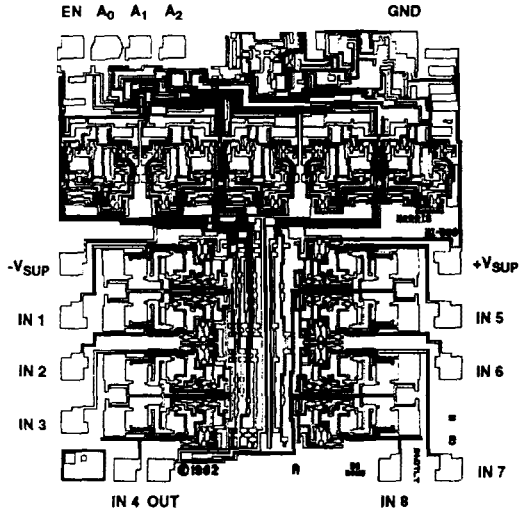
PROCESS: CMOS-DI

SUBSTRATE POTENTIAL*: $-V_{SUPPLY}$

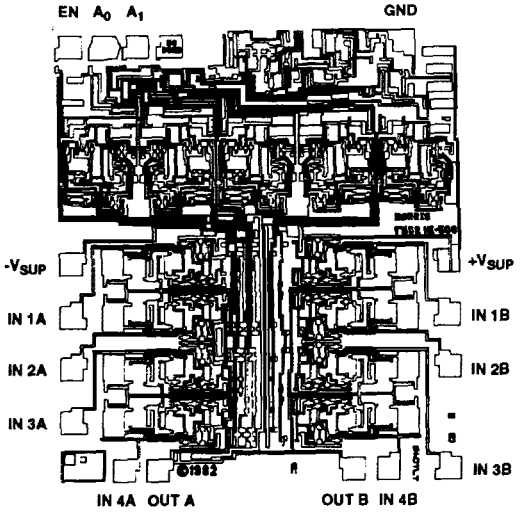
* The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential

Metallization Mask Layout

HI-508



HI-509



NOTE: Pad numbers correspond to DIP pin numbers only.