28 Gbps EML Driver with Peak Detector

Data Sheet **HMC7144**

FEATURES

- Operation up to 32 Gbps
- Low dc power dissipation
  - 0.15 W for 1.5 V p-p swing at 3.5 V supply
  - 0.4 W for 2 V p-p swing at 5 V supply
- Adjustable output amplitude from 1.2 V p-p to 2.2 V p-p
- Integrated peak detector
- 24-lead, ceramic, 4 mm × 4 mm LCC package: 16 mm²

APPLICATIONS

- 100 Gbps Ethernet LR4 (10 km) and ER4 (40 km) applications
- C-form factor pluggable (CFP/CFP2) or similar form factor modules
- Optical transceivers and pluggable modules
- Broadband gain stages and preamplifiers
- Broadband test and measurement equipment

FUNCTIONAL BLOCK DIAGRAM

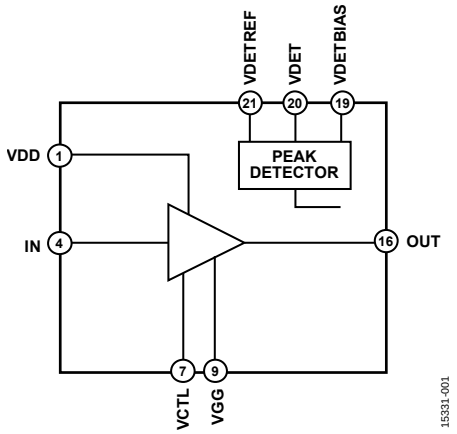

Figure 1.

GENERAL DESCRIPTION

The HMC7144 is a broadband driver amplifier for electro-absorption modulated lasers (EML). The device supports data rates up to 28 Gbps to meet 100 Gbps Ethernet system requirements. The device provides module designers with a scalable power dissipation for varying drive voltage characteristics of different modulators; the power consumption of the module can be set as low as 0.12 W to 0.5 W at 1.5 V p-p and 2.2 V p-p output amplitudes, respectively.

The HMC7144 supports a wide range of supply voltages from 3.5 V to 7 V and delivers excellent time domain performance. The driver incorporates the unique peak detector with reference feature that enables continuous output amplitude monitoring without the need for external high frequency circuitry. The output amplitude and crosspoint are adjustable via control pins. The input and output are 50 Ω and require ac coupling.

The HMC7144 is housed in a robust, leadless, 4 mm × 4 mm ceramic LCC package.

Rev. C
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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Last Content Update: 02/23/2017

COMPARABLE PARTS

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- HMC7144LC4 Evaluation Board

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- HMC7144 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

12/2016—v02.0314 to Rev. C

Changes to Features, Applications, and General Description Section 1
Changes to Table 3 4
Changes to Table 4 5
Changes to Table 5 6
Changes to Device Power-Up Section 11

SPECIFICATIONS

3.5 V ELECTRICAL SPECIFICATIONS

V_{DD} = 3.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM DATA RATE			28	32	Gbps
GAIN	DC to 10 GHz	10	13	13.8	dB
	10 GHz to 20 GHz	11.8	12.8	13.5	dB
	20 GHz to 30 GHz	5.8	8.8	13	dB
RETURN LOSS					
Input	DC to 10 GHz		−13	−10	dB
	10 GHz to 20 GHz		−16	−9	dB
	20 GHz to 30 GHz		−18	−4	dB
Output	DC to 10 GHz		−23	−15	dB
	10 GHz to 20 GHz		−21	−13	dB
	20 GHz to 30 GHz		−18	−11	dB
GROUP DELAY VARIATION	DC to 10 GHz		±5		ps
	10 GHz to 20 GHz		±10		ps
	20 GHz to 30 GHz		±22		ps
ADJUSTABLE OUTPUT SWING RANGE	Data input = 28 Gbps nonreturn to zero (NRZ) pseudo-random binary sequence (PRBS) 23^1 − 1 pattern, 0.5 V p-p	0.9		1.5	V p-p
TIMING	Data input = 28 Gbps NRZ PRBS 23^1 − 1 pattern, 0.5 V p-p				
Rise	20% to 80%		14.5		ps
Fall	20% to 80%		16.2		ps
JITTER					
Additive RMS Jitter[1]	Data input = 28 Gbps NRZ PRBS 23^1 − 1 pattern, 0.5 V p-p	240	270	320	f_S
Deterministic				2	ps
SIGNAL-TO-NOISE RATIO (SNR)	Data input = 28 Gbps NRZ PRBS 23^1 − 1 pattern, 0.5 V p-p		23		dB
SUPPLY CURRENT (I_{DD})		40	45	55	mA
BIAS CURRENT ADJUST/CROSSPOINT ADJUST					
Bias Voltage (V_{GG})		−1.5	−0.9	−0.5	V
Bias Current (I_{GG})				1	mA
OUTPUT AMPLITUDE ADJUST					
Voltage (V_{CTL})		−1	−0.2	+0.5	V
Current (I_{CTL})				1	mA
CROSSPOINT RANGE[2]		45	50	55	%
PEAK DETECT SENSITIVITY	R_{LOAD} = 10 MΩ at VDET and VDETREF	75	85	95	mV/V

[1] Additive rms jitter is calculated by $J_{RMS\ DUT} = \sqrt{((J_{TESTED})^2 - (J_{SOURCE})^2)}$ with 28 Gbps 10101 … pattern, 0.5 V p-p.
[2] Adjust V_{GG} between −1 V and 0 V to achieve the desired crosspoint percentage.

5.0 V ELECTRICAL SPECIFICATIONS

V_{DD} = 5.0 V, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM DATA RATE			28	32	Gbps
GAIN	DC to 10 GHz	11	15	16	dB
	10 GHz to 20 GHz	10	14	15	dB
	20 GHz to 30 GHz	7	12	13	dB
RETURN LOSS					
Input	DC to 10 GHz		−13	−10	dB
	10 GHz to 20 GHz		−14	−10	dB
	20 GHz to 30 GHz		−16	−7	dB
Output	DC to 10 GHz		−23	−10	dB
	10 GHz to 20 GHz		−21	−10	dB
	20 GHz to 30 GHz		−15	−7	dB
GROUP DELAY VARIATION	DC to 10 GHz		±6		ps
	10 GHz to 20 GHz		±10		ps
	20 GHz to 30 GHz		±20		ps
ADJUSTABLE OUTPUT SWING RANGE	Data input = 28 Gbps NRZ PRBS 23[1] − 1 pattern, 0.5 V p-p	1.2		2.2	V p-p
TIMING	Data input = 28 Gbps NRZ PRBS 23[1] − 1 pattern, 0.5 V p-p				
Rise	20% to 80%		15		ps
Fall	20% to 80%		16		ps
JITTER					
Additive RMS Jitter[1]	Data input = 28 Gbps NRZ PRBS 23[1] − 1 pattern, 0.5 V p-p	240	250	310	f_S
Deterministic				2	ps
SIGNAL-TO-NOISE RATIO (SNR)	Data input = 28 Gbps NRZ PRBS 23[1] − 1 pattern, 0.5 V p-p		22		dB
SUPPLY CURRENT (I_{DD})		50	70	80	mA
BIAS CURRENT ADJUST/CROSSPOINT ADJUST					
Gate Bias Voltage (V_{GG})		−1.5	−0.85	−0.5	V
Gate Bias Current (I_{GG})				1	mA
OUTPUT AMPLITUDE ADJUST					
Control Bias Voltage (V_{CTL})		−1	0	+0.5	V
Control Bias Current (I_{CTL})				1	mA
CROSSPOINT RANGE[2]		45	50	55	%
PEAK DETECT SENSITIVITY	R_{LOAD} = 10 MΩ at VDET and VDETREF	75	85	95	mV/V

[1] Additive rms jitter is calculated by $J_{RMS\ DUT} = \sqrt{((J_{TESTED})^2 - (J_{SOURCE})^2)}$ with 28 Gbps 10101 … pattern, 0.5 V p-p.
[2] Adjust V_{GG} between −1 V and 0 V to achieve the desired crosspoint percentage.

TYPICAL BIAS VOLTAGES

Input data amplitude = 500 mV p-p.

Table 3.

Parameter	V_{CTL}	V_{GG}	I_{DD}
V_{DD}			
3.5 V	−0.4 V	−0.9 V	45 mA
4. 0 V	−0.4 V	−0.85 V	53 mA
5.0 V	0 V	−0.85 V	70 mA
6.0 V	−0.2 V	−0.8 V	76 mA
7.0 V	−0.2 V	−0.8 V	92 mA
	−0.2 V	Set to get I_{DD}	120 mA[1]

[1] This value denotes the worst case operating conditions with a maximum case temperature of 87°C.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Drain Bias Voltage (V_{DD}) Range	12 V
Gate Bias Voltage (V_{GG})	
Minimum	−1.5 V
Maximum	0 V
Control Bias Voltage (V_{CTL})	
Minimum	−1.5 V
Maximum	2.0 V
Maximum Detector Bias Voltage ($V_{DETBIAS}$)	2.5 V
Input Voltage Swing (V_{IN})	2 V p-p
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +87°C
Maximum Peak Reflow Temperature	260°C
Channel Temperature	137°C
Thermal Resistance (Channel to Ground Pad)	56.58°C/W
ESD Sensitivity (Human Body Model)	Class 1A

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

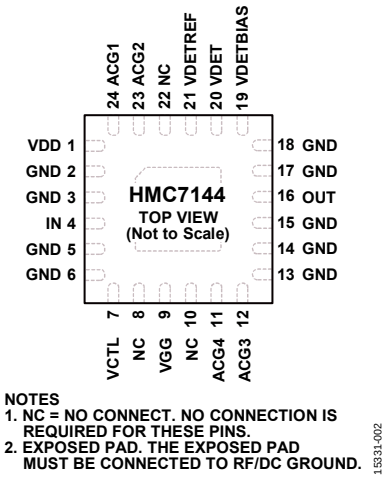

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD	Supply Voltage.
2, 3, 5, 6, 13 to 15, 17, 18	GND	Ground. These pins and the die bottom must be connected to RF/dc ground. See Figure 3 for the GND interface schematic.
4	IN	Input. Pin 4 is dc-coupled and matched to 50 Ω (see Figure 6).
7	VCTL	Gate Control Voltage. This pin controls the output voltage swing of the amplifier. The typical value for VCTL is −0.2 V. See Figure 5.
8, 10, 22	NC	No Connect. No connection is required for these pins.
9	VGG	Gate Control Voltage, Current.
11	ACG4	Low Frequency Termination. Attach bypass capacitors per the application circuit shown in Figure 5.
12	ACG4	Low Frequency Termination. Attach bypass capacitors per the application circuit shown in Figure 5.
16	OUT	Output. Pin 16 is decoupled and matched to 50 Ω (see Figure 7). The data polarity of the OUT pin is the inverse of the data polarity on the IN pin.
19	VDETBIAS	Detector Bias Voltage. Set Pin 19 to 1.2 V (see Figure 7).
20	VDET	Detector Output Voltage.
21	VDETREF	Detector Reference Voltage (see Figure 7).
23	ACG2	Low Frequency Termination. Attach bypass capacitors per the application circuit shown in Figure 4.
24	ACG1	Low Frequency Termination. Attach bypass capacitors per the application circuit shown in Figure 4.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

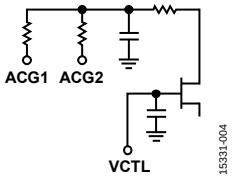

Figure 4. ACG1, ACG2, and VCTL Interface Schematic

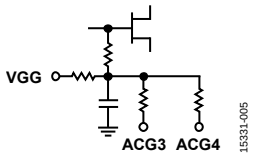

Figure 5. ACG3, ACG4, and VGG Interface Schematic

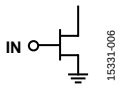

Figure 6. IN Interface Schematic

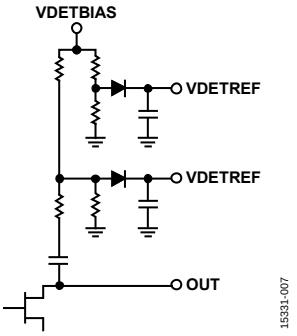

Figure 7. VDETBIAS, VDETREF, and OUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

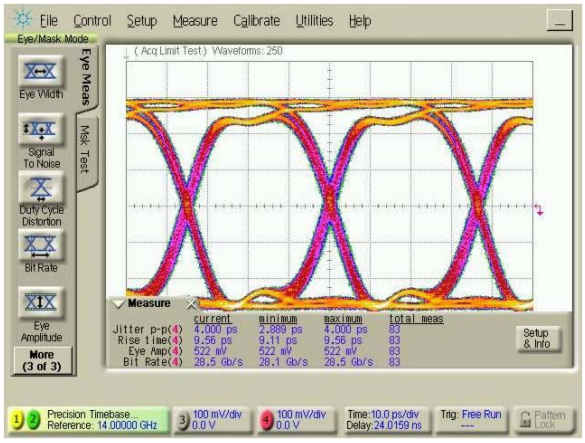

Figure 8. 28 Gbps NRZ PRBS $2^{31} - 1$ Pattern Input Data, Input Eye Diagram, V_{IN} = 510 mV p-p

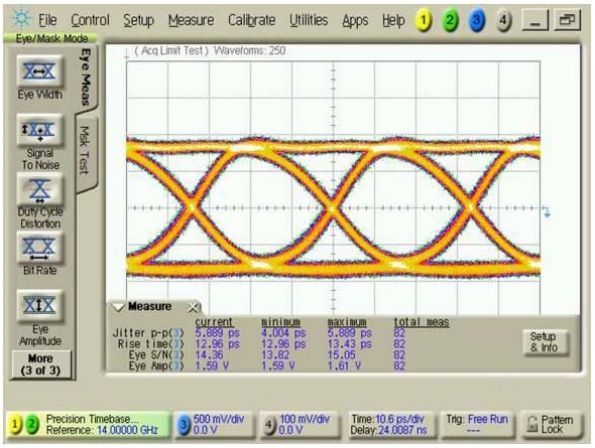

Figure 9. 28 Gbps Output Eye Diagram at V_{DD} = 3.5 V, V_{CTL} = −0.3 V, V_{GG} = −0.9 V, I_{DD} = 44 mA, V_{OUT} = 1.59 V p-p, P_{DISS} = 0.15 W

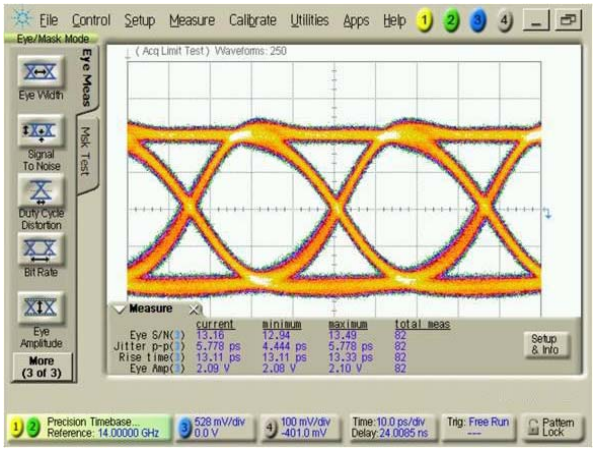

Figure 10. 28 Gbps Output Eye Diagram at V_{DD} = 5.0 V, V_{CTL} = −0.05 V, V_{GG} = −0.85 V, I_{DD} = 64 mA, V_{OUT} = 2.09 V p-p, P_{DISS} = 0.32 W

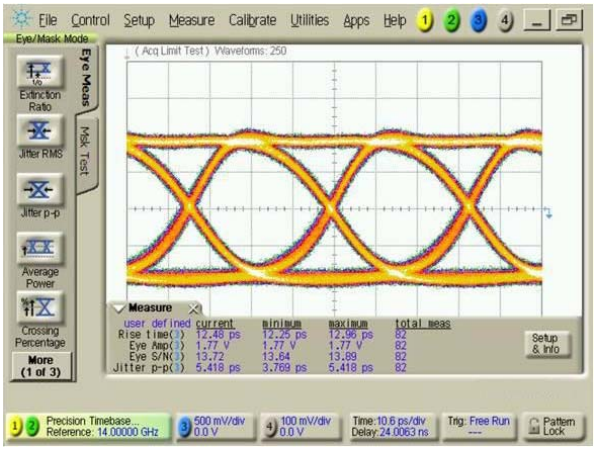

Figure 11. 28 Gbps Output Eye Diagram at V_{DD} = 4.0 V, V_{CTL} = −0.2 V, V_{GG} = −0.89 V, I_{DD} = 50 mA, V_{OUT} = 1.77 V p-p, P_{DISS} = 0.20 W

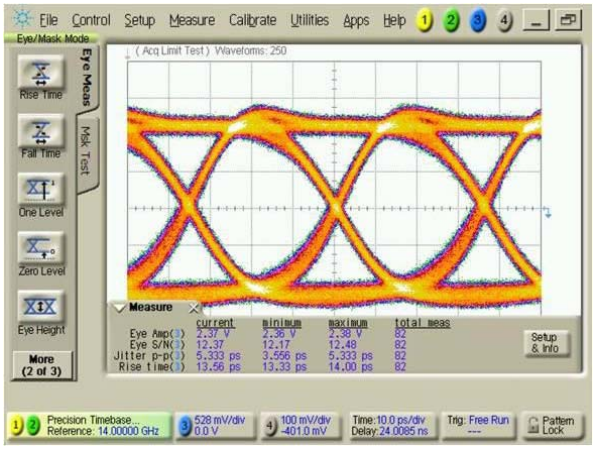

Figure 12. 28 Gbps Output Eye Diagram at V_{DD} = 6.0 V, V_{CTL} = −0.03 V, V_{GG} = −0.81 V, I_{DD} = 79 mA, V_{OUT} = 2.37 V p-p, P_{DISS} = 0.47 W

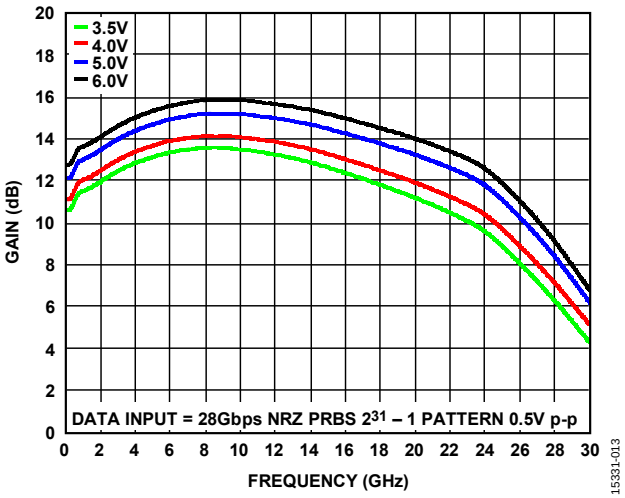

Figure 13. Gain over Supply, V_{GG} = −0.90 V

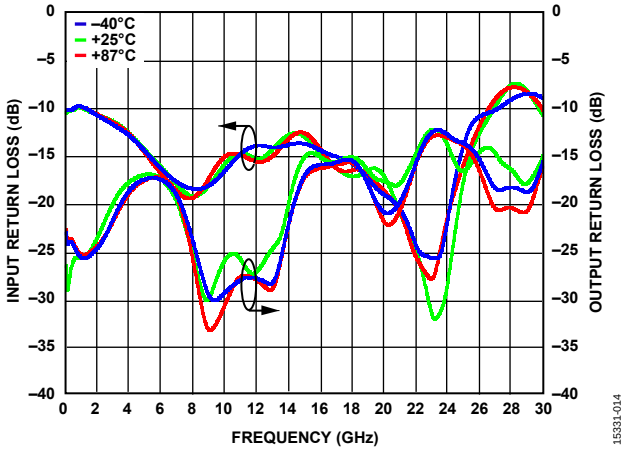

Figure 14. Input and Output Return Loss over Temperature, V_{DD} = 5 V (See Table 3 for Typical Bias Voltages)

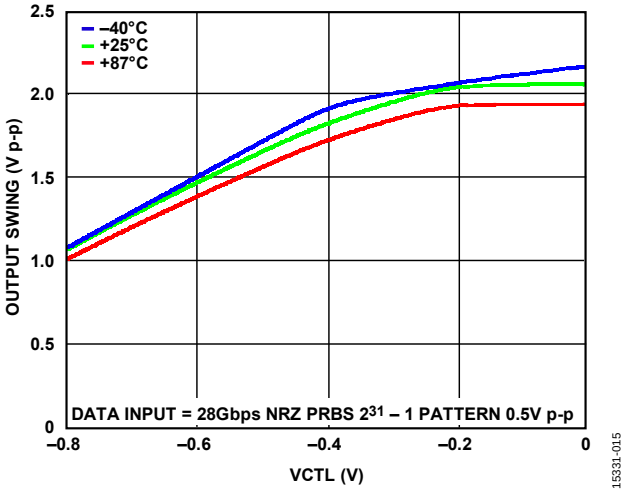

Figure 15. Output Swing vs. VCTL over Temperature, V_{GG} = –0.90 V, Data Input = 28 Gbps NRZ PRBS 23^1 – 1 Pattern, 0.5 V p-p, V_{DD} = 5 V (See Table 3 for Typical Bias Voltages)

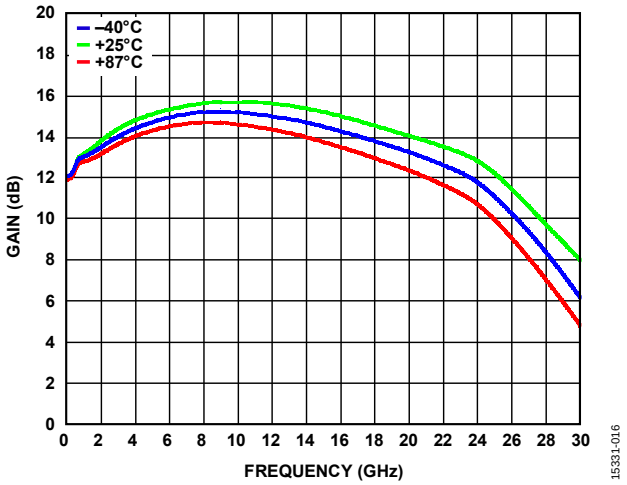

Figure 16. Gain over Temperature, V_{DD} = 5 V (See Table 3 for Typical Bias Voltages)

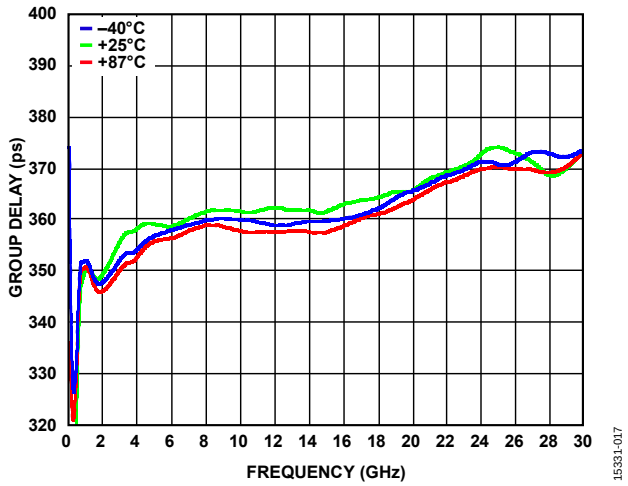

Figure 17. Group Delay vs. Frequency over Temperature, V_{GG} = –0.90 V, V_{DD} = 5 V (See Table 3 for Typical Bias Voltages)

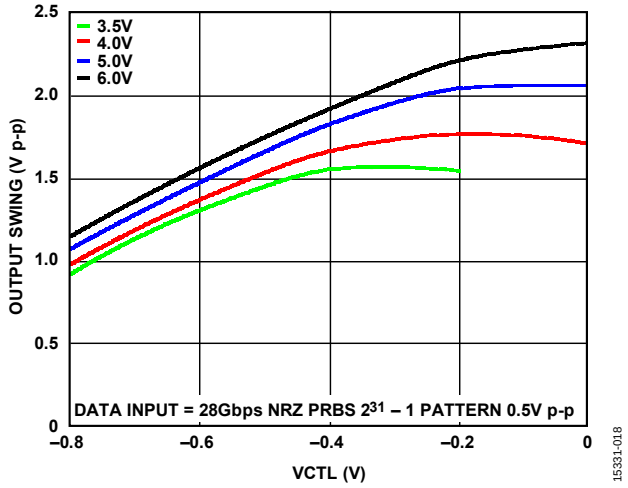

Figure 18. Output Swing vs. VCTL over Supply, V_{GG} = –0.90 V, Data Input = 28 Gbps NRZ PRBS 23^1 – 1 Pattern, 0.5 V p-p

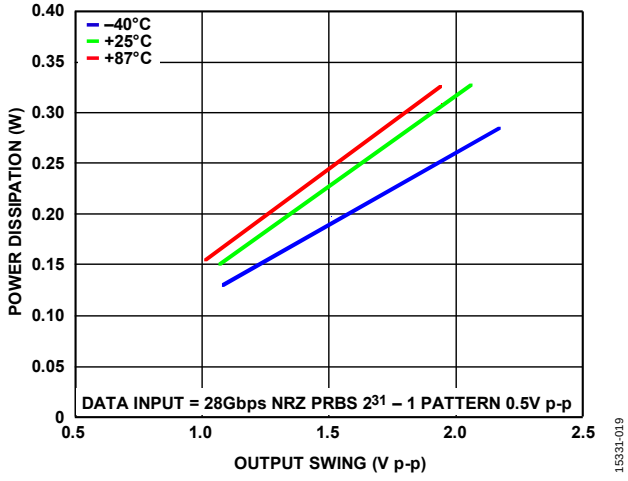

Figure 19. Power Dissipation vs. Output Swing over Temperature, V_{DD} = 5 V (See Table 3 for Typical Bias Voltages), Data Input = 28 Gbps NRZ PRBS 23^1 – 1 Pattern, 0.5 V p-p

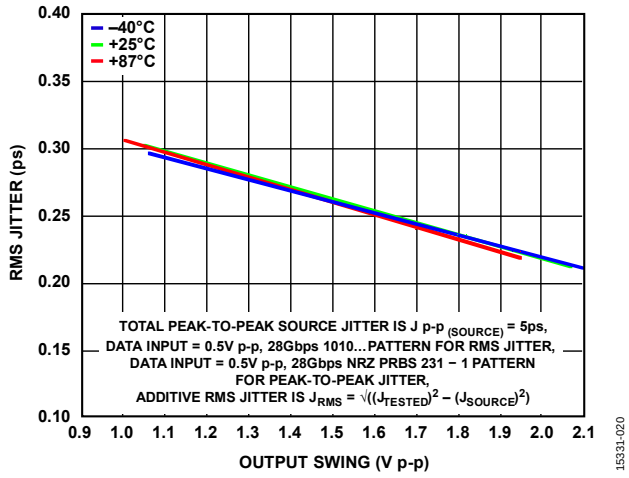

Figure 20. RMS Jitter vs. Output Swing over Temperature, V_{DD} = 5 V (See Table 3 for Typical Bias Voltages), Total Peak-to-Peak Source Jitter is $J_{p-p(SOURCE)}$ = 5 ps, Data Input = 0.5 V p-p, 28 Gbps 1010 … Pattern for RMS Jitter, Data Input = 0.5 V p-p, 28 Gbps NRZ PRBS $2^{31} - 1$ Pattern for Peak-To-Peak Jitter, Additive RMS Jitter is $J_{RMS} = \sqrt{((J_{TESTED})^2 - (J_{SOURCE})^2)}$

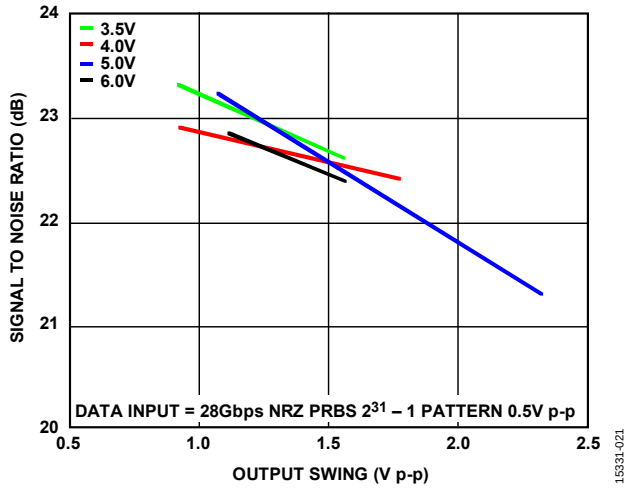

Figure 21. Signal-to-Noise Ratio vs. Output Swing over Supply, V_{GG} = –0.90 V, Data Input = 28 Gbps NRZ PRBS $2^{31} - 1$ Pattern, 0.5 V p-p

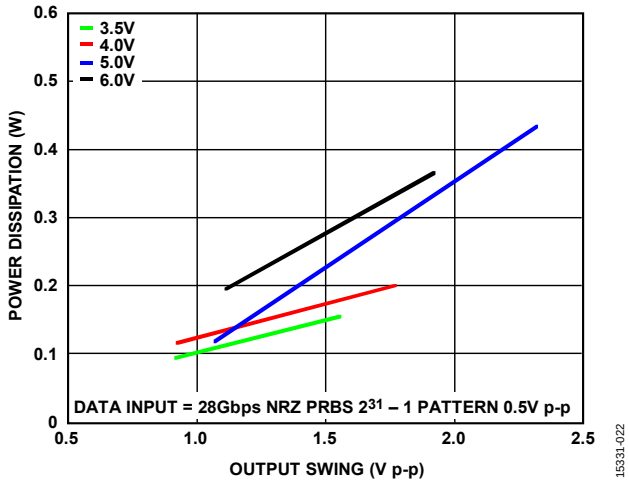

Figure 22. Power Dissipation vs. Output Swing over Supply, V_{GG} = –0.90 V, Data Input = 28 Gbps NRZ PRBS $2^{31} - 1$ Pattern, 0.5 V p-p

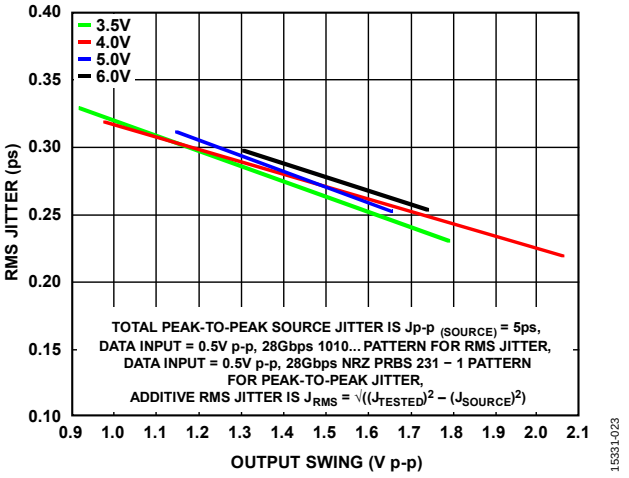

Figure 23. RMS Jitter vs. Output Swing over Supply, V_{GG} = –0.90 V, Total Peak-to-Peak Source Jitter is $J_{p-p(SOURCE)}$ = 5 ps, Data Input = 0.5 V p-p, 28 Gbps 1010 … Pattern for RMS Jitter, Data Input = 0.5 V p-p, 28 Gbps NRZ PRBS $2^{31} - 1$ Pattern for Peak-To-Peak Jitter, Additive RMS Jitter is $J_{RMS} = \sqrt{((J_{TESTED})^2 - (J_{SOURCE})^2)}$

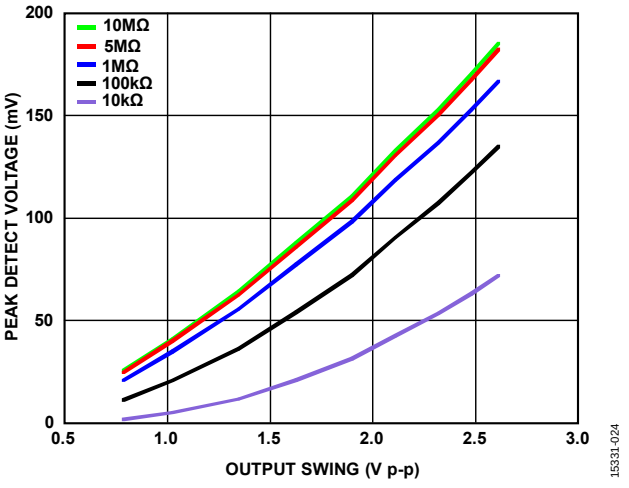

Figure 24. Peak-Detect Voltage vs. Output Swing over R_{LOAD}, V_{DD} = 5 V (See Table 3 for Typical Bias Voltages), VDETBIAS = 1.2 V, Peak Detect Voltage = VDET – VDETREF, R_{LOAD} is Equivalent Resistance to GND at VDET and VDETREF Pins

APPLICATIONS INFORMATION

DEVICE OPERATION

The HMC7144 is susceptible to damage from electrostatic discharge. Observe proper precautions during handling, assembly, and test.

DEVICE POWER-UP

To power-up the device properly, take the following steps:

1. Ground the device.
2. Set VGG to −1.3 V to ensure the device is turned off when supply is applied in Step 4 (no drain current).
3. Set VCTL to its typical value (see Table 3, no drain current).
4. Set VDD to its typical value (see Table 3, no drain current).
5. Increase VGG until the supply current (I_{DD}) reaches its desired value.
6. Make necessary adjustments, as follows:
   a. VGG can be adjusted to obtained the desired eye crossing point percentage.
   b. VCTL can be adjusted to set the desired output voltage swing.
   c. VDD can be further adjusted to optimize the power consumption and the output voltage swing.

Note that Step 2 and Step 3 can be performed at the same time, or Step 3 can be performed before Step 2.

DEVICE POWER-DOWN

Reverse Step 1 through Step 4 listed in the Device Power-Up section.

APPLICATION CIRCUIT

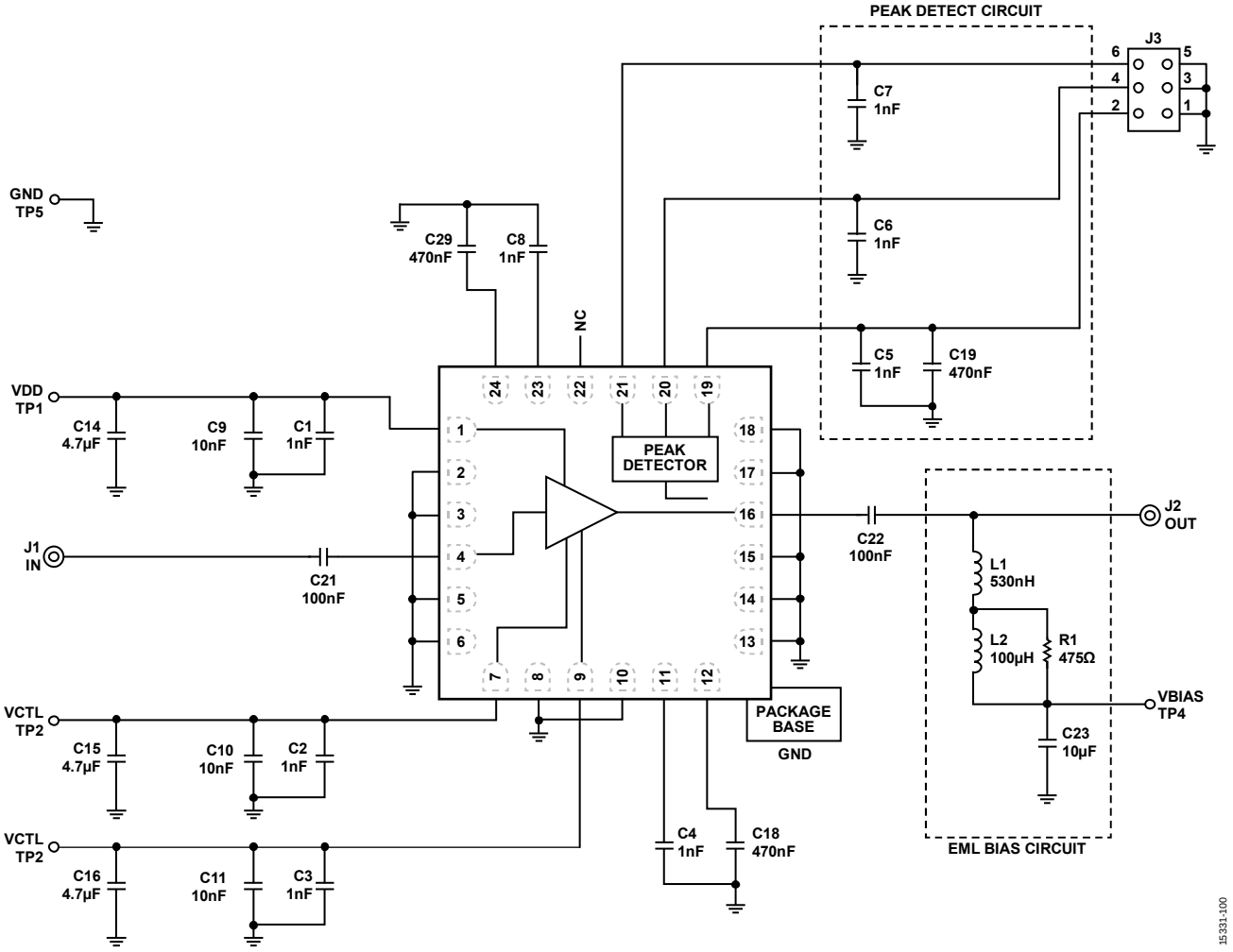

Figure 25. Evaluation Board Schematic

EVALUATION PRINTED CIRCUIT BOARD (PCB)

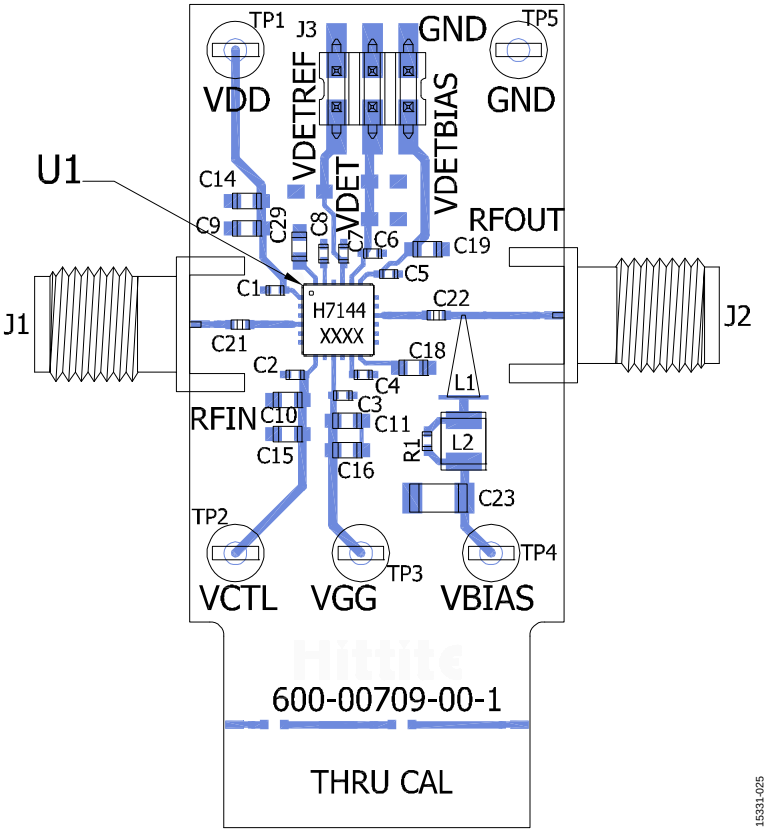

Figure 26. EVAL01-HMC7144LC4 Evaluation PCB

Table 6. Bill of Materials for the EVAL01-HMC7144LC4 Evaluation Board[1]

Item	Description
J1, J2	K connector
J3	2 mm, 6-pin SMT header
TP1 to TP5	DC test point
C1 to C8	1000 pF capacitor, 0402 package
C9 to C11	10 nF capacitor, 0603 package
C14 to C16	4.7 µF capacitor, 0603 package
C18 to C19, C29	0.47 µF capacitor, 0603 package
C21, C22	47,000 pF capacitor, 0402 package
C23	10 µF capacitor, 1206 package
L1	0.53 µH inductor, conical package
L2	100 µH inductor, 1210 package
U1	HMC7144, 28 Gbps, EML driver with peak detector
PCB	600-00709-00-1 evaluation board, circuit board material is Rogers 4350 or Arlon 25 FR

[1] Reference this number to order the full evaluation PCB.

The board in this application uses radio frequency (RF) circuit board design techniques. Provide 50 Ω impedance for the signal lines and connect the package ground leads and exposed pad directly to the ground plane, similar to that shown in Figure 26. Use a sufficient number of via holes to connect the top and bottom ground planes.

OUTLINE DIMENSIONS

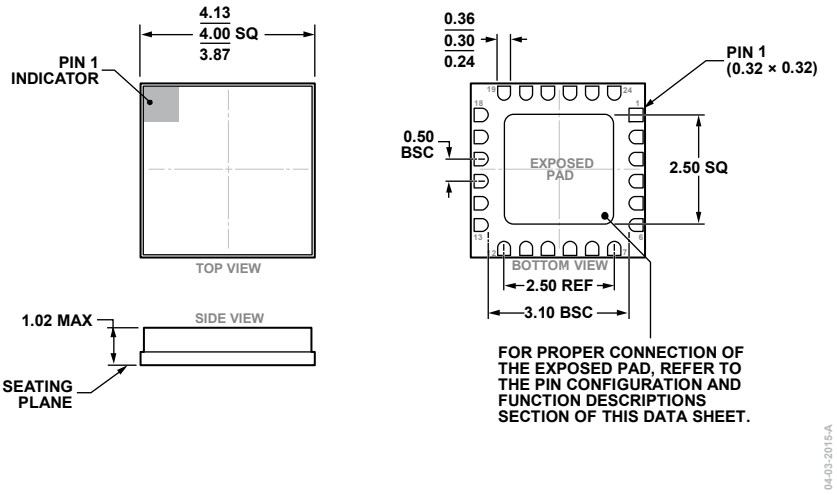

Figure 27. 24-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-24-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	MSL Rating[1]	Package Description[2]	Package Option	Branding[3]
HMC7144LC4	−40°C to +87°C	MSL3	24-Terminal Ceramic Leadless Chip Carrier Package [LCC], 50 Pieces Reel	E-24-1	H7144 XXXX
HMC7144LC4TR	−40°C to +87°C	MSL3	24-Terminal Ceramic Leadless Chip Carrier Package [LCC], 100 Pieces Reel	E-24-1	H7144 XXXX
HMC7144LC4TR-R5	−40°C to +87°C	MSL3	24-Terminal Ceramic Leadless Chip Carrier Package [LCC], 500 Pieces Reel	E-24-1	H7144 XXXX
EVAL01-HMC7144LC4			Evaluation Board		

[1] See the Absolute Maximum Ratings section.
[2] Package body material is alumina, white. Lead finish is gold over nickel.
[3] XXXX is the 4-digit lot number.