Low Skew CMOS 8-Bit Buffers/Line Drivers

QS5244

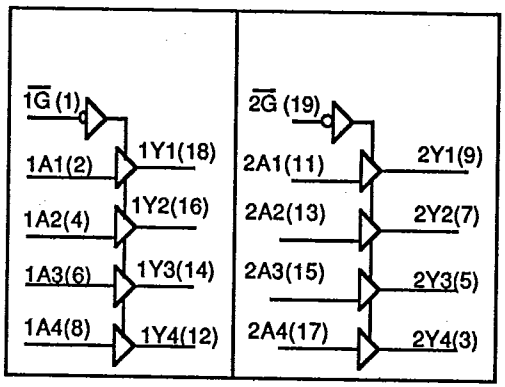
FEATURES/BENEFITS

- 0.5 ns on-chip skew (same trans.)
- 244 compatible pinout and function
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Undershoot clamp diodes on all inputs
- 1.2ns on-chip skew (opposite trans.)
- 1.5ns skew between chips
- CMOS power levels: <7.5 mW static
- Available in PDIP, ZIP, SOIC, QSOP, CERDIP
- 4.1 ns propagation delay

DESCRIPTION

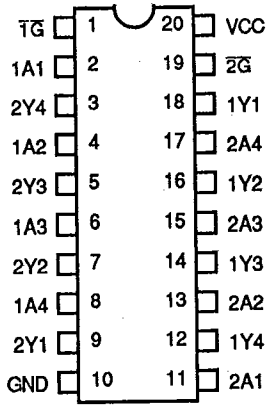
The QS5244 is an 8-bit buffers/line driver with three-state outputs that are ideal for driving high-capacitance loads as in memory address and data buses. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PINOUT

PDIP, SOIC, QSOP



ALL PINS TOP VIEW

FUNCTION TABLES

$\overline{1G}$ / $\overline{2G}$	Input A	Output Y
H	X	Z
L	L	L
L	H	H

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
DC Output Voltage V_O ..... -0.5V to 7.0V
DC Input Voltage V_I ..... -0.5V to 7.0V
AC Input Voltage (for a pulse width ≤20 ns)..... -3.0V
DC Input Diode Current with V_I<0.....-20 mA
DC Output Diode Current with V_O <0..... -50 mA
DC Output Current Max. sink current/pin..... 120 mA
Maximum Power Dissipation.....0.5 watts
T_{STG}Storage Temperature..... -65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pins	SOIC	QSOP	PDIP,LCC	ZIP	Unit
1,19	4	4	5	7	pF
-------	6	6	7	9	pF
2-9,11-18	8	8	9	10	pF

Note: Capacitance is characterized but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%

Symbol	Parameter	Test Conditions		Min	Typ (1)	Max	Unit
Vih	Input High Voltage	Logic HIGH for All Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Logic LOW for All Inputs		-	-	0.8	
ΔVt	Input Hysterisis	Vtlh - Vthl for All Inputs		-	0.2	-	
|Iih| |Iil|	Input Current Input HIGH or LOW	Vcc = MAX	0 ≤ Vin < Vcc	-	-	5	µA
|Ioz|	Off State Output Current (Hi-Z)	Vcc = MAX, 0 ≤ Vin ≤ Vcc		-	-	5	
Ios	Short Circuit Current	Vcc = MAX, Vo = GND (2,3)		-60	-	-255	mA
Vic	Input Clamp Voltage	Vcc = MIN, Iin = 18 mA (3)		-	-0.7	-1.2	Volts
Voh	Output HIGH Voltage	Vcc = MIN	Ioh = 12 mA (MIL)	2.4	-	-	Volts
			Ioh = 15 mA (COM)	2.4	-	-	
Vol	Output LOW Voltage	Vcc = MIN	Iol = 48 mA (MIL)	-	-	0.55	
			Iol = 64 mA (COM)	-	-	0.55	

Notes:
1. Typical values indicate V_{CC}=5.0V and T_A=25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = MAX, freq = 0 0V≤Vin≤0.2V or Vcc-0.2V≤Vin≤Vcc	-	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = MAX, Vin =3.4 V, freq = 0 (2)	-	2.0	
Qccd	Supply Current per input per mHz	Vcc = MAX, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or Vcc (3,4)	-	0.25	mA/ MHz

1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (Vi=3.4V)
3. For flipflops Qccd is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±5% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%
Cload = 50 pF, Rload = 500Ω unless otherwise noted

Symbol	Description		Notes	807T		Unit
				Min	Max	
t PHL t PLH	Propagation Delay Ai to Yi	COM	1	1.5	4.1	ns
t PZH t PZL	Output Enable Time $\overline{OE}$ to Yi	COM	1	1.5	5.6	
t PHZ t PLZ	Output Disable Time $\overline{OE}$ to Yi	COM	1,2	1.5	5.2	
tSK1	Skew between two outputs (same transition)	COM	2		0.5	
tSK2	Skew between two outputs (opposite transition, same device	COM	2		1.2	
tSK3	Skew between two outputs of different devices	COM	2		1.5	

Notes:
1. Minimum propagation delay values are guaranteed but not tested.
2. This parameter is guaranteed but not tested.