Rochester Electronics

Datasheet

PART NUMBER

54HC390BEA-ROCV

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Rochester Electronics®

Datasheet

54HC390

Dual Binary Counter with Divide By 2 and Divide By 5 Sections

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- ISO-9001
- AS9120 certification
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    - Class Q Military
    - Class V Space Level
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FOR REFERENCE ONLY

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Convert to Military Drawing format. Add vendor CAGE 27014 for device type 01	87-01-09	N A Hauck
B	Add case 2 for approved source 27014. Add one approved source 01295 for cases E and 2	87-08-25	N A Hauck
C	Delete vendor CAGE 18714. Technical and editorial changes throughout	91-11-05	M. A. Frye
D	Update boilerplate to current MIL-PRF-38535 requirements. – MAA	08-06-25	Thomas M. Hess
E	Update boilerplate paragraphs to current MIL-PRF-38535 requirements. – jwc	16-03-23	Thomas M. Hess

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			E	E	E	E	E	E	E	E	E	E	E	E	E	
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

PREPARED BY
Jeffery Tunstall

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

CHECKED BY
D A Di Cenzo

APPROVED BY
N A Hauck

ORIGINAL DRAWING APPROVAL DATE
86-01-29

MICROCIRCUIT, DIGITAL, HIGH-SPEED CMOS, DUAL BINARY COUNTER, MONOLITHIC SILICON

REVISION LEVEL
E

SIZE	CAGE CODE	
A	**67268**	**86009**

AMSC N/A

SHEET 1 OF 13

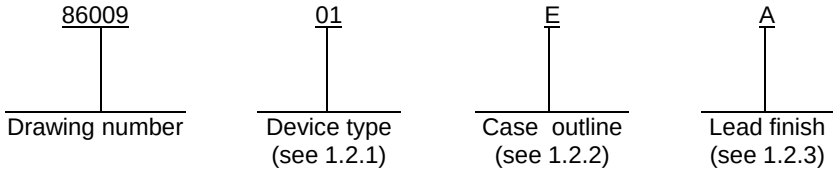
DSCC FORM 2234
APR 97

5962-E274-16

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC390	Dual binary counter with divide by 2 and divide by 5 sections

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535,appendix A

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
Input clamp diode current (I_{IK})	±20 mA
DC output current (per pin) (I_{OK})	±25 mA
DC V_{CC} or GND current (per pin)	±50 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	-500 mW 4/
Lead temperature (soldering 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+2.0 V dc min. to +6.0 V dc max.
Input voltage range (V_{IN})	0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	0.0 V dc to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Input rise or fall time (t_r, t_f):	
V_{CC} = 2.0 V	0 to 500 ns
V_{CC} = 4.5 V	0 to 500 ns
V_{CC} = 6.0 V	0 to 400 ns
Minimum recovery time, reset (t_{rec}):	
For T_C = 25°C,	
V_{CC} = 2.0 V	50 ns
V_{CC} = 4.5 V	10 ns
V_{CC} = 6.0 V	9 ns
For T_C = -55°C / +125°C,	
V_{CC} = 2.0 V	75 ns
V_{CC} = 4.5 V	15 ns
V_{CC} = 6.0 V	13 ns
Minimum width of clock or reset pulse (t_w):	
For T_C = 25°C,	
V_{CC} = 2.0 V	85 ns
V_{CC} = 4.5 V	17 ns
V_{CC} = 6.0 V	14 ns
For T_C = -55°C / +125°C,	
V_{CC} = 2.0 V	130 ns
V_{CC} = 4.5 V	26 ns
V_{CC} = 6.0 V	22 ns
Maximum clock frequency (f_{max}):	
For T_C = 25°C,	
V_{CC} = 2.0 V	5.4 MHz
V_{CC} = 4.5 V	27 MHz
V_{CC} = 6.0 V	32 MHz
For T_C = -55°C / +125°C,	
V_{CC} = 2.0 V	3.6 MHz
V_{CC} = 4.5 V	18 MHz
V_{CC} = 6.0 V	21 MHz

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case operating temperature range of -55°C to +125°C.
4/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 7A - Standard for Description of 54/74HCXXXX and 54/74HCTXXXX High-Speed CMOS Devices.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S Arlington, VA 22201-2107).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram(s). The logic diagram(s) shall be as specified on figure 2.

3.2.4 Truth table(s) and counting sequence diagram. The truth table(s) and counting sequence diagram shall be as specified on figure 3.

3.2.5 Switching waveforms. The switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	$V_{IN} = V_{IH}$ min. or V_{IL} max. $I_{OH} = -20$ µA	$V_{CC} = 2.0$ V	1, 2, 3	1.9		V
			$V_{CC} = 4.5$ V		4.4		
			$V_{CC} = 6.0$ V		5.9		
		$V_{IN} = V_{IH}$ min. or V_{IL} max. $I_{OH} = -4$ mA	$V_{CC} = 4.5$ V		3.7		
		$V_{IN} = V_{IH}$ min. or V_{IL} max. $I_{OH} = -5.2$ mA	$V_{CC} = 6.0$ V		5.2		
Low level output voltage	V_{OL}	$V_{IN} = V_{IH}$ min. or V_{IL} max. $I_{OL} = +20$ µA	$V_{CC} = 2.0$ V	1, 2, 3		0.1	V
			$V_{CC} = 4.5$ V			0.1	
			$V_{CC} = 6.0$ V			0.1	
		$V_{IN} = V_{IH}$ min. or V_{IL} max. $I_{OL} = +4$ mA	$V_{CC} = 4.5$ V			0.4	
		$V_{IN} = V_{IH}$ min. or V_{IL} max. $I_{OL} = +5.2$ mA	$V_{CC} = 6.0$ V			0.4	
High level input voltage	V_{IH}	2/	$V_{CC} = 2.0$ V	1, 2, 3	1.50		V
			$V_{CC} = 4.5$ V		3.15		
			$V_{CC} = 6.0$ V		4.2		
Low level input voltage	V_{IL}	2/	$V_{CC} = 2.0$ V	1, 2, 3		0.3	V
			$V_{CC} = 4.5$ V			0.9	
			$V_{CC} = 6.0$ V			1.2	
Input leakage current	I_{IN}	$V_{IN} = V_{CC}$ or GND $V_{CC} = 6.0$ V		1, 2, 3		±1.0	µA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND $V_{CC} = 6.0$ V		1, 2, 3		160	µA
Input capacitance	C_{IN}	$V_{IN} = 0.0$ V; See 4.4.1c		4		10	pF
Functional test		See 4.4.1d		7, 8			
Propagation delay time, Clock An to QAn 3/	t_{PHL1}, t_{PLH1}	$C_L = 50$ pF See figure 4	$V_{CC} = 2.0$ V	9		145	ns
				10, 11		220	
			$V_{CC} = 4.5$ V	9		29	
				10, 11		44	
			$V_{CC} = 6.0$ V	9		25	
				10, 11		38	
Propagation delay time, Clock Bn to QBn 3/	t_{PHL2}, t_{PLH2}	$C_L = 50$ pF See figure 4	$V_{CC} = 2.0$ V	9		155	ns
				10, 11		235	
			$V_{CC} = 4.5$ V	9		31	
				10, 11		47	
			$V_{CC} = 6.0$ V	9		26	
				10, 11		40	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, Clock Bn to QCn 3/	t_{PHL3}, t_{PLH3}	C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		210	ns
				10, 11		315	
			V_{CC} = 4.5 V	9		42	
				10, 11		63	
			V_{CC} = 6.0 V	9		36	
				10, 11		54	
Propagation delay time, Clock An to QDn 3/	t_{PHL4}, t_{PLH4}	C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		155	ns
				10, 11		235	
			V_{CC} = 4.5 V	9		31	
				10, 11		47	
			V_{CC} = 6.0 V	9		26	
				10, 11		40	
Propagation delay time, RESETn to any Qn 3/	t_{PHL5}	C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		165	ns
				10, 11		250	
			V_{CC} = 4.5 V	9		33	
				10, 11		50	
			V_{CC} = 6.0 V	9		28	
				10, 11		43	
Transition time 4/	t_{TLH}, t_{THL}	C_L = 50 pF See figure 4	V_{CC} = 2.0 V	9		75	ns
				10, 11		110	
			V_{CC} = 4.5 V	9		15	
				10, 11		22	
			V_{CC} = 6.0 V	9		13	
				10, 11		19	

1/ For a power supply of 5.0 V ±10% the worst case output voltage (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when design with this supply voltage. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V)

The worst case leakage current (I_{IN} , I_{CC} and I_{OZ}) occur for CMOS at the higher voltage, So V_{CC} = 6.0 V values should be used.

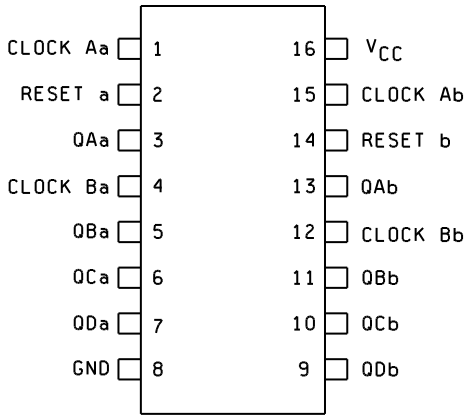
Power dissipation capacitance (C_{PD}) typically 40 pF, to determine the no load dynamic power consumption, $P_D = C_{PD} (V_{CC} \times V_{CC}) \times f + (I_{CC} \times V_{CC})$, and no load dynamic current consumption, $I_S = (C_{PD} \times V_{CC} \times f) + I_{CC}$

2/ V_{IH} and V_{IL} tests are not required if applied as forcing function for V_{OH} and V_{OL}.

3/ AC testing at V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed, if not tested to the specified parameters.

4/ Transition time (t_{TLH} and t_{THL}) shall be guaranteed, if not tested to the specified parameters.

CASE E



CASE 2

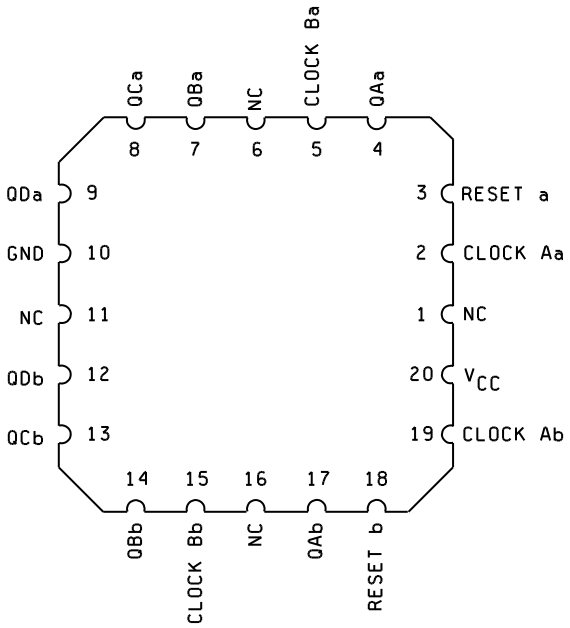


FIGURE 1. Terminal connections.

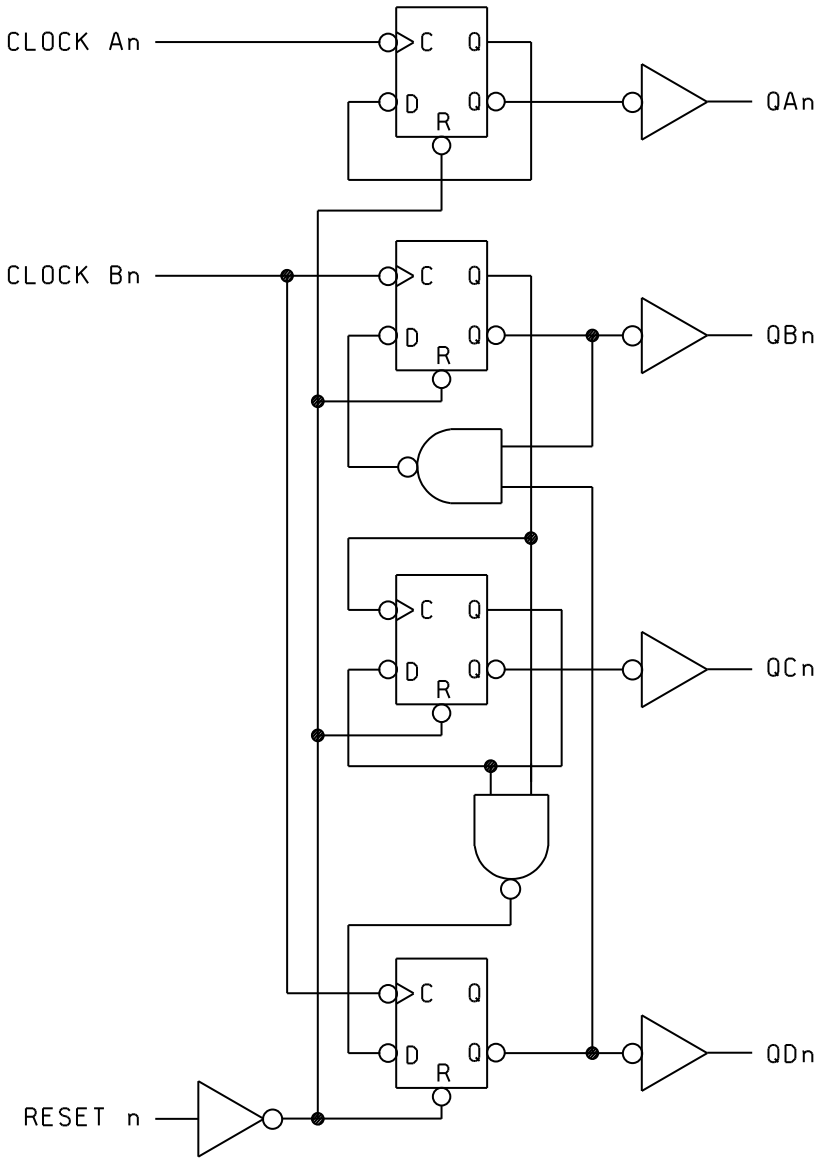
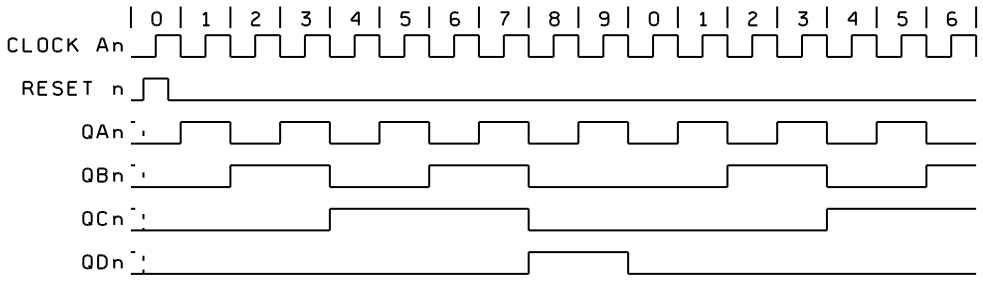


FIGURE 2. Logic diagram.



BIQUINARY COUNT SEQUENCE**

Count	Output			
	QAn	QDn	QCn	QBn
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

**Output QDn is connected to input clock A with counter input on clock Bn.

BCD COUNT SEQUENCE*

Count	Output			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

*Output QA is connected to clock B with counter input on clock An

FUNCTION TABLE

CLOCK		RESETn	ACTION
An	Bn		
X	X	H	Reset (÷2 and ÷5 counters)
⌥	X	L	Increment ÷2
X	⌥	L	Increment ÷5

L = Low level voltage
H = High level voltage
⌥ = High to low transition of clock
X = Don't care

FIGURE 3. Truth table and counting sequence.

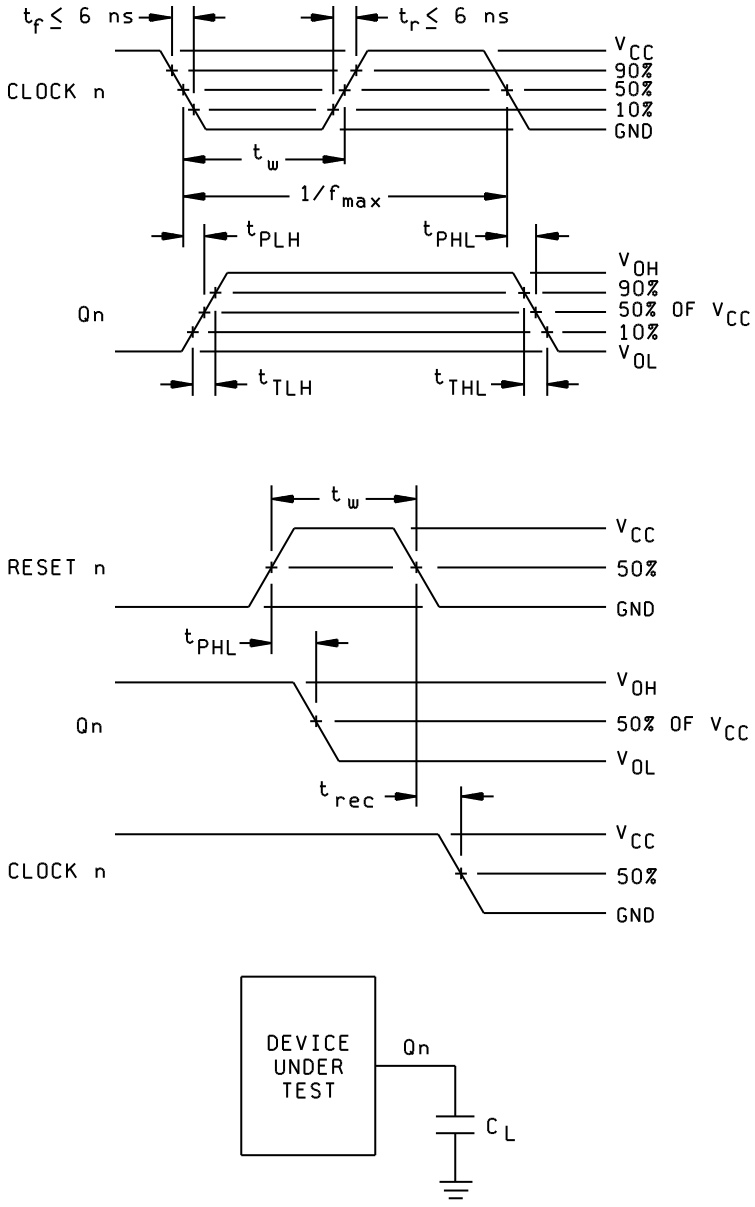


FIGURE 4. Switching waveforms

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,9
Group A test requirements (method 5005)	1,2,3,7,8,9,10**,11**
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.
** Subgroups 10 and 11 shall be guaranteed to the specified limits in the table I, if not tested.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-03-23

Approved sources of supply for SMD 86009 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Replacement military specification PIN
8600901EA	3V146	54HC390/BEA	M38510/66308BEX
	3/	SNJ54HC390J	
	3/	54HC390/BEAJC	
	3/	MM54HC390J/883	
	3/	CD54HC390F/3A	
86009012A	3V146	54HC390/B2A	M38510/66308B2X
	3/	SNJ54HC390FK	
	3/	54HC390M/B2CJC	
	3/	MM54HC390E/883	

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics Inc. 16 Malcolm Hoyt Drive Newburyport, MA 01950