HARRIS SEMICONDUCTOR

HFA3724

400MHz Quadrature IF Modulator/Demodulator

August 1997

Features

- Integrates all IF Transmit and Receive Functions
- Broad Frequency Range . . . . . .10MHz to 400MHz
- I/Q Amplitude and Phase Balance . . . . . 0.2dB, 2°
- 5th Order Programmable Low Pass Filter. . . . . .2.2MHz - 17.6MHz
- 400MHz Limiting IF Gain Strip with RSSI 84dB
- Low LO Drive Level . . . . . .-15dBm
- Fast Transmit-Receive Switching. 1µs
- Power Management/Standby Mode
- Single Supply 2.7V to 5.5V Operation

Applications

- Systems Targeting IEEE 802.11 Standard
- TDD Quadrature-Modulated Communication Systems
- Wireless Local Area Networks
- PCMCIA Wireless Transceivers
- ISM Systems
- TDMA Packet Protocol Radios
- PCS/Wireless PBX
- Wireless Local Loop

Description

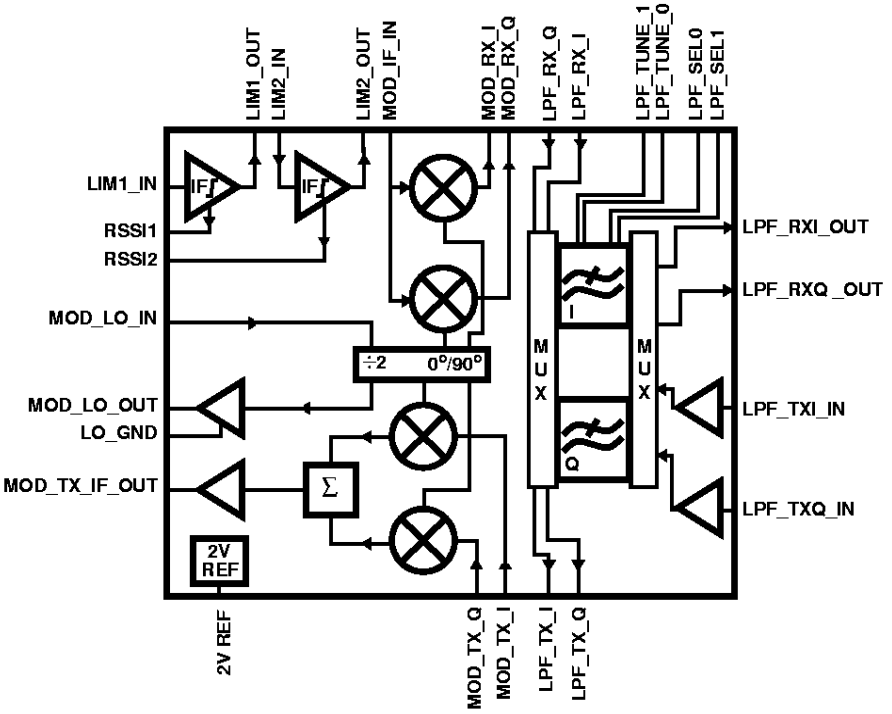
The Harris 2.4GHz PRISM™ chip set is a highly integrated five-chip solution for RF modems employing Direct Sequence Spread Spectrum (DSSS) signaling. The HFA3724 400MHz Quadrature IF Modulator/Demodulator is one of the five chips in the PRISM™ chip set (see the Typical Application Diagram).

The HFA3724 is a highly integrated baseband converter for quadrature modulation applications. It features all the necessary blocks for baseband modulation and demodulation of I and Q signals. It has a two stage integrated limiting IF amplifier with 84db of gain with a built in Receive Signal Strength Indicator (RSSI). Baseband antialiasing and shaping filters are integrated in the design. Four filter bandwidths are programmable via a two bit digital control interface. In addition, these filters are continuously tunable over a ±20% frequency range via one external resistor. The modulator channel receives digital I and Q data for processing. To achieve broadband operation, the Local Oscillator frequency input is required to be twice the desired frequency of modulation/demodulation. A selectable buffered divide by 2 LO output and a stable reference voltage are provided for convenience of the user. The device is housed in a thin 80 lead TQFP package well suited for PCMCIA board applications.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3724IN	-40 to 85	80 Ld TQFP	Q80.14x14
HFA3724IN96	-40 to 85	Tape and Reel	

Simplified Block Diagram



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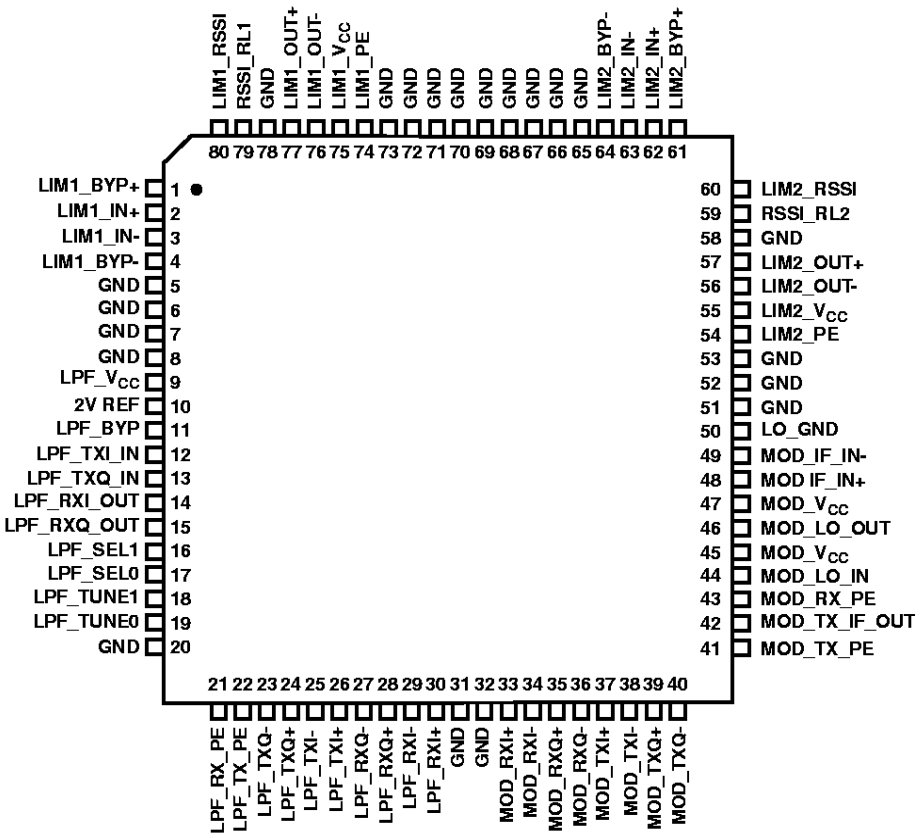
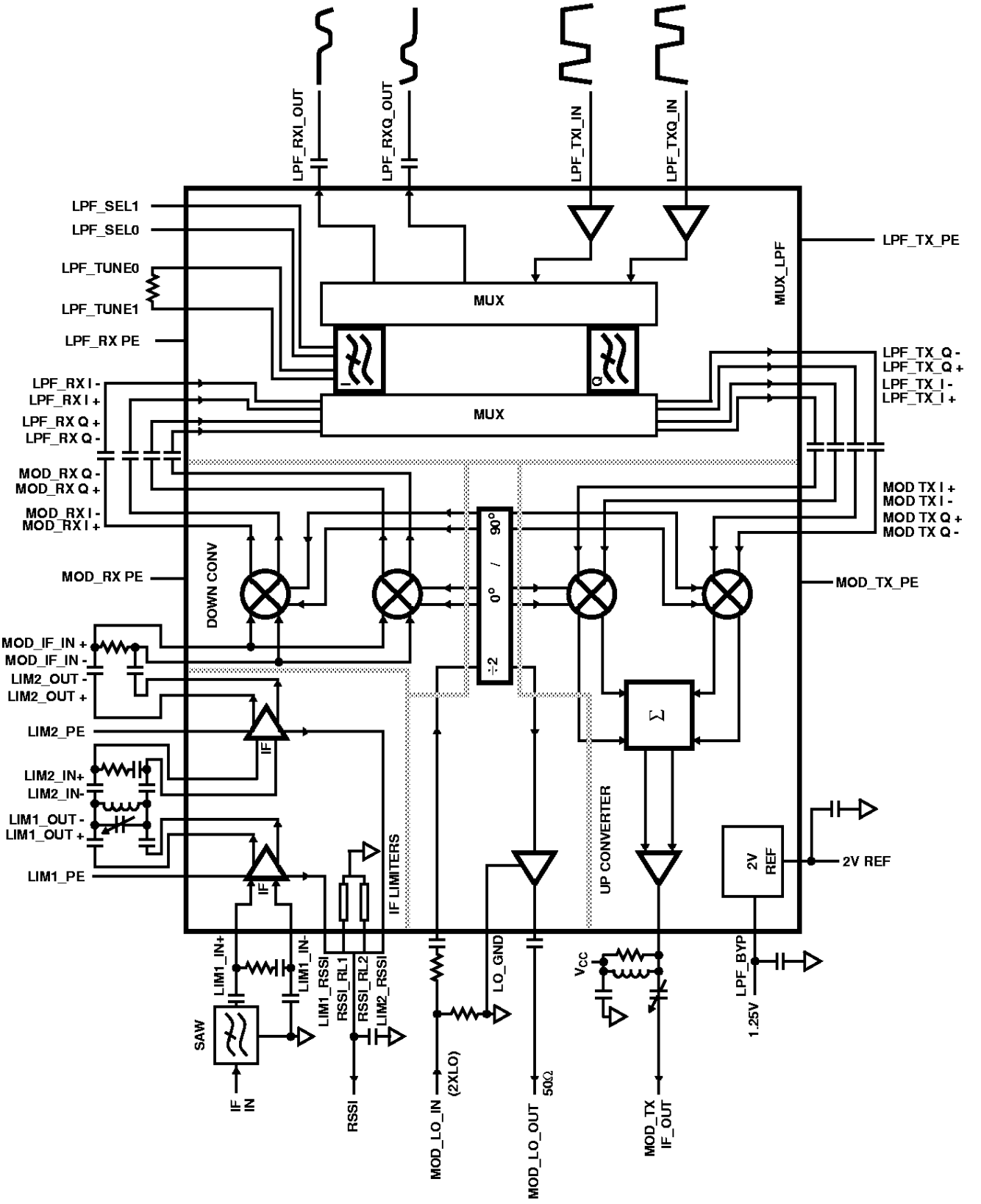
Pinout

80 LEAD TQFP
TOP VIEW

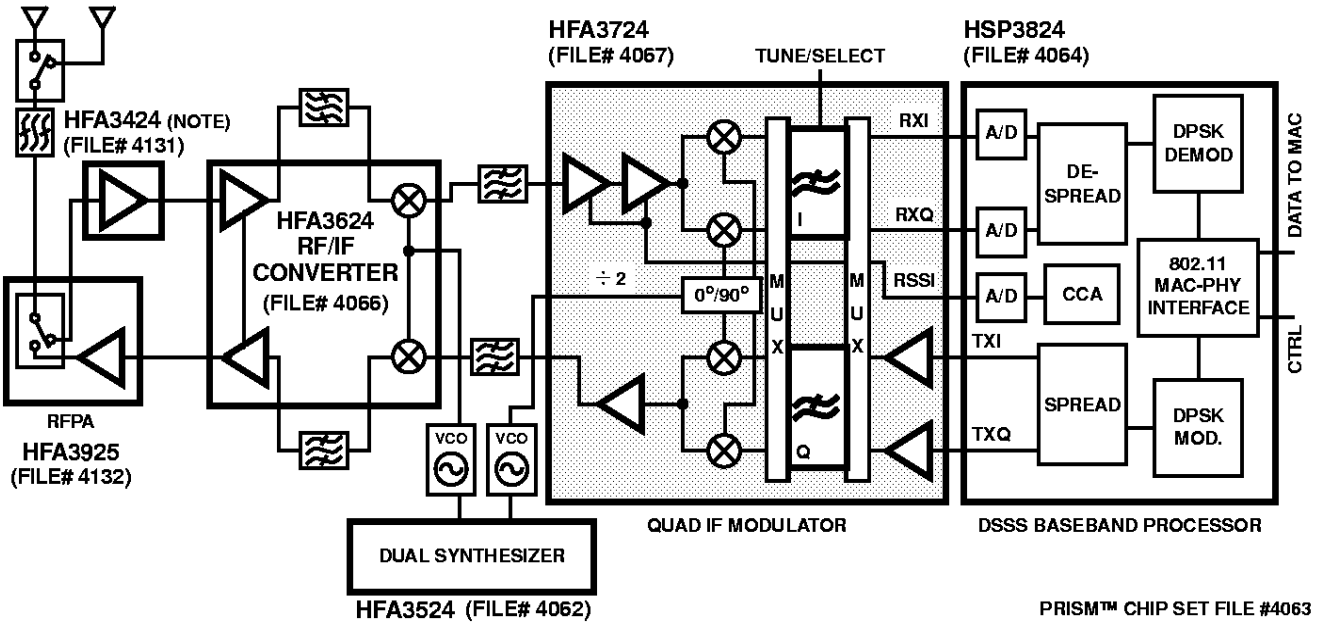


Block Diagram



NOTE: V_{CC}, GND and Bypass capacitors not shown.

Typical Application Diagram



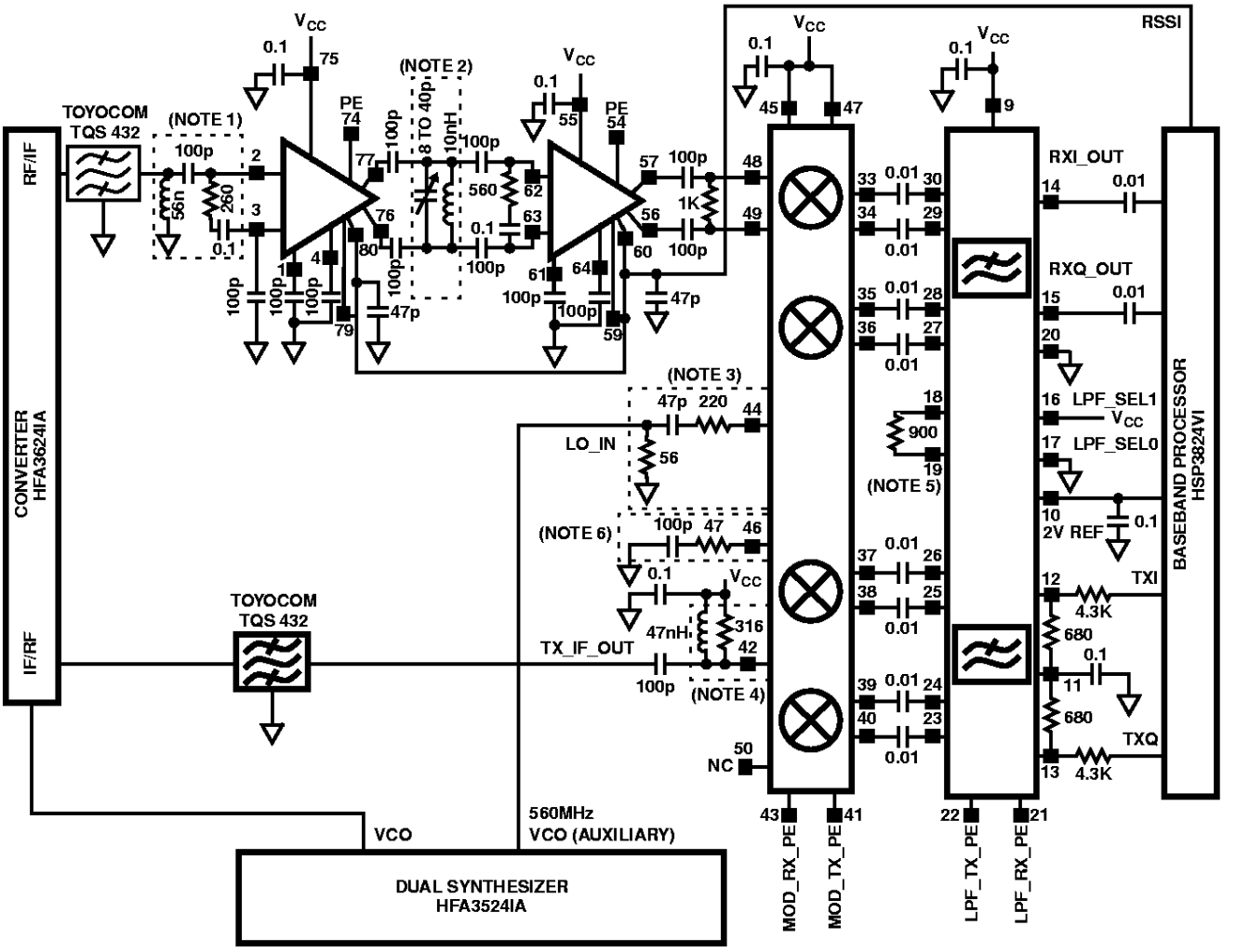
TYPICAL TRANSCEIVER APPLICATION USING THE HFA3724

NOTE: Required for systems targeting 802.11 specifications.

For additional information on the PRISM™ chip set, call (407) 724-7800 to access Harris' AnswerFAX system. When prompted, key in the four-digit document number (File #) of the datasheets you wish to receive.

The four-digit file numbers are shown in Typical Application Diagram, and correspond to the appropriate circuit.

Typical Application Diagram (Targeting IEEE 802.11 Standard)



TYPICAL APPLICATION DIAGRAM (TARGETING IEEE 802.11 STANDARD)

NOTES:

1. Input termination used to match a SAW filter.
2. Typical bandpass filter for 280MHz, BW = 47MHz, Q = 6. Can also be used if desired after the second stage.
3. Network shown for a typical -10dBm input at 50Ω.
4. Output termination used to match a SAW filter.
5. R_{TUNE} value for a 7.7MHz cutoff frequency setting.
6. LO buffer output termination is needed only when the buffer is enabled by pin 50 connected to GND, otherwise tie pin 46 to pin 47.

Pin Description

PIN	SYMBOL	DESCRIPTION
1	LIM1_BYP+	DC feedback pin for Limiter amplifier 1. Requires good decoupling and minimum wire length to a solid signal ground.
2	LIM1_In+	Non inverting analog input of Limiter amplifier 1.
3	LIM1_In-	Inverting input of Limiter amplifier 1.
4	LIM1_BYP-	DC feedback pin for Limiter amplifier 1. Requires good decoupling and minimum wire length to a solid signal ground.
5, 6, 7, 8	GND	Ground. Connect to a solid ground plane.
9	LPF_V_{CC}	Supply pin for the Low pass filter. Use high quality decoupling capacitors right at the pin.
10	2V REF	Stable 2V reference voltage output for external applications. Loading must be higher than 10kΩ. A bypass capacitor of at least 0.1µF is required.
11	LPF_BYP	Internal reference bypass pin. This is the common voltage (V_{CM}) used for the LPF digital thresholds. Requires 0.1µF decoupling capacitor.
12	LPF_TXI_In	Low pass filter in phase (I) channel transmit input. Conventional or attenuated direct coupling is required for digital inputs. (Note 7)
13	LPF_TXQ_In	Low pass filter quadrature (Q) channel transmit input. Conventional or attenuated direct coupling is required for digital inputs. (Note 7)
14	LPF_RXI_Out	Low pass filter in phase (I) channel receive output. Requires AC coupling. (Note 8)
15	LPF_RXQ_Out	Low pass filter quadrature (Q) channel receive output. Requires AC coupling. (Note 8)
16	LPF_Sel1	Digital control input pins. Selects four programed cut off frequencies for both receive and transmit channels. Tuning speed from one cutoff to another is less than 1µs. SEL1 SEL0 Cutoff Frequency — SEL1 SEL0 Cutoff Frequency LO LO 2.2MHz — HI LO 8.8MHz LO HI 4.4MHz — HI HI 17.6MHz
17	LPF_Sel0	
18	LPF_Tune1	These two pins are used to fine tune the Low pass filter cutoff frequency. A resistor connected between the two pins (R_{TUNE}) will fine tune both transmit and receive filters. Refer to the tuning equation in the LPF AC specifications.
19	LPF_Tune0	
20	GND	Ground. Connect to a solid ground plane.
21	LPF_RX_PE	Digital input control pin to enable the LPF receive mode of operation. Enable logic level is High.
22	LPF_TX_PE	Digital input control pin to enable the LPF transmit mode of operation. Enable logic level is High.
23	LPF_TXQ-	Negative output of the transmit Low pass filter, quadrature channel. AC coupling is required. Normally connects to the inverting input of the quadrature Modulator (Mod_TXQ-), pin 40.
24	LPF_TXQ+	Positive output of the transmit Low pass filter, quadrature channel. AC coupling is required. Normally connects to the non inverting input of the quadrature Modulator (Mod_TXQ+), pin 39.
25	LPF_TXI-	Negative output of the transmit Low pass filter, in phase channel. AC coupling is required. Normally connects to the inverting input of the in phase Modulator (Mod_TXI-), pin 38.
26	LPF_TXI+	Positive output of the transmit Low pass filter, in phase channel. AC coupling is required. Normally connects to the non inverting input of the in phase Modulator (Mod_TXI+), pin 37.
27	LPF_RXQ-	Low pass filter inverting input of the receive quadrature channel. AC coupling is required. This input is normally coupled to the negative output of the quadrature demodulator (Mod_RXQ-), pin 36.
28	LPF_RXQ+	Low pass filter non inverting input of the receive quadrature channel. AC coupling is required. This input is normally coupled to the positive output of the quadrature demodulator (Mod_RXQ+), pin 35.
29	LPF_RXI-	Low pass filter inverting input of the receive in phase channel. AC coupling is required. This input is normally coupled to the negative output of the in phase demodulator (Mod_RXI-), pin 34.

Pin Description (Continued)

PIN	SYMBOL	DESCRIPTION
30	LPF_RXI+	Low pass filter non inverting input of the receive in phase channel. AC coupling is required. This input is normally coupled to the positive output of the in phase demodulator (Mod_RXI-), pin 33.
31, 32	GND	Ground. Connect to a solid ground plane.
33	Mod_RXI+	In phase demodulator positive output. AC coupling is required. Normally connects to the non inverting input of the Low pass filter (LPF_RXI+), pin 30.
34	Mod_RXI-	In phase demodulator negative output. AC coupling is required. Normally connects to the inverting input of the Low pass filter (LPF_RXI-), pin 29.
35	Mod_RXQ+	Quadrature demodulator positive output. AC coupling is required. Normally connects to the non inverting input of the Low pass filter (LPF_RXQ+), pin 28.
36	Mod_RXQ-	Quadrature demodulator negative output. AC coupling is required. Normally connects to the inverting input of the Low pass filter (LPF_RXQ+), pin 27.
37	Mod_TXI+	In phase modulator non inverting input. AC coupling is required. This input is normally coupled to the Low pass filter positive output (LPF_TXI+), pin 26.
38	Mod_TXI-	In phase modulator inverting input. AC coupling is required. This input is normally coupled to the Low pass filter negative output (LPF_TXI-), pin 25.
39	Mod_TXQ+	Quadrature modulator non inverting input. AC coupling is required. This input is normally coupled to the Low pass filter positive output (LPF_TXQ+), pin 24.
40	Mod_TXQ-	Quadrature modulator inverting input. AC coupling is required. This input is normally coupled to the Low pass filter negative output (LPF_TXQ-), pin 23.
41	Mod_TX_PE	Digital input control to enable the Modulator section. Enable logic level is High for transmit.
42	Mod_TX_IF_Out	Modulator open collector output, single ended. Termination resistor to V_{CC} with a typical value of 316Ω.
43	Mod_RX_PE	Digital input control to enable the demodulator section. Enable logic level is High for receive.
44	Mod_LO_In (2XLO)	Single ended local oscillator current input. Frequency of input signal must be twice the required modulator carrier and demodulator LO frequency. Input current is optimum at 200μA_{RMS}. Input matching networks and filters can be designed for a wide range of power and impedances at this port. Typical input impedance is 130Ω.This pin requires AC coupling. (Note 9) NOTE: High second harmonic content input waveforms may degrade I/Q phase accuracy.
45	Mod_V_{CC}	Modulator/Demodulator supply pin. Use high quality decoupling capacitors right at the pin.
46	Mod_LO_Out	Divide by 2 buffered output reference from “Mod_LO_in” input. Used for external applications where the modulating and demodulating carrier reference frequency is required. 50Ω single end driving capability.This output can be disabled by use of pin 50. AC coupling is required, otherwise tie to pin 47 (V_{CC}).
47	Mod_V_{CC}	Modulator/Demodulator supply pin. Use high quality decoupling capacitors right at the pin.
48	Mod_IF_In+	Demodulator non inverting input. Requires AC coupling.
49	Mod_IF In-	Demodulator inverting input. Requires AC coupling.
50	LO_GND	When grounded, this pin enables the LO buffer (Mod_LO_Out). When open (NC) it disables the LO buffer.
51, 52, 53	GND	Ground. Connect to a solid ground plane.
54	LIM2_PE	Digital input control to enable the limiter amplifier 2. Enable logic level is High.
55	LIM2_V_{CC}	Limiter amplifier 2 supply pin. Use high quality decoupling capacitors right at the pin.
56	LIM2_Out-	Positive output of limiter amplifier 2. Requires AC coupling.
57	LIM2_Out+	Negative output of limiter amplifier 2. Requires AC coupling.
58	GND	Ground. Connect to a solid ground plane.

Pin Description (Continued)

PIN	SYMBOL	DESCRIPTION
59	RSSI_RL2	Load resistor to ground. Nominal value is 6kΩ. This load is used to terminate the LIM RSSI current output and maintain temperature and process variation to a minimum.
60	LIM2_RSSI	Current output of RSSI for the limiter amplifier 2. Connect in parallel with the RSSI output of the amplifier limiter 1 for cascaded response.
61	LIM2_BYP+	DC feedback pin for Limiter amplifier 2. Requires good decoupling and minimum wire length to a solid signal ground.
62	LIM2_In+	Non inverting analog input of Limiter amplifier 2.
63	LIM2_In-	Inverting input of Limiter amplifier 2.
64	LIM2_BYP-	DC feedback pin for Limiter amplifier 2. Requires good decoupling and minimum wire length to a solid signal ground.
65, 66, 67, 68, 69, 70, 71, 72, 73	GND	Ground. Connect to a solid ground plane.
74	LIM1_PE	Digital input control to enable the limiter amplifier 1. Enable logic level is High.
75	LIM1_V_{CC}	Limiter amplifier 1 supply pin. Use high quality decoupling capacitors right at the pin.
76	LIM1_Out-	Negative output of limiter amplifier 1. Requires AC coupling.
77	LIM1_Out+	Positive output of limiter amplifier 1. Requires AC coupling.
78	GND	Ground. Connect to a solid ground plane.
79	RSSI_RL1	Load resistor to ground. Nominal value is 6kΩ. This load is used to terminate the LIM RSSI current output and maintain temperature and process variation to a minimum.
80	LIM1_RSSI	Current output of RSSI for the limiter amplifier 1. Connect in parallel with the RSSI output of the amplifier limiter 2 for cascaded response.

NOTES:

7. The HFA3724 generates a lower sideband signal when the “I” input leads the “Q” input by 90 degrees.
8. For a reference LO frequency higher than a CW IF signal input, the “I” channel leads the “Q” channel by 90 degrees.
9. The in-phase reference LO transitions occur at the rising edges of the 2XLO clock signal. Quadrature LO transitions occur at the falling edges. 180 degrees phase ambiguity is expected for carrier locked systems without differential encoding.

TABLE 1. POWER MANAGEMENT

	TRANSMIT	RECEIVE	POWER DOWN
LIM1_PE	0	1	0
LIM2_PE	0	1	0
LPF_RX_PE	0	1	0
MOD_RX_PE	0	1	0
MOD_TX_PE	1	0	0
LPF_TX_PE	1	0	0

Absolute Maximum Ratings

Supply Voltage . . . . . -0.3V to +6.0V
Voltage on Any Other Pin . . . . . -0.3V to V_{CC} +0.3V

Operating Conditions

Supply Voltage Range . . . . . +2.7V to +5.5V
Temperature Range . . . . . $-40^oC \le T_A \le 85^oC$

Thermal Information

Thermal Resistance (Typical, Note 10) θ_{JA} ($^oC/W$)
TQFP Package 75
Package Power Dissipation at 70°C
TQFP Package 1.1W
Maximum Junction Temperature (Plastic Package . . . . . 150°C
Maximum Storage Temperature Range . . . . . $-65^oC \le T_A \le 150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(TQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

10. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 2.7V to 5.5V, Unless Otherwise Specified

PARAMETER	SYMBOL	(NOTE 11) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
Total Supply Current, RX Mode at 5.5V	RXI_{CC}	A	Full	-	70	105	mA
Total Supply Current, TX Mode at 5.5V	TXI_{CC}	A	Full	-	60	80	mA
Shutdown Current at 5.5V	I_{CCOFF}	A	Full	-	0.8	2.0	mA
All Digital Inputs V_{IH} (TTL Threshold for All V_{CC})	V_{IH}	A	Full	2.0		V_{CC}	V
All Digital Inputs V_{IL} (TTL Threshold for All V_{CC})	V_{IL}	A	Full	-0.2		0.8	V
High Level Input Current at 2.7V V_{CC}, V_{IN} = 2.4V	I_{IHl}	A	25	-	-	80	µA
High Level Input Current at 5.5V V_{CC}, V_{IN} = 4.0V	I_{IHh}	A	25	-	-	400	µA
Low Level Input Current, V_{IN} = 0.8V	I_{IL}	A	25	-20	-	+20	µA
RX to TX/TX to RX Switching Speed (Figure 23)	PEt	B	25	-	2	-	µs
Power Down/Up Switching Speed (Figure 23)	PEtpd	B	25	-	10	-	µs
Reference Voltage	V_{REF}	A	Full	1.87	2.0	2.13	V
Reference Voltage Variation Over Temperature	V_{REFT}	B	25	-	800	-	µV/°C
Reference Voltage Variation Over Supply Voltage	V_{REFV}	B	25	-	1.6	-	mV/V
Reference Voltage Minimum Load Resistance	V_{REFRL}	C	25	10	-	–	kΩ

NOTE:

11. A = Production Tested, B = Based on Characterization, C = By Design

AC Electrical Specifications, Demodulator Performance

Application Targeting IEEE 802.11, V_{CC} = 3V, Figure 23 Unless Otherwise Specified

PARAMETER	SYMBOL	(NOTE 12) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
IF Demodulator 3dB Limiting Sensitivity (Note 13)	D3db	B	25	-	-84	-	dBm
IF Demodulator I and Q Outputs Voltage Swing	DIQsw	A	Full	300	460	650	mV_{P-P}
IF Demodulator I and Q Channels Output Drive Capability (Z_{OUT} = 50Ω) C_{MAX} = 10pF	Doutz	C	25	1.2	2	-	kΩ
IF Demodulator I/Q Amplitude Balance, IFin = -70dbm at 50Ω	Dabal	A	Full	-1.0	0	+1.0	dB
IF Demodulator I/Q Phase Balance, IFin = -70dbm at 50Ω	Dphbal	A	Full	-4.0	0	+4.0	Degrees
IF Demodulator Output Variation at -70dbm to 0dbm input	Dovar	A	Full	-0.5	0	+0.5	dB
IF Demodulator RSSI Noise Induced Offset Voltage (Note 14)	Drssio	B	25	-	580	-	mV_{DC}
IF Demodulator RSSI Voltage Output Slope (Note 15)	Drssis	B	25	-	15	-	mV/dB

AC Electrical Specifications, Demodulator Performance

Application Targeting IEEE 802.11, V_{CC} = 3V, Figure 23 Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	(NOTE 12) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
IF Demodulator RSSI DC Level, Pin = -30dBm (Note 15)	Drssi_30	A	Full	0.90	1.46	1.71	V_{DC}
IF Demodulator RSSI DC Level, Pin = -70dBm (Note 15)	Drssi_70	A	Full	0.456	0.86	0.99	V_{DC}
IF Demodulator RSSI Linear Dynamic Range (Note 16)	Drssidr	B	25	-	60	-	dB
IF Demodulator RSSI Rise and Fall Time from -30dBm to -50dBm Input at 100pF Load	Drssitr	B	25	-	0.3	-	µs

NOTES:

12. A = Production Tested, B = Based on Characterization, C = By Design
13. 2XLO input = 572MHz, measure IF input level required to drop the I and Q output at 6MHz by 3dB from a reference output generated at IF input = -30dBm (hard limiting). LPF selected for 8.8MHz. This is a noise limited case with a BW of 47MHz. Please refer to the Overall Device Description, IF limiter.
14. The residual DC voltage generated by the RSSI circuit due to a noise limited stage at the end of the chain with no IF input. IF port terminated into 50Ω. Please referred to the Overall Device Description, IF limiter.
15. Both limiter RSSI current outputs are summed by on chip 6KΩ resistors in parallel.
16. Range is defined where the indicated received input strength by the RSSI is ±3dBm accurate.

AC Electrical Specifications, Modulator Performance

Application Targeting IEEE 802.11, V_{CC} = 3V, Figure 23 Unless Otherwise Specified

PARAMETER	SYMBOL	(NOTE 17) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
IF Modulator I/Q Amplitude Balance (Note 18)	Mabal	B	25	-1.0	0	+1.0	dB
IF Modulator I/Q Phase Balance (Note 18)	Mphbal	B	25	-4.0	0	+4.0	Degrees
IF modulator SSB Output Power (Note 19)	Mssbpw	A	Full	-12	-7	-4	dBm
IF Modulator Side Band Suppression (Note 19)	Mssbss	A	Full	26	33	-	dBc
IF Mod Carrier Suppression (LO Buffer Enabled) (Note 19)	Mssbcs	A	Full	28	30	-	dBc
IF Mod Carrier Suppression (LO Buffer Disabled) (Note 19)	Mssbcs1	B	25	28	36	-	dBc
IF Modulator Output Noise Floor (Out of Band)	Moutn0	B	25	-	-132	-	dBm/Hz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 2.2MHz (Note 20)	Msel1f	A	Full	1.8	2.2	2.5	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 4.4MHz (Note 20)	Msel2f	A	Full	3.6	4.4	5.0	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 8.8MHz (Note 20)	Msel3f	A	Full	7.3	8.8	9.8	MHz
IF Modulator I/Q 3dB Cutoff SEL0/1 = 17.6MHz (Note 20)	Msel4f	A	Full	14.6	17.6	19.6	MHz
IF Modulator Spread Spectrum Output Power (Note 21)	Mdsspw	B	25	-12	-7	-4	dBm
IF Modulator Side Lobe to Main Lobe Ratio, LPF = 8.8MHz (Note 21)	Mdsssl	A	Full	32	35	-	dB

NOTES:

17. A = Production Tested, B = Based on Characterization, C = By Design
18. Data is characterized by DC levels applied to MOD TXI and Q pins for 4 quadrants with LO output as reference or indirectly by the SSB characteristics.
19. Power at the fundamental SSB frequency of two 6MHz, 90 degrees apart square waves applied at TXI and TXQ inputs. V_{IH} = 3.0V, V_{IL} = 0.5V. LPF selected to 8.8MHz cutoff.
20. Cutoff frequencies are specified for both modulator and demodulator as the filter bank is shared and multiplexed for Transmit and Receive. Data is characterized by observing the attenuation of the fundamental of a square wave digital input swept at each channel separately. The IF output is down converted by an external wideband mixer with a coherent LO input for each of quadrature signals separately.
21. Typical ratio characterization with R_{TUNE} set to 7.7MHz, LPF selected for 8.8MHz. TXI and TXQ Digital Inputs at two independent and aligned 11M chip/s, 2^{23}-1 sequence code signals.