

## Features

- 64K x 18 Organization
  - 0.5 Micron CMOS Technology
  - Synchronous Pipeline Mode Of Operation
  - Single +3.3V  $\pm$  5 % Power Supply and Ground
  - Common I/O and LVTTL I/O Compatible
  - Registered Addresses, Write Enables, Chip Selects and Data Ins
  - Asynchronous Output Enable
  - Registered Outputs
  - Self-timed Write Operation
  - Byte Write Capability
  - 5V Tolerant I/O
  - Low Power Dissipation
    - 935 mW Active at 100 MHz
    - 90 mW Standby
  - 7 X 17 Ball Grid Array
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## Description

IBM Microelectronics 1M SRAM is a Synchronous Pipeline Mode, high performance CMOS STATIC RAM that is versatile, wide I/O, and achieves 10 nsec cycle times. A single clock is used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the Clock, all Addresses, Write-Enables, Chip Selects and Data Ins are registered internally and new signals can be applied to the chip prior to Data Out valid. Data from the previous cycle, is available in the following cycle. The chip is operated with a single +3.3 V power supply and is compatible with LVTTL I/O interfaces.

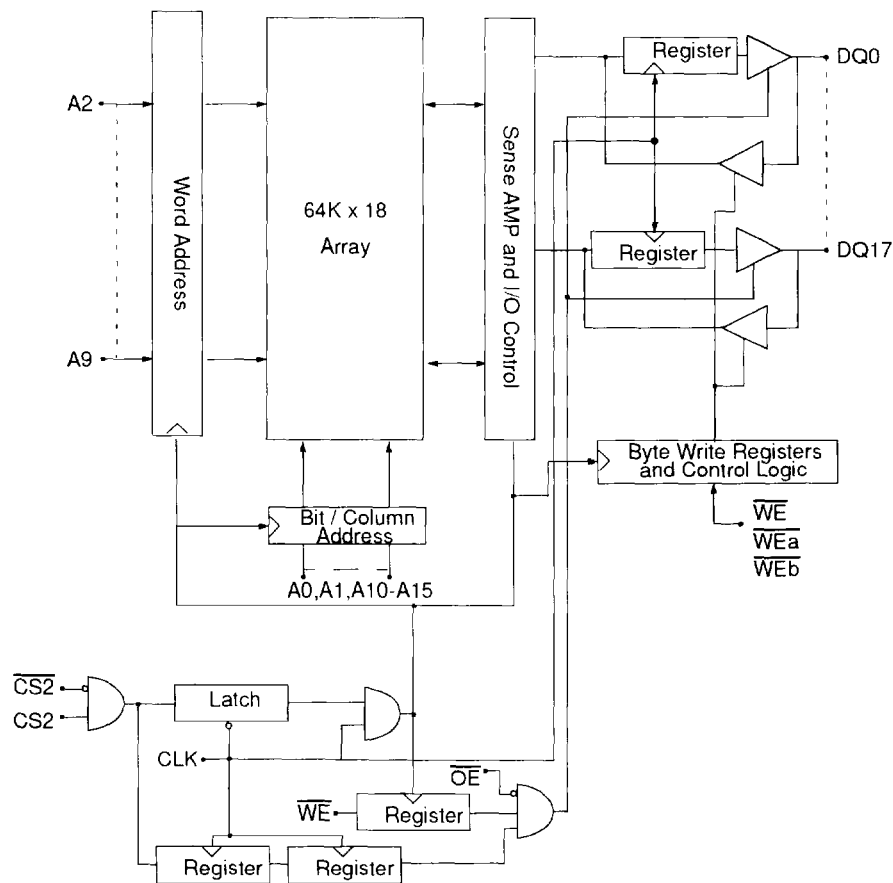
**X18 Ball Grid Array Layout** (Top View)

	A	B	C	D	E	F	G
1	VDDQ	SA	SA	NC	SA	SA	VDDQ
2	NC	CS2	NC	NC	NC	$\overline{CS2}$	NC
3	NC	SA	SA	VDD	SA	SA	NC
4	DQb	NC	VSS	NC	VSS	DQa	NC
5	NC	DQb	VSS	NC	VSS	NC	DQa
6	VDDQ	NC	VSS	$\overline{OE}$	VSS	DQa	VDDQ
7	NC	DQb	$\overline{WEb}$	NC	VSS	NC	DQa
8	DQb	NC	VSS	NC	VSS	DQa	NC
9	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
10	NC	DQb	VSS	CLK	VSS	NC	DQa
11	DQb	NC	VSS	NC	$\overline{WEa}$	DQa	NC
12	VDDQ	DQb	VSS	$\overline{WE}$	VSS	NC	VDDQ
13	DQb	NC	VSS	SA	VSS	DQa	NC
14	NC	DQb	VSS	SA	VSS	NC	DQa
15	NC	SA	NC	VDD	VSS	SA	NC
16	NC	SA	SA	NC	SA	SA	NC
17	VDDQ	NC	NC	NC	NC	NC	VDDQ

### Pin Description

A0-A15	Address input (SA)	$\overline{OE}$	Output Enable
DQ0-DQ17	Data Input/Output (0-8,9-17)	$\overline{CS2}$ , CS2	Chip selects
$\overline{CLK}$	Clock	$V_{DD}$	Power Supply (+3.3V)
$\overline{WE}$	Write Enable, global	$V_{SS}$	Ground
$\overline{WEa}$	Write Enable, Byte a (0 to 8)	$V_{DDQ}$	Output Power Supply (+3.3V)
$\overline{WEb}$	Write Enable, Byte b (9 to 17)	NC	No Connect

### Block Diagram



### Ordering Information

Part Number	Organization	Speed	Leads	Notes
IBM041811PLA-10	64K x 18	5 ns Access / 10 ns Cycle	7 X 17 BGA	

### Clock Truth Table

CLK	$\overline{CS2}$	CS2	$\overline{WE}$	$\overline{OE}$	Function	DQ	Current	Notes
L→H	H	X	X	X	Deselected	HIZ	$I_{SB}$	1
L→H	X	L	X	X	Deselected	HIZ	$I_{SB}$	1
L→H	L	H	H	L	Read	$Q_{OUT}$	$I_{DD}$	2
L→H	L	H	H	H	Read	HIZ	$I_{DD}$	2
L→H	L	H	L	X	Write	$D_{IN}$	$I_{DD}$	2

1.  $I_{SB}$  = Stand-by Current  
 2.  $I_{DD}$  = Selected Current

### Write Enable Truth Table

$\overline{WE}$	$\overline{WEa}$	$\overline{WEb}$	Byte Written	Notes
L	H	H	Abort Write	
L	L	L	Write All Bytes	
L	L	H	Write Byte A ( $D_{IN} 0 - 8$ )	
L	H	L	Write Byte B ( $D_{IN} 9 - 17$ )	
H	X	X	Read	

### Absolute Maximum Ratings

Item	Symbol	Rating	Units	Notes
Power Supply Voltage	$V_{DD}$	-0.5 to 4.6	V	1
Input Voltage	$V_{IN}$	-0.5 to 6.0	V	1
Output Voltage	$V_{OUT}$	-0.5 to $V_{DD}+0.5$	V	1
Operating Temperature	$T_{OPR}$	0 to +70	°C	1
Storage Temperature	$T_{STG}$	-55 to +125	°C	1
Power Dissipation	$P_D$	2	W	1
Short Circuit Output Current	$I_{OUT}$	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended DC Operating Conditions ( $T_A=0$ to $70^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	$V_{DD}$	3.135	3.3	3.465	V	2,5
Input High Voltage	$V_{IH}$	2.2	—	5.5	V	2,3,5
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V	2,4,5
Output Current	$I_{OUT}$	—	5	8	mA	5

2. All voltages referenced to  $V_{SS}$ . All  $V_{DD(Q)}$  and  $V_{SS}$  pins must be connected.
3.  $V_{IH}(\text{Max})\text{DC} = 5.5\text{ V}$ ,  $V_{IH}(\text{Max})\text{AC} = 6.0\text{ V}$  (pulse width  $\leq 4.0\text{ns}$ )
4.  $V_{IL}(\text{Min})\text{DC} = -0.3\text{ V}$ ,  $V_{IL}(\text{Min})\text{AC} = -1.5\text{ V}$  (pulse width  $\leq 4.0\text{ns}$ )
5. Input voltage levels are tested to the following DC conditions: 1 microsecond cycle and 200 ns set-up and hold times.

### Capacitance ( $T_A=0$ to $+70^\circ\text{C}$ , $V_{DD}=3.3\text{V} \pm 5\%$ , $f=1\text{MHz}$ )

Parameter	Symbol	Test Condition	Max	Units	Notes
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{V}$	5	pF	
Data I/O Capacitance (DQ0-DQ17)	$C_{OUT}$	$V_{OUT} = 0\text{V}$	5	pF	

### DC Electrical Characteristics ( $T_A=0$ to $+70^\circ\text{C}$ , $V_{DD}=3.3\text{V} \pm 5\%$ )

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Current Average Power Supply Operating Current ( $\overline{OE} = V_{IH}$ , $I_{OUT} = 0$ )	$I_{DD10}$	—	270	mA	2,3
Standby Current Power Supply Standby Current ( $\overline{CS2} = V_{IH}$ , $\overline{CS2} = V_{IL}$ All other inputs = $V_{IH}$ or $V_{IL}$ , $I_{OUT} = 0$ , Clock at 100 MHz)	$I_{SB}$	—	25	mA	1,3
Input Leakage Current Input Leakage Current, any input ( $V_{IN} = 0$ & $V_{DD}$ )	$I_{LI}$	—	+1	$\mu\text{A}$	
Output Leakage Current ( $V_{OUT} = 0$ & $V_{DD}$ , $\overline{OE} = V_{IH}$ )	$I_{LO}$	—	+1	$\mu\text{A}$	
Output High Level Output "H" Level Voltage ( $I_{OH} = -8\text{mA}$ @ 2.4V)	$V_{OH}$	2.4	—	V	
Output Low Level Output "L" Level Voltage ( $I_{OL} = +8\text{mA}$ @ 0.4V)	$V_{OL}$	—	0.4	V	

1.  $I_{SB}$  = Stand-by Current
2.  $I_{DD}$  = Selected Current
3.  $I_{OUT}$  = Chip Output Current

**AC Test Conditions** ( $T_A=0$  to  $+70^\circ\text{C}$ ,  $V_{DD}=3.3\text{V} \pm 5\%$ )

Parameter	Symbol	Conditions	Units	Notes
Input Pulse High Level	$V_{IH}$	3.0	V	
Input Pulse Low Level	$V_{IL}$	0.0	V	
Input Rise Time	$T_R$	2.0	ns	
Input Fall Time	$T_F$	2.0	ns	
Input and Output Timing Reference Level		1.5	V	
Output Load Conditions				1

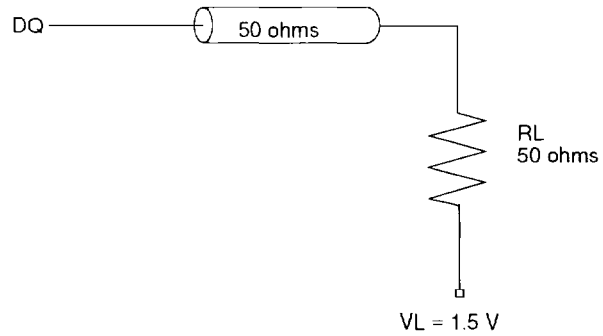
1. See AC Test Loading figure on page 57.

**AC Characteristics** ( $T_A=0$  to  $+70^\circ\text{C}$ ,  $V_{DD}=3.3\text{V} \pm 5\%$ )

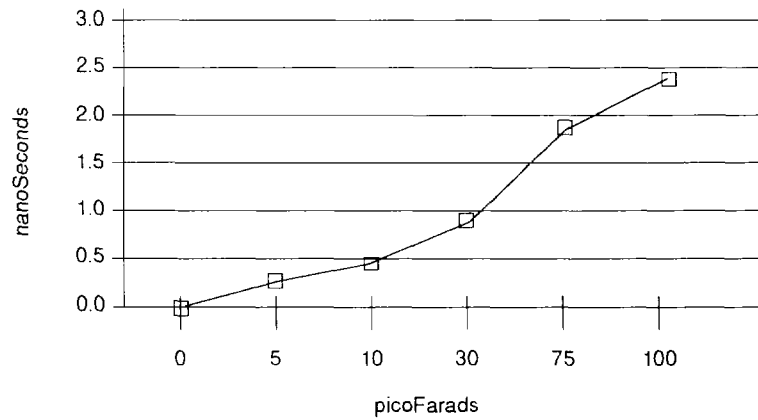
Parameter	Symbol	-10		Units	Notes
		Min.	Max.		
Cycle Time	$t_{CYCLE}$	10.0	—	ns	
Clock Pulse High	$t_{CH}$	2.0	—	ns	
Clock Pulse Low	$t_{CL}$	2.0	—	ns	
Clock to Output Valid	$t_{CO}$	—	5.0	ns	1
Address Setup Time	$t_{AS}$	1.0	—	ns	
Address Hold Time	$t_{AH}$	1.5	—	ns	
Chip Selects Setup Time	$t_{CSS}$	2.0	—	ns	
Chip Selects Hold Time	$t_{CSH}$	0.5	—	ns	
Write Enables Setup Time	$t_{WES}$	1.0	—	ns	
Write Enables Hold Time	$t_{WEH}$	1.5	—	ns	
Data In Setup Time	$t_{DS}$	1.0	—	ns	
Data In Hold Time	$t_{DH}$	1.5	—	ns	
Data Out Hold Time	$t_{DOX}$	1.0	—	ns	1
Clock High to Output High Z	$t_{CHZ}$	—	4.0	ns	1,2
Clock High to Output Active	$t_{CLZ}$	1.0	—	ns	1,2
Output Enable to High Z	$t_{OHZ}$	2.0	5.0	ns	1,2
Output Enable to Low Z	$t_{OLZ}$	0.25	—	ns	1,2
Output Enable to Output Valid	$t_{OO}$	—	5.0	ns	1

1. See AC Test Loading figure on page 57.  
2. Transitions are measured  $\pm 200$  mV from steady state voltage.

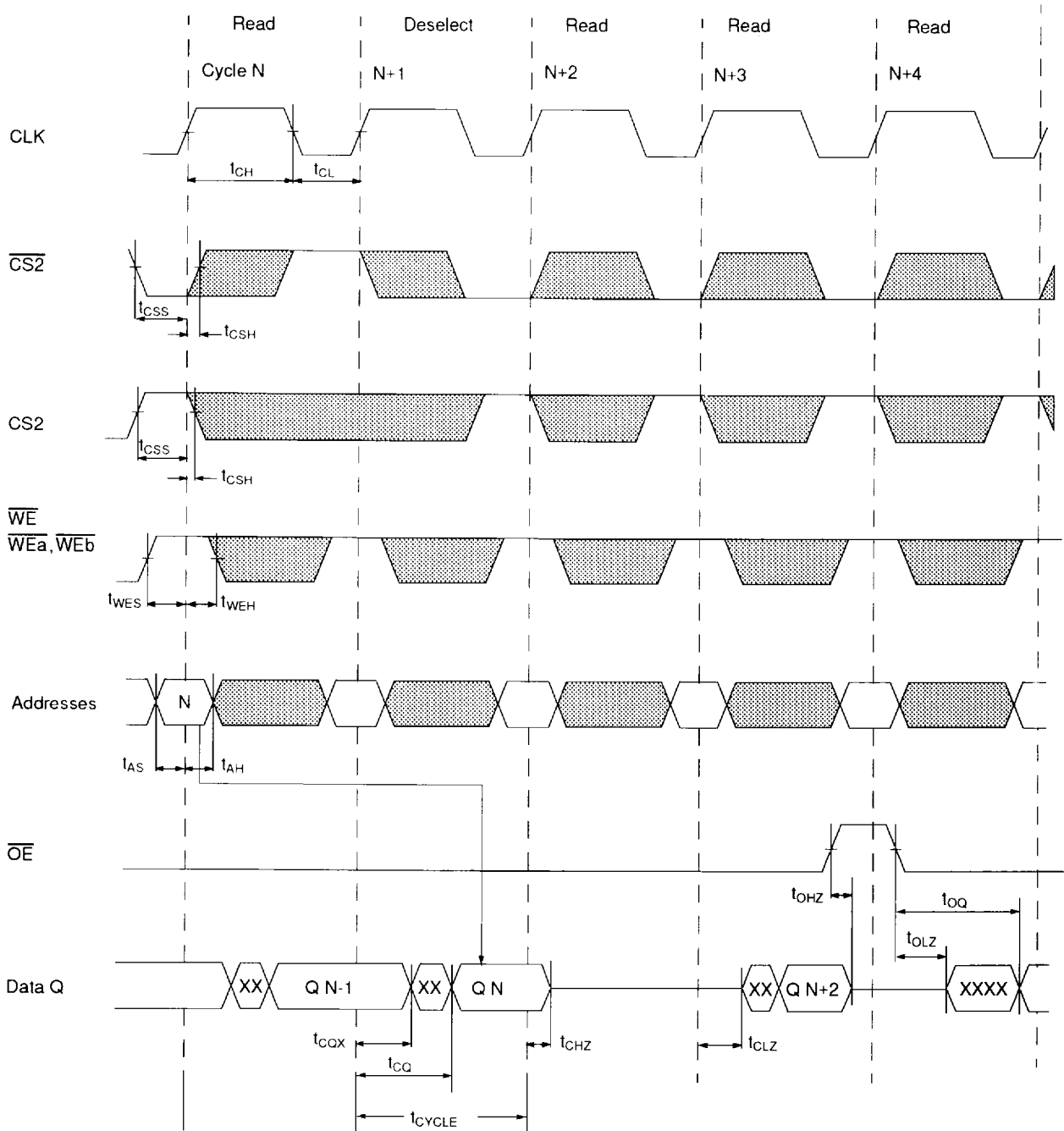
### AC Test Loading



**Capacitive Load Derating Curve**

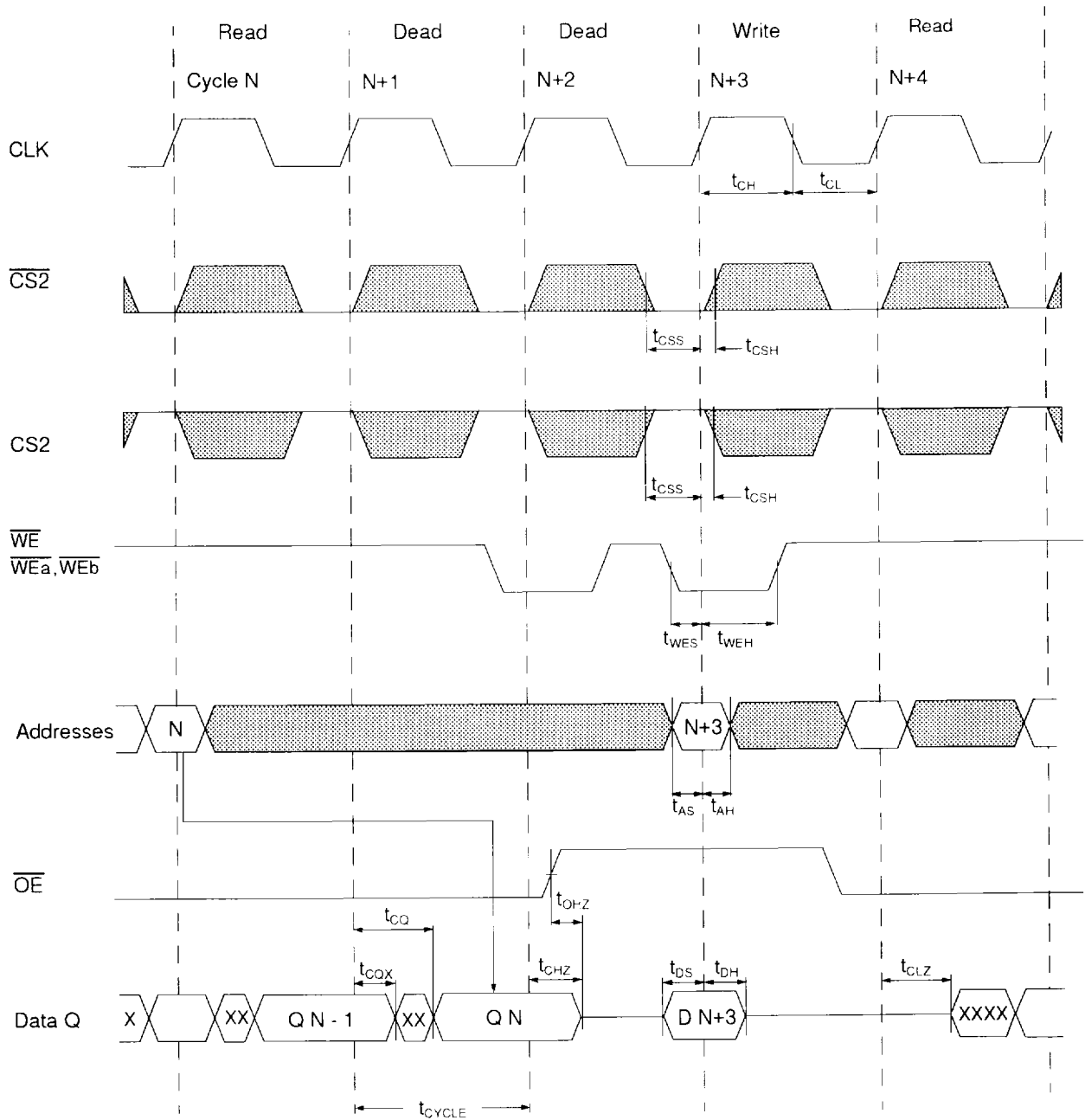


### Timing Diagram (Read)

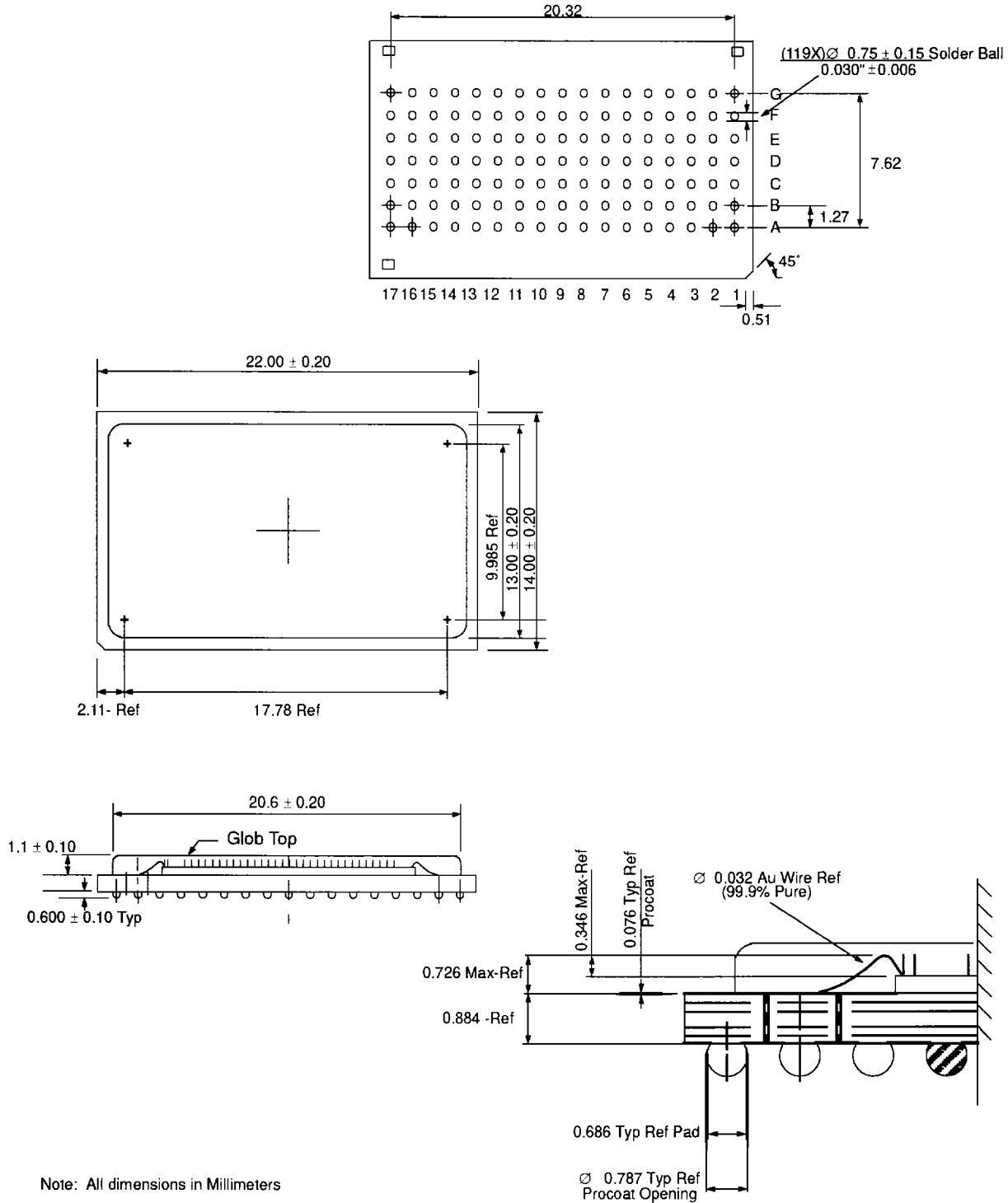




**Timing Diagram (Read Followed by Write)**



**7 x 17 Ball Grid Array Package Diagram**



Note: All dimensions in Millimeters