NEC

MOS Integrated Circuit

V850ES/KJ2

32-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The V850ES/KJ2 is a 32-bit single chip microcontroller of the V850ES series. 32-bit CPU, ROM, RAM, timer/counters, serial interface, A/D converter, D/A converter and so on are integrated on a single chip.

FEATURES

- V850ES core, 32-bit RISC architecture
- Instruction execution time: 50ns(min.) @20MHz , Integrated PLL(x4) circuit
- On-chip ROM , RAM

Type / Part Number	Program Memory (Flash Memory Size)	Data Memory (RAM Size)
μPD70F3733	**128KB**	**6KB**
μPD70F3734	**256KB**	**16KB**

- Timer:
  - 16-bit timer (Type TMP) : 1 channel
  - 16-bit timer (Type TM0) : 6 channels
  - 8-bit timer (Type TM5) : 2 channels
  - 8-bit timer (Type TMH) : 2 channels
  - 8-bit timer (Type BRG) : 1 channel
  - Watch timer : 1 channel
  - Watchdog timer : 2 channels
- Serial interface :
  - CSI : 2 channels
  - Auto CSI : 2 channels
  - UART : 2 channels
  - I^2C : 1 channel
  - UART [note]/CSI : 1 channel
  - UART [note]/ I^2C : 1 channel
- A/D converter : 10-bit resolution : 16 channels
- D/A converter : 8-bit resolution : 2 channels
- DMA controller : 4 channels
- Operation Voltage :
  - 4.5V to 5.5V: 20MHz max. (OSC=5MHz x4)
  - 4.0V to 5.5V: 16MHz max. (OSC=4MHz x4)
  - 2.7V to 5.5V: 10MHz max. (OSC=10MHz)
- Package :
  - 144-pin LQFP (20 x 20mm, 0.5mm pitch)

Note: This UART is identical.

Please note: The information in this document is subject to change without notice

Function Table

Device name		V850ES/KE2	V850ES/KF2	V850ES/KG2	V850ES/KJ2	
					μPD 70F3733	μPD 70F3734
CPU core		V850ES				
CPU performance		29MIPS(@20MHz)				
Internal flash memory		128KB	128/256KB	128KB/256KB	128KB	256KB
Internal RAM		4KB	6/12KB	6KB/16KB	6KB	16KB
External bus interface	Bus type	-	Multiplexed	Multiplexed/ separate	Multiplexed/ separate	
	Address bus	-	16 bits	22 bits	24 bits	
	Data bus	-	8/16 bits	8/16 bits	8/16 bits	
	Chip select signal	-	2	2	4	
Interrupt sources	Internal	9	9	9	9	
	External	26	29	41	47	
Timer/counter		TMP x 1 ch TM0 x 1 ch TM5 x 2 ch TMH x 2 ch BGR x 1 ch Watch x 1 ch WDT x 2 ch	TMP x 1 ch TM0 x 2 ch TM5 x 2 ch TMH x 2 ch BRG x 1 ch Watch x 1 ch WDT x 2 ch	TMP x 1 ch TM0 x 4 ch TM5 x 2 ch TMH x 2 ch BRG x 1 ch Watch x 1 ch WDT x 2 ch	16-bit timer(TMP) x 1 ch 16-bit timer(TM0) x 6 ch 8-bit timer(TM5) x 2 ch 8-bit timer(TMH) x 2 ch 8-bit interval timer(BRG) x 1 ch Watch timer x 1 ch Watchdog timer x 2 ch	
Serial interface		CSI x 2 ch UART x 2 ch I^2C x 1 ch	CSI x 2 ch UART x 2 ch I^2C x 1 ch Auto CSI x 1 ch	CSI x 1 ch UART x 2 ch I^2C x 1 ch Auto CSI x 2 ch UART/CSI x 1 ch	CSI x 2 ch UART x 2 ch I^2C x 1 ch Auto CSI x 2 ch UART note/ CSI x 1 ch UART note / I^2C x 1 ch	
A/D converter		10-bit x 8 ch	10-bit x 8 ch	10-bit x 8 ch	10-bit x 16 ch	
D/A converter		-	-	8-bit x 2 ch	8-bit x 2 ch	
DMA controller		-	-	4 ch	4 ch	
Ports	I/O	43	59	76	112	
	Input	8	8	8	16	
Debug control unit		Provided (RUN/break)	Provided (RUN/break)	Provided (RUN/break)	Provided (RUN/break)	
Other peripheral functions		Real-time output 6-bit x 1 ch (V850ES/KJ2: 2 ch) Key return input x 8 ch				
Operating frequency		When using main clock : 2 to 20MHz When using subclock : 32.768kHz				
Power supply voltage		4.5 to 5.5V(@20MHz) 4.0 to 5.5V(@16MHz) 2.7 to 5.5V(@10MHz)				
Package		64-pin LQFP (10x10mm)	80-pin QFP (14x14mm)	100-pin LQFP (14x14mm) 100-pin QFP (14x20mm)	144-pin LQFP (20 x 20 mm)	
Operating ambient temperature		-40°C to +85°C				

Note: This UART is identical. In the V850ES/KJ2, three channels of UART are provided.

Timer & Serial interface functions overview

Function	Overview
CSI	➢ Maximum transfer speed: 5Mbps (fxx=20MHz, using internal clock) ➢ Master mode/slave mode selectable ➢ Transmission data length: 8 bits or 16bits can be set ➢ MSB/LSB-first selectable for transfer data ➢ Eight clock signals can be selected (7 master clocks and 1 slave clock) ➢ 3-wire type SO0n: Serial transmit data output SI0n: Serial receive data input SCK0n: Serial clock I/O ➢ Interrupt sources: 1 type Transmission/reception completion interrupt request signal (INTCSI0n) ➢ Transmission/reception mode or reception-only mode selectable ➢ Two transmission buffer registers (SOTBFn/SOTBFLn, SOTBn/SOTBLn) and two reception buffer registers (SIRBn/SIRBLn, SIRBEn/SIRBELn) are provided on chip ➢ Single transfer mode/continuous transfer mode selectable **Remark** n = 0 to 2
Automatic transmit/ receive CSI	➢ Maximum transfer speed: 2MHz (fxx=20MHz, in master mode) ➢ Master mode/slave mode selectable ➢ Transfer data length: 8 bits ➢ MSB/LSB-first selectable for transfer data ➢ Automatic transmit/receive function: ✓Number of transfer bytes can be specified between 1 and 32 ✓Transfer interval can be specified (0 to 63 clocks) ✓Single transfer/repeat transfer selectable ➢ On-chip dedicated baud rate generator (6/8/16/32 divisions) ➢ 3-wire type SOAn: Serial transmit data output SIAn: Serial receive data input SCKAn: Serial clock I/O ➢ Transmission/reception completion interrupt request signal: INTCSIAn ➢ Internal 32-byte buffer RAM **Remark** n = 0, 1
I^2C	➢ Operation stop mode This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption. ➢ I^2C bus mode (multi-master supported) This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLn) line and a serial data bus (SDAn) line. This mode complies with the I^2C bus format and the master device can output “start condition”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received data by hardware. This function can simplify the part of application program that controls the I^2C bus. **Remark** n = 0, 1

Timer & Serial interface functions overview

Function	Overview
UART	➢ Maximum transfer speed: 312.5kbps (fxx=20MHz, using internal clock) ➢ Full-duplex communications: On-chip RXBn register On-chip TXBn register ➢ Two-pin configuration: TXDn: Transmit data output pin RXDn: Receive data input pin ➢ Reception error detection functions Parity error / Framing error / Overrun error ➢ Interrupt sources: 3 type ✓ Reception error interrupt request signal (INTSREn): Interrupt is generated according to the logical OR of the three types of reception errors ✓ Reception completion interrupt request signal (INTSRn): Interrupt is generated when receive data is transferred from the receive shift register to the RXBn register after serial transfer is completed during a reception enabled state ✓ Transmission completion interrupt request signal (INTSTn): Interrupt is generated when the serial transmission of transmit data (8 or 7 bits) from the transmit shift register is completed ➢ Character length: 7 or 8 bits ➢ Parity functions: Odd, even, 0, or none ➢ Transmission stop bits: 1 or 2 bits ➢ On-chip dedicated baud rate generator **Note** The ASCK0 pin (external clock input) is available only for UART0. **Remark** n = 0 to 2
16-bit timer/event counter (TMP)	➢ Clock selection: 8 ways ➢ Capture trigger input pins: 2 ➢ External event count input pins: 1 ➢ External trigger input pins: 1 ➢ Timer/counters: 1 ➢ Capture/compare registers: 2 ➢ Capture/compare match interrupt request signals: 2 ➢ Timer output pins: 2 ➢ TMP0 has the following functions. ✓ Interval timer ✓ External event counter ✓ External trigger pulse output ✓ One-shot pulse output ✓ PWM output ✓ Free-running timer ✓ Pulse width measurement

Timer & Serial interface functions overview

Function	Overview
16-bit timer/event counter (TM0)	➢ Interval timer ➢ PPG output ➢ Pulse width measurement ➢ External event counter ➢ Square-wave output ➢ One-shot pulse output
8-bit timer/event counter (TM5)	➢ Mode using 8-bit timer/event counter alone (individual mode) ✓ Interval timer ✓ External event counter ✓ Square-wave output ✓ PWM output ➢ Mode using cascade connection (16-bit resolution: cascade connection mode) ✓ Interval timer with 16-bit resolution ✓ External event counter with 16-bit resolution ✓ Square-wave output with 16-bit resolution
8-bit timer (TMH)	➢ Interval timer ➢ PWM output ➢ Square wave output ➢ Carrier generator mode
Interval timer, Watch timer	➢ Interval timer BRG: An interrupt request signal (INTBRG) is generated at a specified interval. ➢ Generation of count clock for watch timer: When the main clock is used as the count clock for the watch timer, a count clock (f_{BRG}) is generated.
Watchdog timer 1	➢ Watchdog timer 1 has the following operation modes. ✓ Watchdog timer ✓ Interval timer ➢ The following functions are realized from the above-listed operation modes. ✓ Generation of non-maskable interrupt request signal (INTWDT1) upon overflow of watchdog timer 1 ✓ Generation of system reset signal (WDTRES1) upon overflow of watchdog timer 1 ✓ Generation of maskable interrupt request signal (INTWDTM1) upon overflow of interval timer
Watchdog timer 2	➢ Default start watchdog timer ✓ Reset mode: Reset operation upon overflow of watchdog timer 2 (generation of WDTRES2 signal) ✓ Non-maskable interrupt request mode: NMI operation upon overflow of watchdog timer 2 (generation of INTWDT2 signal) ➢ Input selectable from internal oscillation clock and sub-clock as the source clock

Other functions overview

Function	Overview
A/D converter	➢ Operating voltage (AV_{REF0}): 2.7 to 5.5 V ➢ Successive approximation method 10-bit A/D converter ➢ Analog input pin: 16 ➢ Trigger mode: ✓ Software trigger mode ✓ Timer trigger mode (INTTM010) ✓ External trigger mode (ADTRG pin) ➢ Operation mode ✓ Select mode ✓ Scan mode ➢ Power fail detection function
D/A converter	➢ 8-bit resolution x 2 channels ➢ R-2R ladder string method ➢ Conversion time: 20μs (MAX.) (AV_{REF1} = 2.7 to 5.5 V) ➢ Analog output voltage: AV_{REF1} x m/256 (m = 0 to 255; value set to DACSn register) ➢ Operation modes: Normal mode, real-time output mode **Remark** n = 0, 1
DMA	➢ 4 independent DMA channels ➢ Transfer unit: 8/16 bits ➢ Maximum transfer count: 65,536 (2^{16}) ➢ Transfer type: Two-cycle transfer ➢ Transfer mode: Single transfer mode ➢ Transfer requests ✓ Request by interrupts from on-chip peripheral I/O (serial interface, timer/counter, A/D converter) or interrupts from external input pin ✓ Requests by software trigger ➢ Transfer targets ✓ Internal RAM ↔ Peripheral I/O ✓ Peripheral I/O ↔ Peripheral I/O ✓ Internal RAM ↔ External memory ✓ External memory ↔ Peripheral I/O ✓ External memory ↔ External memory
Interrupt/exception processing	➢ Interrupts ✓ Non-maskable interrupts: 3 sources ✓ Maskable interrupts: External: 8, Internal: 45 sources ✓ 8 levels of programmable priorities (maskable interrupts) ✓ Multiple interrupt control according to priority ✓ Masks can be specified for each maskable interrupt request. ➢ Exceptions ✓ Software exceptions: 32 sources ➢ Exception trap: 2 sources (illegal op code exception and debug trap)
Key interrupt	➢ A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins (KR0 to KR7) by setting the KRM register.

Other functions overview

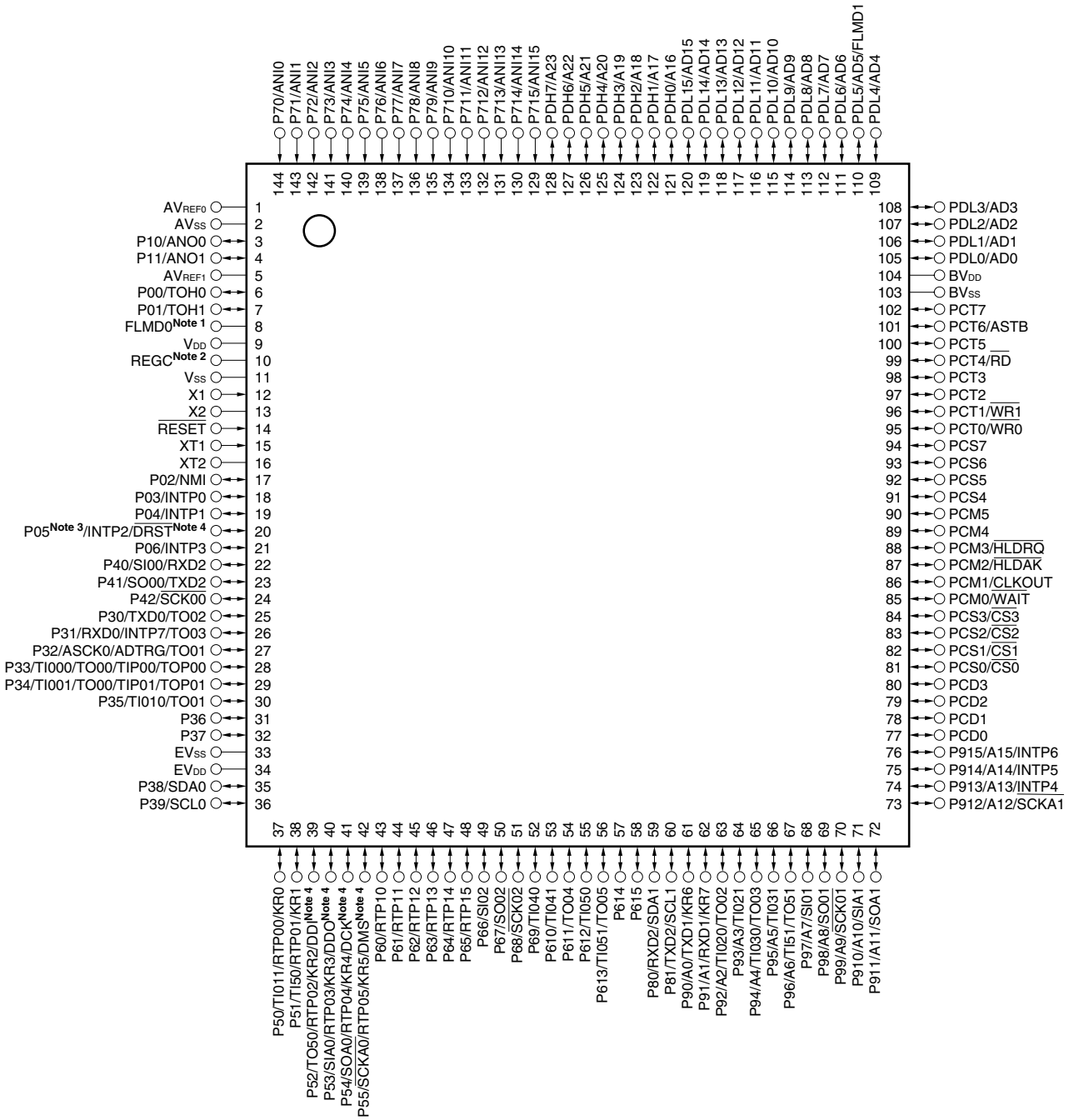
Function	Overview
Standby modes	➢ The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. ✓ HALT mode: Mode to stop only the operating clock of the CPU ✓ IDLE mode: Mode to stop all the operations of the internal circuits except the oscillator ✓ STOP mode: Mode to stop all the operations of the internal circuits except the sub-clock oscillator ✓ Subclock operation mode: Mode to use the subclock as the internal system clock ✓ Sub-IDLE mode: Mode to stop all the operations of the internal circuits, except the oscillator, in the subclock operation mode
Bus control	➢ Output is selectable from a multiplex bus with a minimum of 3 bus cycles and a separate bus with a minimum of 2 bus cycles ➢ Chip select function for up to 2 spaces ➢ 8-bit/16-bit data bus selectable (for each area selected by chip select function) ➢ Wait function ✓ Programmable wait function of up to 7 states (selectable for each area selected by chip select function) ✓ External wait function using $\overline{\text{WAIT}}$ pin ➢ Idle state function ➢ Bus hold function ➢ The bus can be controlled using a different voltage from the operating voltage by setting $BV_{DD} \leq V_{DD} = EV_{DD}$ (however, only in multiplex bus mode).

Pin configuration (TOP VIEW)

144-pin plastic LQFP (20 x 20 mm, 0.5mm pitch)

μPD70F3733GJ-UEN-A

μPD70F3734GJ-UEN-A



Notes 1. FLMD0 pin: Connect to V_{SS} in normal operation mode.

2. When using a regulator, connect the REGC pin to V_{SS} via a 10 μF capacitor.
When not using a regulator, connect the REGC pin directly to V_{DD}.

3. Care must be exercised in processing the P05 pin when reset is released.

4. The $\overline{DRST}$, DDI, DDO, DCK and DMS pins can be used only in the μPD70F3734.

Caution Make EV_{DD} the same potential as V_{DD}.
BV_{DD} can be used when $V_{DD} = EV_{DD} \geq BV_{DD}$.

List of Pin Functions

(1) Port pins (1/4)

Pin Name	Pin No.	I/O	Pull-up Resistor	Function	Alternate Function
P00	6	I/O	Yes	Port 0 I/O port Input/output can be specified in 1-bit units.	TOH0
P01	7				TOH1
P02	17				NMI
P03	18				INTP0
P04	19				INTP1
P05 Note 1	20				INTP2/$\overline{\text{DRST}}$ Note 3
P06	21				INTP3
P10	3	I/O	Yes	Port 1 I/O port Input/output can be specified in 1-bit units.	ANO0
P11	4				ANO1
P30	25	I/O	Yes	Port 3 I/O port Input/output can be specified in 1-bit units. P36 to P39 are fixed to N-ch open-drain output.	TXD0/TO02
P31	26				RXD0/INTP7/TO03
P32	27				ASCK0/ADTRG/TO01
P33	28				TI000/TO00/TIP00/TOP00
P34	29				TI001/TO00/TIP01/TOP01
P35	30				TI010/TO01
P36	31		No		–
P37	32				–
P38	35				SDA0
P39	36				SCL0
P40	22	I/O	Yes	Port 4 I/O port Input/output can be specified in 1-bit units. P41 and P42 can be specified as N-ch open-drain output in 1-bit units.	SI00/RXD2 Note 2
P41	23				SO00/TXD2
P42	24				$\overline{\text{SCK00}}$
P50	37	I/O	Yes	Port 5 I/O port Input/output can be specified in 1-bit units. P54 and P55 can be specified as N-ch open-drain output in 1-bit units.	TI011/RTP00/KR0
P51	38				TI50/RTP01/KR1
P52	39				TO50/RTP02/KR2/DDI Note 3
P53	40				SIA0/RTP03/KR3/DDO Note 3
P54	41				SOA0/RTP04/KR4/DCK Note 3
P55	42				SCKA0/RTP05/KR5/DMS Note 3

Notes 1. Care must be exercised in processing the P05 pin when reset is released.

In the V850ES/KJ2, perform the following operations before starting operation after reset is released. If the following operations are not performed, a normal operation is not executed.

<1> Input a low level to the P05/INTP2 pin.

<2> Clear the OCDM.OCDM0 bit to 0.

Fix the P05/INTP2 pin to low-level input until the processing of <2> is completed.

2. The V850ES/KJ2 also assigns the RXD2 pin function to the P80 pin. If the P40 and P80 pins are used as the RXD2 pin simultaneously, the UART2 receive operation may not be performed correctly. Therefore, do not use the P40 and P80 pins as the RXD2 pin simultaneously.

3. The $\overline{\text{DRST}}$, DDI, DDO, DCK and DMS pins can be used only in the μPD70F3734.

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Pin Name	Pin No.	I/O	Pull-up Resistor	Function	Alternate Function
P60	43	I/O	Yes	Port 6 I/O port Input/output can be specified in 1-bit units. P67 and P68 can be specified as N-ch open-drain output in 1-bit units. P614 and P615 are fixed to N-ch open-drain output.	RTP10
P61	44				RTP11
P62	45				RTP12
P63	46				RTP13
P64	47				RTP14
P65	48				RTP15
P66	49				SI02
P67	50				SO02
P68	51				$\overline{\text{SCK02}}$
P69	52				TI040
P610	53				TI041
P611	54				TO04
P612	55				TI050
P613	56				TI051/TO05
P614	57		No		–
P615	58				–
P70	144	Input	No	Port 7 Input port	ANI0
P71	143				ANI1
P72	142				ANI2
P73	141				ANI3
P74	140				ANI4
P75	139				ANI5
P76	138				ANI6
P77	137				ANI7
P78	136				ANI8
P79	135				ANI9
P710	134				ANI10
P711	133				ANI11
P712	132				ANI12
P713	131				ANI13
P714	130				ANI14
P715	129				ANI15
P80	59	I/O	Yes	Port 8 I/O port Input/output can be specified in 1-bit units. N-ch open-drain output can be specified in 1-bit units.	RXD2[Note]/SDA1
P81	60				TXD2/SCL1

Note The V850ES/KJ2 also assigns the RXD2 pin function to the P40 pin. If the P40 and P80 pins are used as the RXD2 pin simultaneously, the UART2 receive operation may not be performed correctly. Therefore, do not use the P40 and P80 pins as the RXD2 pin simultaneously.

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Pin Name	Pin No.	I/O	Pull-up Resistor	Function	Alternate Function
P90	61	I/O	Yes	Port 9 I/O port Input/output can be specified in 1-bit units. P98, P99, P911, and P912 can be specified as N-ch open-drain output in 1-bit units.	A0/TXD1/KR6
P91	62				A1/RXD1/KR7
P92	63				A2/TI020/TO02
P93	64				A3/TI021
P94	65				A4/TI030/TO03
P95	66				A5/TI031
P96	67				A6/TI51/TO51
P97	68				A7/SI01
P98	69				A8/SO01
P99	70				A9/$\overline{\text{SCK01}}$
P910	71				A10/SIA1
P911	72				A11/SOA1
P912	73				A12/$\overline{\text{SCKA1}}$
P913	74				A13/INTP4
P914	75				A14/INTP5
P915	76				A15/INTP6
PCD0	77	I/O	Yes	Port CD I/O port Input/output can be specified in 1-bit units.	–
PCD1	78				–
PCD2	79				–
PCD3	80				–
PCM0	85	I/O	Yes	Port CM I/O port Input/output can be specified in 1-bit units.	$\overline{\text{WAIT}}$
PCM1	86				CLKOUT
PCM2	87				$\overline{\text{HLDAK}}$
PCM3	88				$\overline{\text{HLDRQ}}$
PCM4	89				–
PCM5	90				–
PCS0	81	I/O	Yes	Port CS I/O port Input/output can be specified in 1-bit units.	$\overline{\text{CS0}}$
PCS1	82				$\overline{\text{CS1}}$
PCS2	83				$\overline{\text{CS2}}$
PCS3	84				$\overline{\text{CS3}}$
PCS4	91				–
PCS5	92				–
PCS6	93				–
PCS7	94				–
PCT0	95	I/O	Yes	Port CT I/O port Input/output can be specified in 1-bit units.	$\overline{\text{WR0}}$
PCT1	96				$\overline{\text{WR1}}$
PCT2	97				–
PCT3	98				–
PCT4	99				$\overline{\text{RD}}$
PCT5	100				–
PCT6	101				ASTB
PCT7	102				–

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Pin Name	Pin No.	I/O	Pull-up Resistor	Function	Alternate Function
PDH0	121	I/O	Yes	Port DH I/O port Input/output can be specified in 1-bit units.	A16
PDH1	122				A17
PDH2	123				A18
PDH3	124				A19
PDH4	125				A20
PDH5	126				A21
PDH6	127				A22
PDH7	128				A23
PDL0	105	I/O	Yes	Port DL I/O port Input/output can be specified in 1-bit units.	AD0
PDL1	106				AD1
PDL2	107				AD2
PDL3	108				AD3
PDL4	109				AD4
PDL5	110				AD5/FLMD1
PDL6	111				AD6
PDL7	112				AD7
PDL8	113				AD8
PDL9	114				AD9
PDL10	115				AD10
PDL11	116				AD11
PDL12	117				AD12
PDL13	118				AD13
PDL14	119				AD14
PDL15	120				AD15

(2) Non-port pins **(1/5)**

Pin Name	Pin No.	I/O	Pull-up Resistor	Function	Alternate Function
A0	61	Output	Yes	Address bus for external memory (when using a separate bus)	P90/TXD1/KR6
A1	62				P91/RXD1/KR7
A2	63				P92/TI020/TO02
A3	64				P93/TI021
A4	65				P94/TI030/TO03
A5	66				P95/TI031
A6	67				P96/TI51/TO51
A7	68				P97/SI01
A8	69				P98/SO01
A9	70				P99/$\overline{\text{SCK01}}$
A10	71				P910/SIA1
A11	72				P911/SOA1
A12	73				P912/$\overline{\text{SCKA1}}$
A13	74				P913/INTP4
A14	75				P914/INTP5
A15	76				P915/INTP6
A16	121	Output	Yes	Address bus for external memory	PDH0
A17	122				PDH1
A18	123				PDH2
A19	124				PDH3
A20	125				PDH4
A21	126				PDH5
A22	127				PDH6
A23	128				PDH7
AD0	105	I/O	Yes	Address/data bus for external memory	PDL0
AD1	106				PDL1
AD2	107				PDL2
AD3	108				PDL3
AD4	109				PDL4
AD5	110				PDL5/FLMD1
AD6	111				PDL6
AD7	112				PDL7
AD8	113				PDL8
AD9	114				PDL9
AD10	115				PDL10
AD11	116				PDL11
AD12	117				PDL12
AD13	118				PDL13
AD14	119				PDL14
AD15	120				PDL15

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Pin Name	Pin No.	I/O	Pull-up Resistor	Function	Alternate Function
ADTRG	27	Input	Yes	A/D converter external trigger input	P32/ASCK0/TO01
ANI0	144	Input	No	Analog voltage input for A/D converter	P70
ANI1	143				P71
ANI2	142				P72
ANI3	141				P73
ANI4	140				P74
ANI5	139				P75
ANI6	138				P76
ANI7	137				P77
ANI8	136				P78
ANI9	135				P79
ANI10	134				P710
ANI11	133				P711
ANI12	132				P712
ANI13	131				P713
ANI14	130				P714
ANI15	129				P715
ANO0	3	Output	Yes	Analog voltage output for D/A converter	P10
ANO1	4				P11
ASCK0	27	Input	Yes	UART0 serial clock input	P32/ADTRG/TO01
ASTB	101	Output	Yes	Address strobe signal output for external memory	PCT6
AV_{REF0}	1	–	–	Reference voltage for A/D converter and positive power supply for alternate-function ports	–
AV_{REF1}	5	–	–	Reference voltage for D/A converter and positive power supply for alternate-function ports	–
AV_{SS}	2	–	–	Ground potential for A/D and D/A converters and alternate-function ports	–
BV_{DD}	104	–	–	Positive power supply for bus interface and alternate-function ports	–
BV_{SS}	103	–	–	Ground potential for bus interface and alternate-function ports	–
CLKOUT	86	Output	Yes	Internal system clock output	PCM1
$\overline{CS0}$	81	Output	Yes	Chip select output	PCS0
$\overline{CS1}$	82				PCS1
$\overline{CS2}$	83				PCS2
$\overline{CS3}$	84				PCS3
DCK Note	41	Input	Yes	Debug clock input	P54/SOA0/RTP04/KR4
DDI Note	39	Input	Yes	Debug data input	P52/TO50/RTP02/KR2
DDO Note	40	Output	Yes	Debug data output	P53/SIA0/RTP03/KR3
DMS Note	42	Input	Yes	Debug mode select input	P55/$\overline{SCKA0}$/RTP05/KR5
$\overline{DRST}$ Note	20	Input	Yes	Debug reset input	P05/INTP2

Note The $\overline{DRST}$, DDI, DDO, DCK and DMS pins can be used only in the μPD70F3734.

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Pin Name	Pin No.	I/O	Pull-up Resistor	Function	Alternate Function
$\overline{\text{HLDAK}}$	87	Output	Yes	Bus hold acknowledge output	PCM2
$\overline{\text{HLDRQ}}$	88	Input	Yes	Bus hold request input	PCM3
INTP0	18	Input	Yes	External interrupt request input (maskable, analog noise elimination)	P03
INTP1	19				P04
INTP2	20				P05/$\overline{\text{DRST}}$ Note
INTP3	21			External interrupt request input (maskable, digital + analog noise elimination)	P06
INTP4	74			External interrupt request input (maskable, analog noise elimination)	P913/A13
INTP5	75				P914/A14
INTP6	76				P915/A15
INTP7	26				P31/RXD0/TO03
KR0	37	Input	Yes	Key return input	P50/TI011/RTP00
KR1	38				P51/TI50/RTP01
KR2	39				P52/TO50/RTP02/DDI Note
KR3	40				P53/SIA0/RTP03/DDO Note
KR4	41				P54/SOA0/RTP04/DCK Note
KR5	42				P55/$\overline{\text{SCKA0}}$/RTP05/DMS Note
KR6	61				P90/A0/TXD1
KR7	62				P91/A1/RXD1
NMI	17	Input	Yes	External interrupt input (non-maskable, analog noise elimination)	P02
$\overline{\text{RD}}$	99	Output	Yes	Read strobe signal output for external memory	PCT4
REGC	10	–	–	Connecting capacitor for regulator output stabilization	–
$\overline{\text{RESET}}$	14	Input	–	System reset input	–
RTP00	37	Output	Yes	Real-time output port	P50/TI011/KR0
RTP01	38				P51/TI50/KR1
RTP02	39				P52/TO50/KR2/DDI Note
RTP03	40				P53/SIA0/KR3/DDO Note
RTP04	41				P54/SOA0/KR4/DCK Note
RTP05	42				P55/$\overline{\text{SCKA0}}$/KR5/DMS Note
RTP10	43				P60
RTP11	44				P61
RTP12	45				P62
RTP13	46				P63
RTP14	47				P64
RTP15	48				P65
RXD0	26	Input	Yes	Serial receive data input for UART0	P31/INTP7/TO03
RXD1	62	Input	Yes	Serial receive data input for UART1	P91/A1/KR7

Note The $\overline{\text{DRST}}$, DDI, DDO, DCK and DMS pins can be used only in the μPD70F3734.

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Pin Name	Pin No.	I/O	Pull-up Resistor	Function	Alternate Function
RXD2	22	Input	Yes	Serial receive data input for UART2	P40[Note 1]/SI00
	59				P80[Note 1]/SDA1
$\overline{SCK00}$	24	I/O	Yes	Serial clock I/O for CSI00 to CSI02, CSIA0, CSIA1 N-ch open-drain output can be specified in 1-bit units.	P42
$\overline{SCK01}$	70				P99/A9
$\overline{SCK02}$	51				P68
$\overline{SCKA0}$	42				P55/RTP05/KR5/DMS[Note 2]
$\overline{SCKA1}$	73				P912/A12
SCL0	36	I/O	No	Serial clock I/O for I^2C0 Fixed to N-ch open-drain output	P39
SCL1	60		Yes	Serial clock I/O for I^2C1 N-ch open-drain output can be specified	P81/TXD2
SDA0	35	I/O	No	Serial transmit/receive data I/O for I^2C0 Fixed to N-ch open-drain output	P38
SDA1	59		Yes	Serial transmit/receive data I/O for I^2C1 N-ch open-drain output can be specified	P80/RXD2
SI00	22	Input	Yes	Serial receive data input for CSI00	P40/RXD2
SI01	68			Serial receive data input for CSI01	P97/A7
SI02	49			Serial receive data input for CSI02	P66
SIA0	40			Serial receive data input for CSIA0	P53/RTP03/KR3/DDO[Note 2]
SIA1	71			Serial receive data input for CSIA1	P910/A10
SO00	23	Output	Yes	Serial transmit data output for CSI00 to CSI02, CSIA0, CSIA1 N-ch open-drain output can be specified in 1-bit units.	P41/TXD2
SO01	69				P98/A8
SO02	50				P67
SOA0	41				P54/RTP04/KR4/DCK[Note 2]
SOA1	72				P911/A11
TI000	28	Input	Yes	Capture trigger input/external event input for TM00	P33/TO00/TIP00/TOP00
TI001	29			Capture trigger input for TM00	P34/TO00/TIP01/TOP01
TI010	30			Capture trigger input/external event input for TM01	P35/TO01
TI011	37			Capture trigger input for TM01	P50/RTP00/KR0
TI020	63			Capture trigger input/external event input for TM02	P92/A2/TO02
TI021	64			Capture trigger input for TM02	P93/A3
TI030	65			Capture trigger input/external event input for TM03	P94/A4/TO03
TI031	66			Capture trigger input for TM03	P95/A5
TI040	52			Capture trigger input/external event input for TM04	P69
TI041	53			Capture trigger input for TM04	P610
TI050	55			Capture trigger input/external event input for TM05	P612
TI051	56			Capture trigger input for TM05	P613/TO05

Notes 1. The V850ES/KJ2 also assigns the RXD2 pin function to the P40 pin. If the P40 and P80 pins are used as the RXD2 pin simultaneously, the UART2 receive operation may not be performed correctly. Therefore, do not use the P40 and P80 pins as the RXD2 pin simultaneously.

2. The $\overline{DRST}$, DDI, DDO, DCK and DMS pins can be used only in the μPD70F3734.

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Pin Name	Pin No.	I/O	Pull-up Resistor	Function	Alternate Function
TI50	38	Input	Yes	External event input for TM50	P51/RTP01/KR1
TI51	67			External event input for TM51	P96/A6/TO51
TIP00	28			Capture trigger input/external event input for TMP0	P33/TI000/TO00/TOP00
TIP01	29			Capture trigger input for TMP0	P34/TI001/TO00/TOP01
TO00	28	Output	Yes	Timer output for TM00	P33/TI000/TIP00/TOP00
	29				P34/TI001/TIP01/TOP01
TO01	27			Timer output for TM01	P32/ASCK0/ADTRG
	30				P35/TI010
TO02	25			Timer output for TM02	P30/TXD0
	63				P92/A2/TI020
TO03	26			Timer output for TM03	P31/RXD0/INTP7
	65				P94/A4/TI030
TO04	54			Timer output for TM04	P611
TO05	56			Timer output for TM05	P613/TI051
TO50	39			Timer output for TM50	P52/RTP02/KR2/DDI [Note]
TO51	67			Timer output for TM51	P96/A6/TI51
TOH0	6			Timer output for TMH0	P00
TOH1	7			Timer output for TMH1	P01
TOP00	28			Timer output for TMP0	P33/TI000/TO00/TIP00
TOP01	29				P34/TI001/TO00/TIP01
TXD0	25	Output	Yes	Serial transmit data output for UART0	P30/TO02
TXD1	61			Serial transmit data output for UART1	P90/A0/KR6
TXD2	23			Serial transmit data output for UART2	P41/SO00
	60				P81/SCL1
V_{DD}	9	–	–	Positive power supply pin for internal	–
V_{SS}	11	–	–	Ground potential for internal	–
$\overline{WAIT}$	85	Input	No	External wait input	PCM0
$\overline{WR0}$	95	Output	No	Write strobe for external memory (lower 8 bits)	PCT0
$\overline{WR1}$	96			Write strobe for external memory (higher 8 bits)	PCT1
X1	12	Input	No	Connecting resonator for main clock	–
X2	13	–	No		–
XT1	15	Input	No	Connecting resonator for subclock	–
XT2	16	–	No		–

Note The $\overline{DRST}$, DDI, DDO, DCK and DMS pins can be used only in the μPD70F3734.