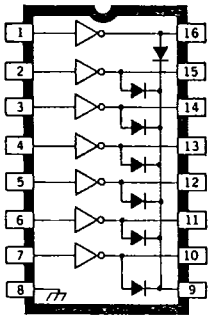
2001 THRU 2025

T-43-25

HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

ULS20XXH/R



Dwg. No. A-9594

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE}
(ULS200X*, ULS201X*) . . . . . **50 V**
(ULS202X*) . . . . . **95 V**
Input Voltage, V_{IN}
(ULS20X2*, X3*, X4*) . . . . . **30 V**
(ULS20X5*) . . . . . **15 V**
Peak Output Current, I_{OUT}
(ULS200X*, ULS202X*) . . . . . **500 mA**
(ULS201X*) . . . . . **600 mA**
Ground Terminal Current, I_{GND} . . . . . **3.0 A**
Continuous Input Current, I_{IN} . . . . . **25 mA**
Power Dissipation, P_D
(one Darlington pair) . . . . . **1.0 W**
(total package) . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-55°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

X = digit to identify specific device. Characteristic shown applies to family of devices with remaining digits as shown.

*Complete part number includes a final letter to indicate package.

Comprised of seven silicon NPN Darlington power drivers on a common monolithic substrate, Series ULS2000EK, ULS2000H, and ULS2000R arrays drive relays, solenoids, magnetic print hammers, lamps, and other devices in high-reliability military or aerospace applications with up to 3 A of output current per package.

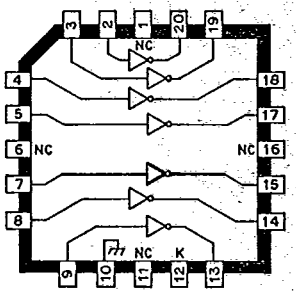
These devices are screened to MIL-STD-883, Class B and are supplied in a leadless ceramic chip carrier with Kovar lid (suffix 'EK'), the popular ceramic/metal side-brazed 16-pin hermetic package (suffix 'H'), or ceramic/glass cer-DIP hermetic package (suffix 'R'). All package styles conform to the dimensional requirements of MIL-M-38510 and are rated for operation over the full military temperature range of -55°C to +125°C. Reverse-bias burn-in and 100% high-reliability screening are standard.

The 35 integrated circuits described here permit the circuit designer to select the optimal device for any application. In addition to the three package styles (note that the ceramic chip carrier is available only for the ULS2001EK through ULS2005EK devices), there are five input characteristics, two output-voltage ratings, and two output-current ratings. The appropriate part for specific applications can be determined from the Device Part Number Designation chart. All units have open-collector outputs and on-chip diodes for inductive-load transient suppression .

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Peak Output Current to 600 mA
- Transient-Protected Outputs
- High-Reliability Screening to MIL-STD-883, Class B
- -55°C to +125°C Temperature Range

ULS200XEK

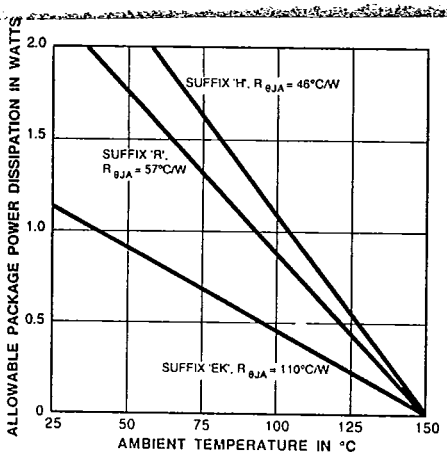


Dwg. No. A-14,378

Always order by complete part number, e.g., ULS2013H883. See matrix on next page.

2001 THRU 2025
HIGH VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

T-43-25



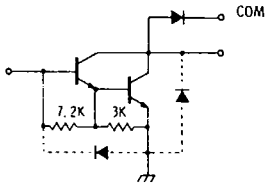
Dwg. GM-004

DEVICE PART NUMBER DESIGNATION

$V_{CE(MAX)}$	50 V	50 V	95 V
$I_{C(MAX)}$	500 mA	600 mA	500 mA
Logic		**Part Number**	
General Purpose PMOS, CMOS	ULS2001*	ULS2011*	ULS2021*
14-25 V PMOS	ULS2002*	ULS2012*	ULS2022*
5 V TTL, CMOS	ULS2003*	ULS2013*	ULS2023*
6-15 V CMOS, PMOS	ULS2004*	ULS2014*	ULS2024*
High-Output TTL	ULS2005*	ULS2015*	ULS2025*

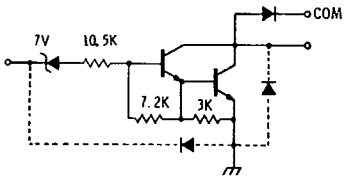
PARTIAL SCHEMATICS

ULS20X1*
(Each Driver)



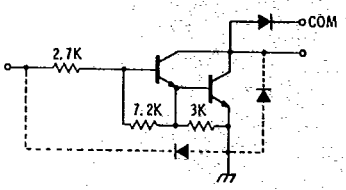
Dwg. No A-9595

ULS20X2*
(Each Driver)



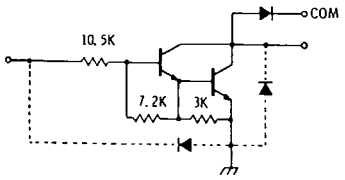
Dwg. No A-9650

ULS20X3*
(Each Driver)



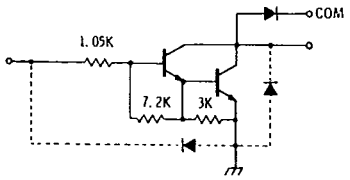
Dwg. No. A-9651

ULS20X4*
(Each Driver)



Dwg. No. A-9898A

ULS20X5*
(Each Driver)



Dwg. No. A-10,228

** Complete part number includes a final letter to indicate package (EK = leadless ceramic chip carrier, H = ceramic/metal side-brazed, R = cermic/glass cer-DIP.*

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

2001 THRU 2025
HIGH VOLTAGE, HIGH CURRENT DARLINGTON ARRAYS

T-43-25

ULS2001EK/H/R THRU ULS2005EK/H/R
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS2002*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS2004*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA†, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS2002*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS2003*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS2004*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS2005*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS2002*	-55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	13	V
		ULS2003*	-55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V

*Complete part number includes a final letter to indicate package (EK = leadless/ceramic chip carrier, H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

Continued next page...

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

2001 THRU 2025
HIGH VOLTAGE, HIGH CURRENT DARLINGTON ARRAYS

T-43-25

ULS2001EK/H/R THRU ULS2005EK/H/R ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Input Voltage (cont.)	$V_{IN(ON)}$	ULS2004*	-55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS2005*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2001*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package (EK = leadless ceramic chip carrier, H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

2001 THRU 2025
HIGH VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

T-43-25

ULS2011H/R THRU ULS2015H/R
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS2012*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS2014*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 500 mA, I_B = 1100 µA	2	—	1.8	2.1	V
				I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
			+25°C	I_C = 500 mA, I_B = 600 µA	2	—	1.7	1.9	V
				I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+125°C	I_C = 500 mA†, I_B = 600 µA	2	—	1.8	2.1	V
				I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA†, I_B = 350 µA	2	—	1.3	1.5	V
Input Current	$I_{IN(ON)}$	ULS2012*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS2013*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS2014*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS2015*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS2012*	-55°C	V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	23.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	17	V
		ULS2013*	-55°C	V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	6.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	3.5	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

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NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

2001 THRU 2025
HIGH VOLTAGE HIGH CURRENT DARLINGTON ARRAYS

T-43-25

ULS2011H/R THRU ULS2015H/R ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Input Voltage (cont.)	$V_{IN(ON)}$	ULS2014*	-55°C	V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	17	V
			+125°C	V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	9.5	V
		ULS2015*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	3.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2011*	-55°C	V_{CE} = 2.0 V, I_C = 500 mA	2	450	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 500 mA	2	900	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA†	7	—	1.7	2.0	V
				I_F = 500 mA†	7	—	—	2.5	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

2001 THRU 2025
HIGH VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

T-43-25

ULS2021H/R THRU ULS2025H/R
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			Units
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	All		V_{CE} = 95 V	1A	—	—	100	µA
		ULS2022*		V_{CE} = 95 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS2024*	+25°C	V_{CE} = 95 V, V_{IN} = 1 V	1B	—	—	500	µA
			+125°C	V_{CE} = 95 V, V_{IN} = 0.5 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA†, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS2022*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS2023*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS2024*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS2025*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	20	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS2022*	-55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	13	V
		ULS2023*	-55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

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NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

2001 THRU 2025
HIGH VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

T-43-25

ULS2021H/R THRU ULS2025H/R ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Input Voltage (cont.)	$V_{IN(ON)}$	ULS2024*	-55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS2025*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2021*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 95 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate pachage (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

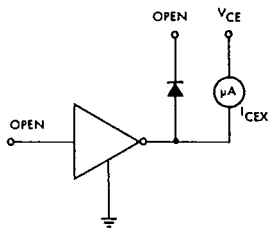
NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

T-43-25

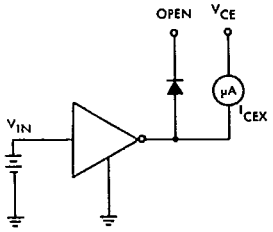
TEST FIGURES

FIGURE 1A



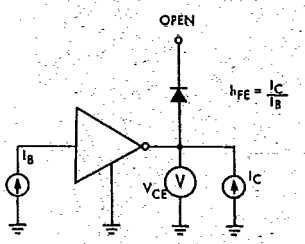
Dwg. No. A.-9729A

FIGURE 1B



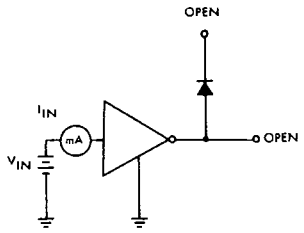
Dwg. No. A-9730A

FIGURE 2



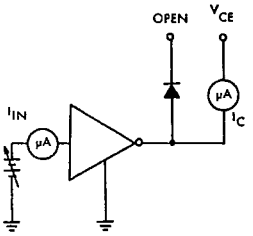
Dwg. No. A-9731

FIGURE 3



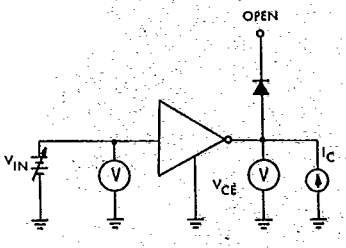
Dwg. No. A-9732

FIGURE 4



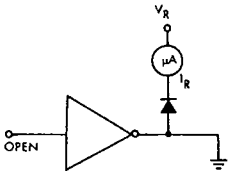
Dwg. No. A-9733A

FIGURE 5



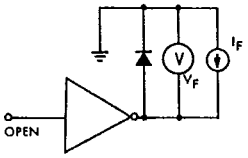
Dwg. No. A-9734A

FIGURE 6



Dwg. No. A-9735A

FIGURE 7

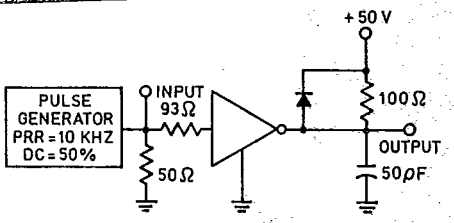


Dwg. No. A-9736

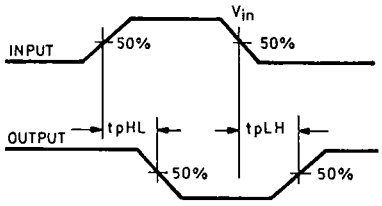
2001 THRU 2025
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

T-43-25

	V_{IN}
ULS20X1*	3.5 V
ULS20X2*	13 V
ULS20X3*	3.5 V
ULS20X4*	12 V
ULS20X5*	3.5 V



Dwg. No. A-13,273



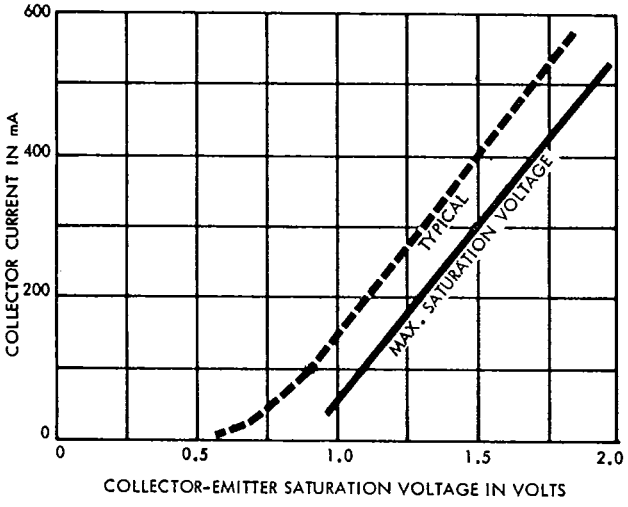
Dwg. No. A-13,272

* Complete part number includes a final letter to indicate package.

X= Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown.

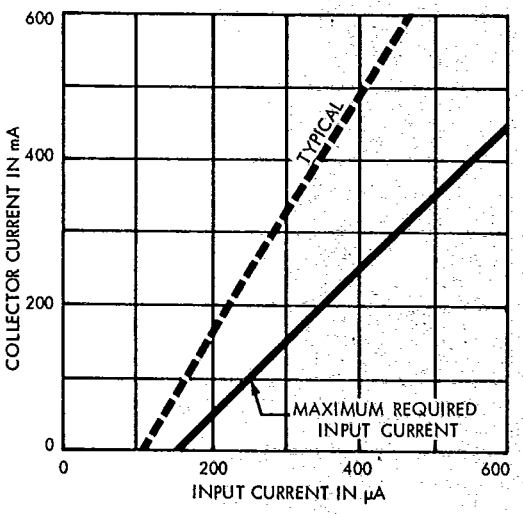
FIGURE 8

COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



Dwg. No. A-9754C

COLLECTOR CURRENT AS A FUNCTION OF INPUT VOLTAGE



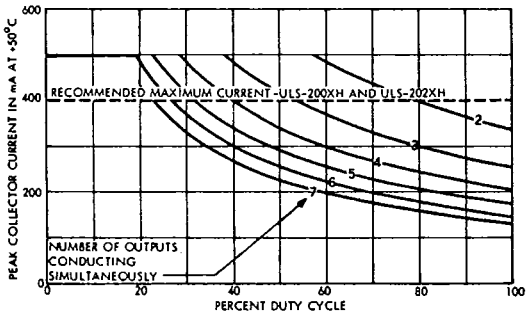
Dwg. No. A-10,872B

2001 THRU 2025
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

T-43-25

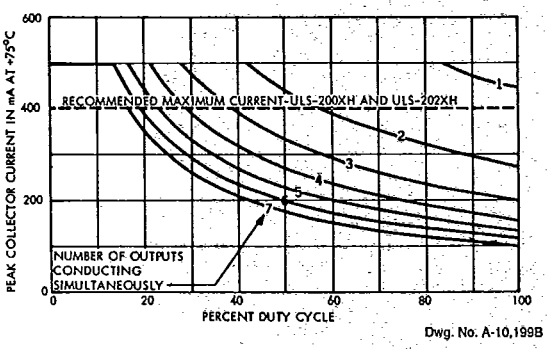
ULS20XXH

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



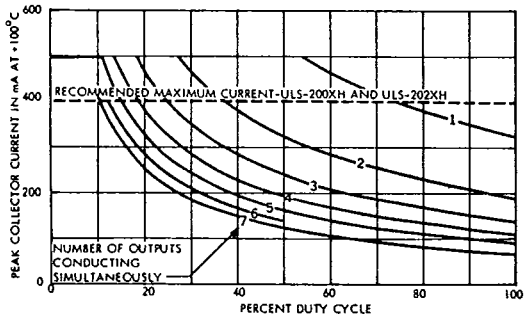
Dwg. No. A-10,197B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



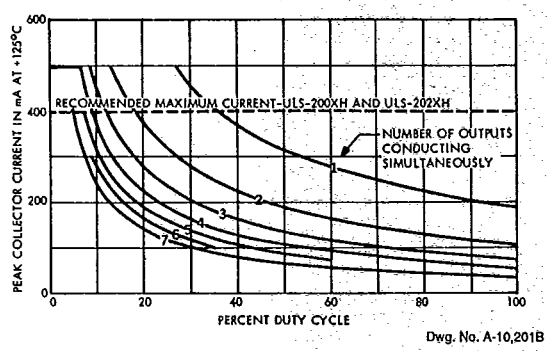
Dwg. No. A-10,199B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-10,200B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C



Dwg. No. A-10,201B

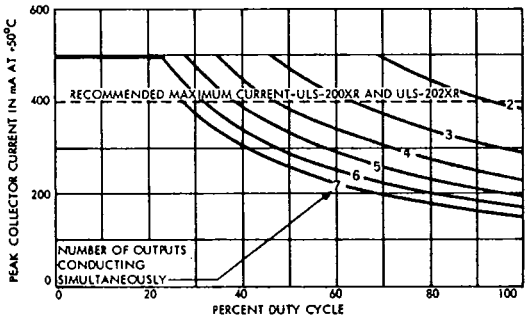
X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

2001 THRU 2025
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

T-43-25

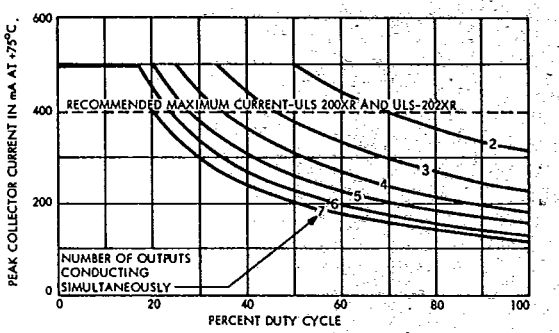
ULS20XXR

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



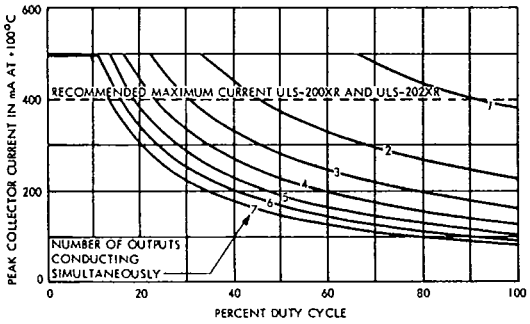
Dwg. No. A-10,883B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



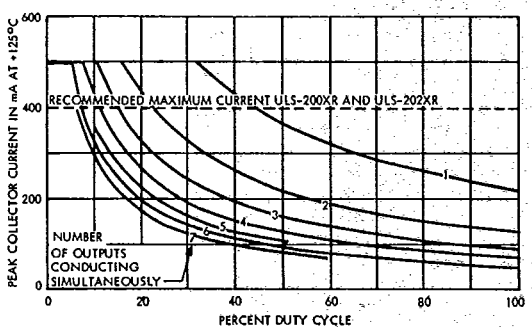
Dwg. No. A-10,887B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-12,434

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C



Dwg. No. A-12,435

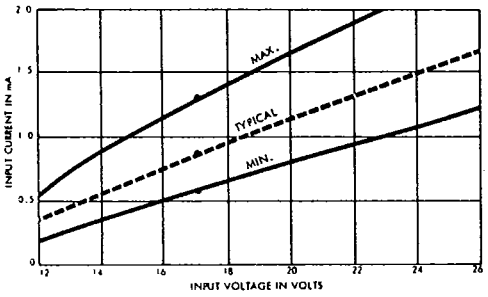
X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

2001 THRU 2025
HIGH VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

T-43-25

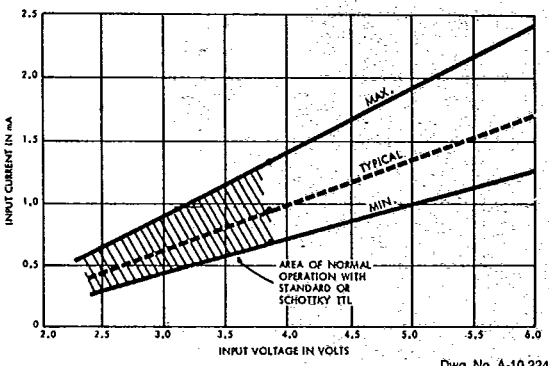
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

ULS20X2*



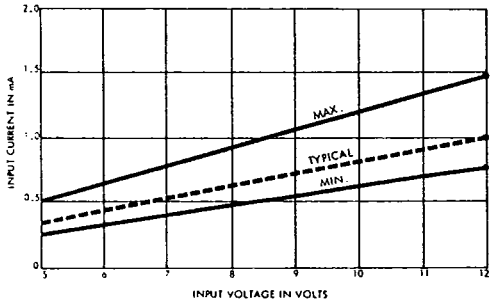
Dwg. No. A-10,225A

ULS20X3*



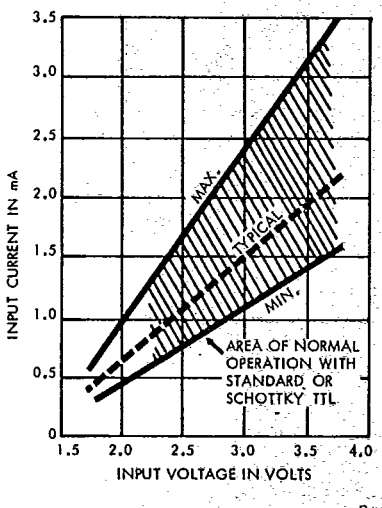
Dwg. No. A-10,224A

ULS20X4*



Dwg. No. A-10,226A

ULS20X5*



Dwg. No. A-10,874A

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.