FAIRCHILD SEMICONDUCTOR™

ML4411*/ML4411A**

Sensorless Spindle Motor Controller

GENERAL DESCRIPTION

The ML4411 provides complete commutation for delta or wye wound Brushless DC (BLDC) motors without the need for signals from Hall Effect Sensors. This IC senses the back EMF of the three motor windings (no neutral required) to determine the proper commutation phase angle using Phase Lock Loop techniques. This technique will commutate virtually any 3-phase BLDC motor and is insensitive to PWM noise and motor snubbing. The ML4411 is architecturally similar to the ML4410 but with improved braking and brown-out recovery circuitry.

Included in the ML4411 is the circuitry necessary for a Hard Disk Drive microcontroller driven control loop. The ML4411 controls motor current with either a constant off-time PWM or linear current control driven by the microcontroller. Braking and Power Fail are also included in the ML4411.

The timing of the start-up sequencing is determined by the micro, allowing the system to be optimized for a wide range of motors and inertial loads.

The ML4411 modulates the gates of external N-Channel power MOSFETs to regulate the motor current. The IC drives P-Channel MOSFETs directly.

The ML4411A includes a comparator on the P3 output to prevent cross-conduction.

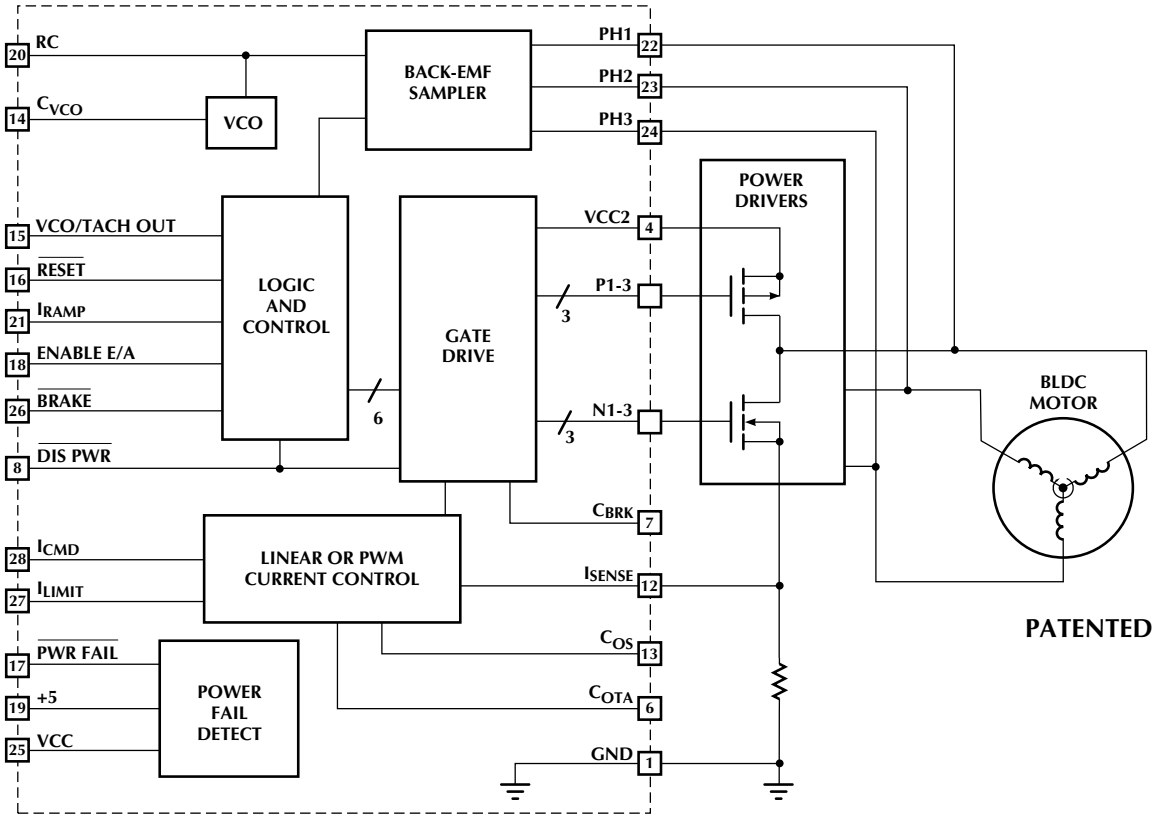
FEATURES

- Back-EMF commutation provides maximum torque for minimum “spin-up” time for spindle motors
- Accurate, jitter-free phase locked motor speed feedback output
- Linear or PWM motor current control
- Easy microcontroller interface for optimized start-up sequencing and speed control
- Power fail detect circuit with delayed braking
- Drives external N-channel FETs and P-channel FETs
- Back-EMF comparator detects motor rotation after power fail for fast re-lock after brownout

* This Product Is Obsolete

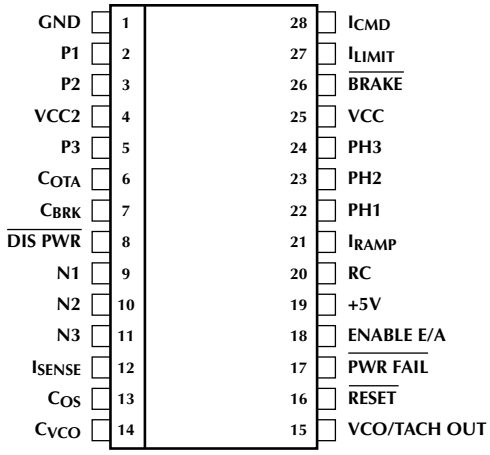
** This Product Is End Of Life As Of August 1, 2000

BLOCK DIAGRAM



PIN CONFIGURATION

ML4411
28-Pin SOIC (S28W)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	GND	Signal and Power Ground
2	P1	Drives the external P-channel transistor driving motor PH1
3	P2	Drives the external P-channel transistor driving motor PH2
4	V_{CC2}	12V power and power for the braking function
5	P3	Drives the external P-channel transistor driving motor PH3
6	C_{OTA}	Compensation capacitor for linear motor current amplifier loop
7	C_{BRK}	Capacitor which stores energy to charge N-channel MOSFETs for braking with power off.
8	$\overline{\text{DIS}}$ $\overline{\text{PWR}}$	A logic 0 on this pin turns off the N and P outputs and causes the TACH comparator output to appear on TACH OUT
9-11	N1, N2 N3	Drives the external N-channel MOSFETs for PH1, PH2, PH3
12	I_{SENSE}	Motor current sense input
13	C_{OS}	Timing capacitor for fixed off-time PWM current control
14	C_{VCO}	Timing capacitor for VCO
15	VCO/TACH OUT	Logic Output from VCO or TACH comparator

PIN	NAME	FUNCTION
16	$\overline{\text{RESET}}$	Input which holds VCO off and sets the IC to the RESET condition
17	$\overline{\text{PWR}}$ $\overline{\text{FAIL}}$	A "0" output indicates 5V or 12V is under-voltage. This is an open collector output with a 4.5kΩ pull-up to +5V
18	ENABLE E/A	A "1" logic input enables the error amplifier and closes the back-EMF feedback loop
19	+5V	5V power supply input
20	RC	VCO loop filter components
21	I_{RAMP}	Current into this pin sets the initial acceleration rate of the VCO during start-up
22	PH1	Motor Terminal 1
23	PH2	Motor Terminal 2
24	PH3	Motor Terminal 3
25	V_{CC}	12V power supply. Terminal which is sensed for power fail
26	$\overline{\text{BRAKE}}$	A "0" activates the braking circuit
27	I_{LIMIT}	Sets the threshold for the PWM comparator
28	I_{CMD}	Current Command for Linear Current amplifier

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (pins 4, 25) 14V
Output Current (pins 2, 3, 5, 9,10,11) ..... ±150mA
Logic Inputs (pins 16, 17, 18, 25) ..... –0.3 to 7V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 150°C
Thermal Resistance (θ_{JA}) ..... 60°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
VCC Voltage +12V (pin 25) ..... 12V ± 10%
+5V (pin 19) ..... 5V ± 10%
I(RAMP) current (Pin 21) ..... 0 to 100µA
I Control Voltage Range (pins 27, 28) ..... 0V to 7V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, $V_{CC} = V_{CC2}$ = 12V, R_{SENSE} = 1Ω, $C_{OTA} = C_{VCO}$ = 0.01µF, C_{OS} = 0.02µF

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator (VCO) Section (V_{PIN16} = 5V)					
Frequency vs. $V_{PIN\ 20}$	1V ≤ V_{PIN20} ≤ 10V		300		Hz/V
Frequency	V_{VCO} = 6V	1450	1800	2150	Hz
	V_{VCO} = 0.5V	70	140	210	Hz
Reset Voltage at C_{VCO}	Mode = 0		125	250	mV
Sampling Amplifier (Note 1)					
V_{RC}	State R		125	250	mV
I_{RC}	V_{PIN18} = 0V, R_{RAMP} = 39kΩ	70	100	130	µA
	V_{PIN18} = 5V, State A, V_{PH2} = 4V	30	50	90	µA
	V_{PIN18} = 5V, State A, V_{PH2} = 6V	–13	2	13	µA
	V_{PIN18} = 5V, State A, V_{PH2} = 8V	–30	–50	–90	µA
V_{PIN21}	R_{PIN21} = 39kΩ to +5V	1.0	1.1	1.20	V
Motor Current Control Section					
I_{SENSE} Gain	V_{PIN27} = 5V, 0V ≤ V_{PIN28} ≤ 2.5V	4.5	5	5.5	V/V
One Shot Off Time		12	25	33	µs
I_{CMD} Transconductance Gain			0.19		mmho
I_{CMD}, I_{LIM} Bias Current	V_{IN} = 0	0	–100	–400	nA
Power Fail Detection Circuit					
12V Threshold		9.1	9.8	10.5	V
Hysteresis			150		mV
5V Threshold		3.8	4.25	4.5	V
Hysteresis			70		mV
Logic Inputs					
Voltage High (V_{IH})		2			V
Voltage Low (V_{IL})				0.8	V
Current High (I_{IH})	V_{IN} = 2.7V	–10	1	10	µA
Current Low (I_{IL})	V_{IN} = 0.4V	–500	–350	–200	µA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Braking Circuit (V_{PIN17} = 0V)					
Brake Active Threshold		0.8	1.2	1.6	V
PIN 26 Bias Current	V_{PIN26} = 0V		0.3	1	µA
N-Channel Leakage	V_{CC}, V_{CC2} = 0V V_{PIN17} = 0V, V_N = 4V	0	0.06	10	nA
C_{BRK} Current	V_{CC}, V_{CC2} = 0V, V_{PIN26} = 3V V_{PIN7} = 6V		20	85	µA
Outputs (I_{CMD} = I_{LIMIT} = 2.5V)					
I_P Low	V_P = 0.8V	5	7	19.5	mA
	V_P = 0.4V	2	4		mA
V_P High	I_P = –10µA	V_{CC} – 0.4			V
P3 Comparator Threshold		V_{CC2} – 1.6		V_{CC2} – 0.8	V
V_N High	V_{PIN12} = 0V	V_{CC2} – 3.2	10	V_{CC} – 1.2	V
V_N Low	I_N = 1mA		0.2	0.7	V
LOGIC Low (V_{OL})	I_{OUT} = 0.4mA			0.5	V
VCO/TACH V_{OH}	I_{OUT} = –100µA	2.4			V
POWER FAIL V_{OH}	I_{OUT} = –10µA	V_{PIN19} – 0.2	V_{PIN19} – 0.1	V_{PIN19}	V
Supply Currents (N and P Outputs Open)					
5V Current			3	4	mA
V_{CC} Current			38	50	mA
V_{CC2} Current	ML4411		2	3	mA
V_{CC2} Current	ML4411A		2.6	3.75	mA

Note 1. For explanation of states, see Figure 5 and Table 1.

FUNCTIONAL DESCRIPTION

The ML4411 provides closed-loop commutation for 3-phase brushless motors. To accomplish this task, a VCO, integrating Back-EMF Sampling error amplifier and sequencer form a phase-locked loop, locking the VCO to the back-EMF of the motor. The IC also contains circuitry to control motor current with either linear or constant off-time PWM modes. Braking and power fail detection functions are also provided on chip. The ML4411 is designed to drive external power transistors (N-channel sinking transistors and PNP sourcing transistors) directly.

Start-up sequencing and motor speed control are accomplished by a microcontroller. Speed sensing is accomplished by monitoring the output of the VCO, which will be a signal which is phased-locked to the commutation frequency of the motor.

BACK-EMF SENSING AND COMMUTATOR

The ML4411 contains a patented back-EMF sensing circuit which samples the phase which is not energized (Shaded area in figure 2) to determine whether to increase or decrease the commutator (VCO) frequency. A late commutation causes the error amplifier to charge the filter (RC) on pin 20, increasing the VCO input while early
commutation causes pin 20 discharge. Analog speed control loops can use pin 20 as a speed feedback voltage.

The input impedance of the three PH inputs is about 8KΩ to GND. When operating with a higher voltage motor, the PH inputs should be divided down in voltage so that the maximum voltage at any PH input does not exceed VCC.

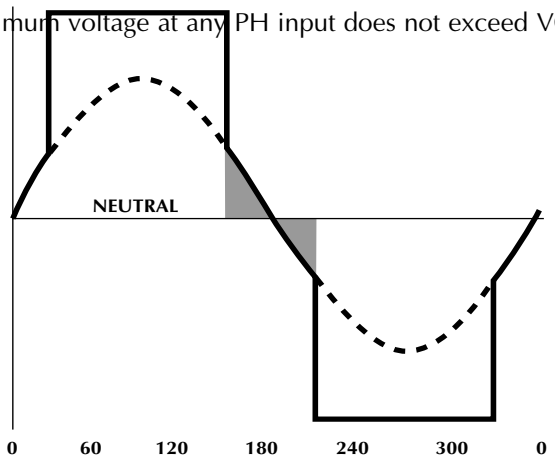


Figure 2. Typical motor phase waveform with Back-EMF superimposed (Ideal Commutation)

VCO AND PHASE DETECTOR CALCULATIONS

The VCO should be set so that at the maximum frequency of operation (the running speed of the motor) the VCO control voltage will be no higher than VCC_{MIN} – 1V. The VCO maximum frequency will be:

$$F_{MAX} = 0.05 \times POLES \times RPM$$

where POLES is the number of poles on the motor and RPM is the maximum motor speed in Revolutions Per

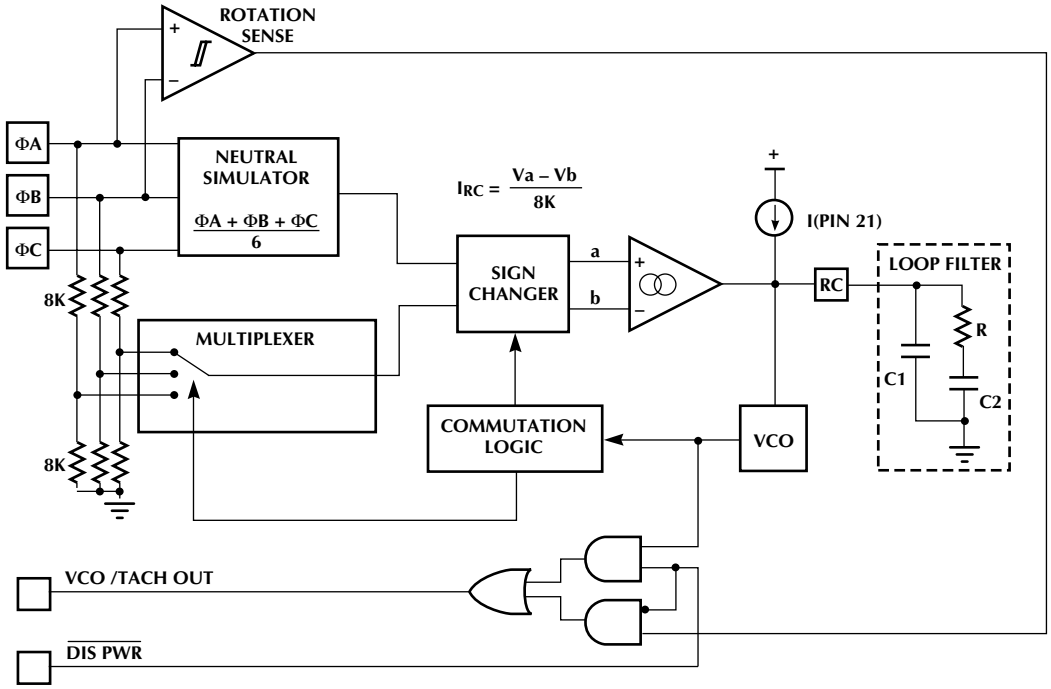


FIGURE 1. BACK EMKF sensing block diagram

Minute.

The minimum VCO gain derived from the specification table (using the minimum Fvco at V_{VCO} = 6V) is:

$$K_{VCO(MIN)} = \frac{2.42 \times 10^{-6}}{C_{VCO}}$$

Assuming that the $V_{VCO(MAX)}$ = 9.5V, then

$$C_{VCO} = \frac{9.5 \times 2.42 \times 10^{-6}}{F_{MAX}}$$

or

$$C_{VCO} = \frac{460}{POLES \times RPM} \mu F$$

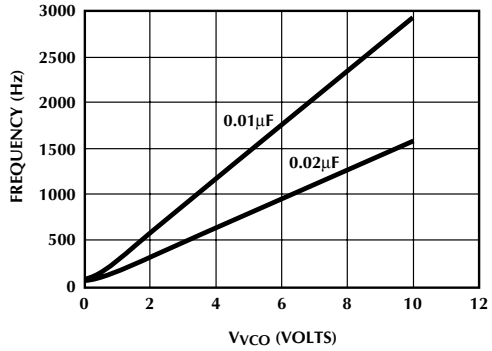


Figure 3. VCO Output Frequency vs. V_{VCO} (Pin 20)

Figure 4 shows the transfer function of the Phase Lock Loop with the phase detector formed from the sampled phase through the Gm amplifier with the loop filtered formed by R, C1, and C2.

The impedance of the loop filter is

$$Z_{RC}(s) = \frac{1}{C_1 s} \frac{(s + \omega_{LEAD})}{(s + \omega_{LAG})}$$

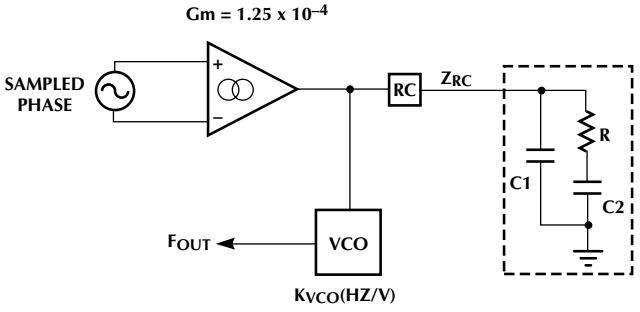


Figure 4. Back EMF Phase Lock Loop Components

Where the lead and lag frequencies are set by:

$$\omega_{LEAD} = \frac{1}{R C_2}$$

$$\omega_{LAG} = \frac{C_1 + C_2}{R C_1 C_2}$$

START-UP SEQUENCING

When the motor is initially at rest, it is generating no back-EMF. Because a back-EMF signal is required for closed loop commutation, the motor must be started "open-loop" until a velocity sufficient to generate some back-EMF is attained (around 100 RPM). The following steps are a typical procedure for starting a motor which is at rest.

Step 1: The IC is held in reset (state R) with full power applied to the windings (see figure 6). This aligns the rotor to a position which is 30° (electrical) before the center of the first commutation state.

Step 2: Reset is released, and a fixed current is input to pin 21 and appears as a current on pin 20, and will ramp the VCO input voltage, accelerating the motor at a fixed rate.

Step 3: When the motor speed reaches about 100 RPM, the back EMF loop can be closed by pulling pin 18 high.

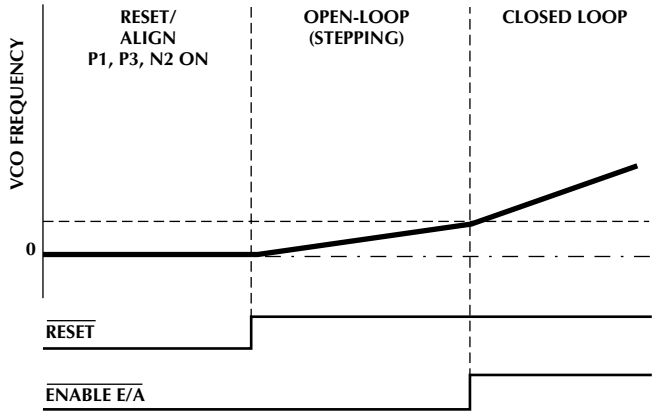


Figure 6. Typical Start-up Sequence.

Using this technique, some reverse rotation is possible. The maximum amount of reverse rotation is 360/N, where N is the number of poles. For an 8 pole motor, 45° reverse rotation is possible.

For quick recovery following a momentary power failure, the following steps can be taken:

STEP	PIN 16	PIN 18	PIN 21	I_{LIMIT} I_{CMD}
1	0	0	FIXED	I_{MAX}
2	1	0	FIXED	I_{MAX}
3	1	1	0	I_{MAX}

Table 2. Start-up Sequence.

STATE	OUTPUTS						INPUT SAMPLING
	N1	N2	N3	P1	P2	P3	
R OR 0	OFF	ON	OFF	ON	OFF	ON	N/A
A	OFF	OFF	ON	ON	OFF	OFF	PH2
B	OFF	OFF	ON	OFF	ON	OFF	PH1
C	ON	OFF	OFF	OFF	ON	OFF	PH3
D	ON	OFF	OFF	OFF	OFF	ON	PH2
E	OFF	ON	OFF	OFF	OFF	ON	PH1
F	OFF	ON	OFF	ON	OFF	OFF	PH3

Table 1. Commutation States.

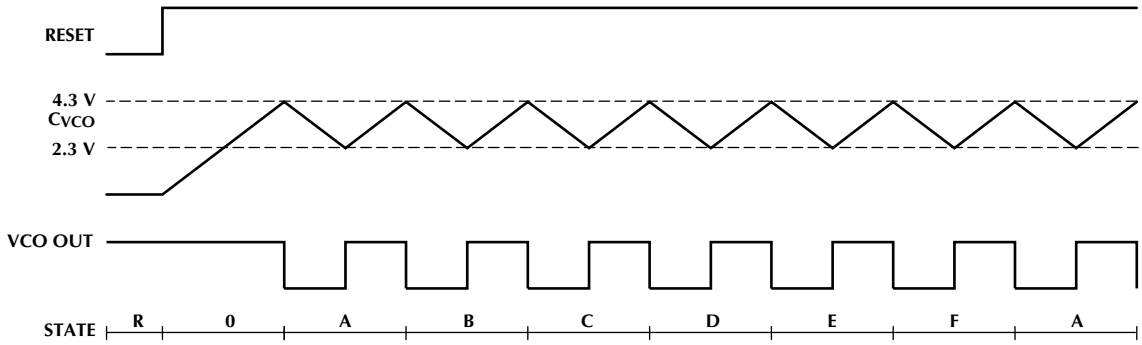


Figure 5. Commutation Timing and Sequencing.

Step 1a: The IC is held in reset (state R) with I_{CMD} low and DIS PWR low. The Micro Processor monitors the VCO/TACH OUT pin to determine if a signal is present. If a signal is present, the frequency is determined (by measuring the period). If a signal is not present, proceed to the routine described above for starting a motor which is a rest.

Step 2a: Release RESET and DIS PWR. Apply a current to pin 21 and monitor the VCO/TACH OUT pin for VCO frequency.

Step 3a: When the VCO frequency approaches 6 X the motor frequency (or where the motor frequency has decelerated to by coasting during the time the VCO frequency was ramping up) the back EMF loop can be closed by pulling pin 18 high and motor current brought up with I_{CMD} or I_{LIMIT}.

ADJUSTING OPEN LOOP STEP RATE

I_{RAMP} should be set so that the VCO's frequency ramp during "open loop stepping" phase of motor starting is less than the motor's acceleration rate. In other words, the motor must be able to keep up with the VCO's ramp rate in open loop stepping mode. The VCO's input voltage ($V_{PIN\ 20}$) ramp rate is given by:

$$\frac{dV_{VCO}}{dt} \approx \frac{I_{RAMP}}{C_1 + C_2}$$

since

$$F_{VCO} = K_{VCO} \times V_{VCO}$$

$$K_{VCO(MAX)} = \frac{4 \times 10^{-6}}{C_{VCO}}$$

then combining the 3 equations I_{RAMP} can be calculated from the desired maximum open loop stepping rate the motor can follow.

$$I_{RAMP} < \frac{dF_{VCO}}{dt} \frac{C_{VCO} \times (C_1 + C_2)}{4 \times 10^{-6}}$$

The motor will start more consistently and tolerate a wider variation in open loop step rate if there is some damping on the motor (such as head drag) during the open loop modes.

The tolerance of the open loop step VCO acceleration $\left(\frac{dF_{VCO}}{dt}\right)$ depends on the tolerances of K_{VCO}, I_{RAMP}, C1, C2, and C_{VCO}. For more optimum spin up times, these variables can be digitally "calibrated" out by the microprocessor using the following procedure:

1. Reset the IC by holding pin 16 low for at least 5µs.
2. Go into open loop step mode with no current on the motor and measure the difference between the first two complete VCO periods with the PWM signal at 50% duty cycle:

   ENABLE E/A = (see below)
   I_{CMD} = 0V
   PWM OUT = 50%

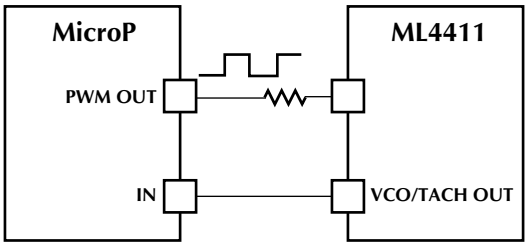


Figure 7. Auto-Calibration of Open-Loop Step Rate.

3. Compute a correction factor to adjust I_{RAMP} current by changing the PWM duty cycle from the Micro (D.C.)

$$D.C.(NEW) = 50\% \times \frac{\Delta F_{VCO}(DESIRED)}{\Delta F_{VCO}(MEASURED)}$$

4. Use new computed duty cycle for open loop stepping mode and proceed with a normal start-up sequence.

If this auto calibration is used ENABLE E/A can be tied permanently high, eliminating a line from the Micro. Since there is offset associated with the Phase Detector Error Amp (E/A), more current than is being injected by I_{RAMP} may be taken out of pin 20 if the offset is positive (into pin 20) if the error amp were enabled during the open loop stepping mode. In that case, V_{VCO} would not rise and the motor would not step properly. The effect of E/A offset can also be canceled out by the auto calibration algorithm described above allowing the E/A to be permanently enabled.

$$A_V = \frac{1.875 \times 10^{-4}}{sC_{OTA}}$$

PWM AND LINEAR CURRENT CONTROL

To facilitate speed control, the ML4411 includes two current control loops — linear and PWM (figure 9). The linear control loop senses the motor current on the I_{SENSE} terminal through R_{SENSE}. An internal current sense amplifier's (A2) output modulates the gates of the 3 N-channel MOSFET's when OTA OUT is tied to OTA IN, or can modulate a single MOSFET gate tied to OTA OUT. When operated in this mode, OTA IN is tied to 12V, and N1-N3 are saturated switches. This method produces the lowest current ripple at the expense of an extra MOSFET.

The linear current control modulates the gates of the external MOSFET drivers. Amplifier A2 is a transconductance amplifier which amplifies the difference between I_{CMD} and I_{SENSE}. The transconductance gain of A2 is:

$$g_m = 1.875 \times 10^{-4}\ \mho$$

The current loop is compensated by C_{OTA} which forms a pole given by

$$\omega_P = \frac{9.375 \times 10^{-4}}{C_{OTA}}$$

This time constant should be fast enough so that the current loop settles in less than 10% of T_{VCO} at the highest motor speed to avoid torque ripple to V_{TH} mismatch of the N-Channel MOSFETs.

The I_{SENSE} input pin should be kept below 1V. If I_{SENSE} goes above 1V, a bias current of about –300µA will flow out of pin 12 and the N outputs will be inhibited. Bringing I_{SENSE} below 0.7V removes the bias current to its normal level. For this reason, the noise filter resistor on the I_{SENSE} pin (1KΩ on Figure 10) should be less than 1.5KΩ.

The noise filter time constant should be great enough to filter the leading edge current spike when the N-FETs turn on but small enough to avoid excessive phase shift in the I_{SENSE} signal.

OUTPUT DRIVERS

The motor's source drivers (P1 thru P3) are open-collector NPN's with internal 16KΩ pull-up resistors. N3is inhibited until P3 is within 1.4V (typ) of V_{CC2} on the ML4411A.

Drivers N1 through N3 are totem-pole outputs capable of sourcing and sinking 10mA. Switching noise in the external MOSFETs can be reduced by adding resistance in series with the gates.

BRAKING

As shown in figure 9, the braking circuit pulls the N-Channel MOSFET gates high when BRAKE falls below a 1.4V threshold. After a power failure, C_{DLY} is discharged slowly through R_{DLY} providing a delay for retract to occur before the braking circuit is activated. The N-Channel buffer (B1) tri-states when the BRAKE pin reaches 2.1V to ensure that no charge from C_{BRK} is lost through the pull-down transistor in B1. To brake the motor with external signals, first disable power by pulling pin 8 low, then pull pin 26 below 1.4V using an open drain (or diode isolated) output.

The bias current for the Braking circuits comes from VCC2. When the N-Channel MOSFETs turn on, no additional power is generated for VCC2 (motor back-EMF rectified through out the MOSFET body diodes). After VCC2 drops below 4V, Q2 turns off. Continued braking relies on the C_{GS} of the N-Channel MOSFETs to sustain the MOSFET gate enhancement voltage.

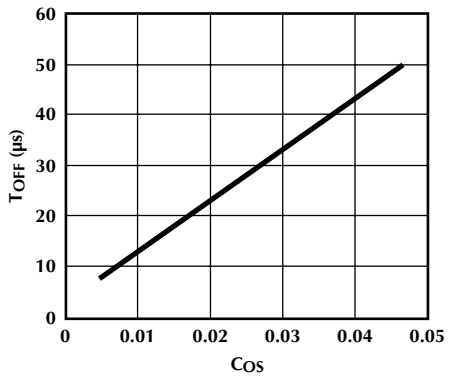


Figure 8. I_{LIMIT} Output Off-Time vs. C_{OS}.

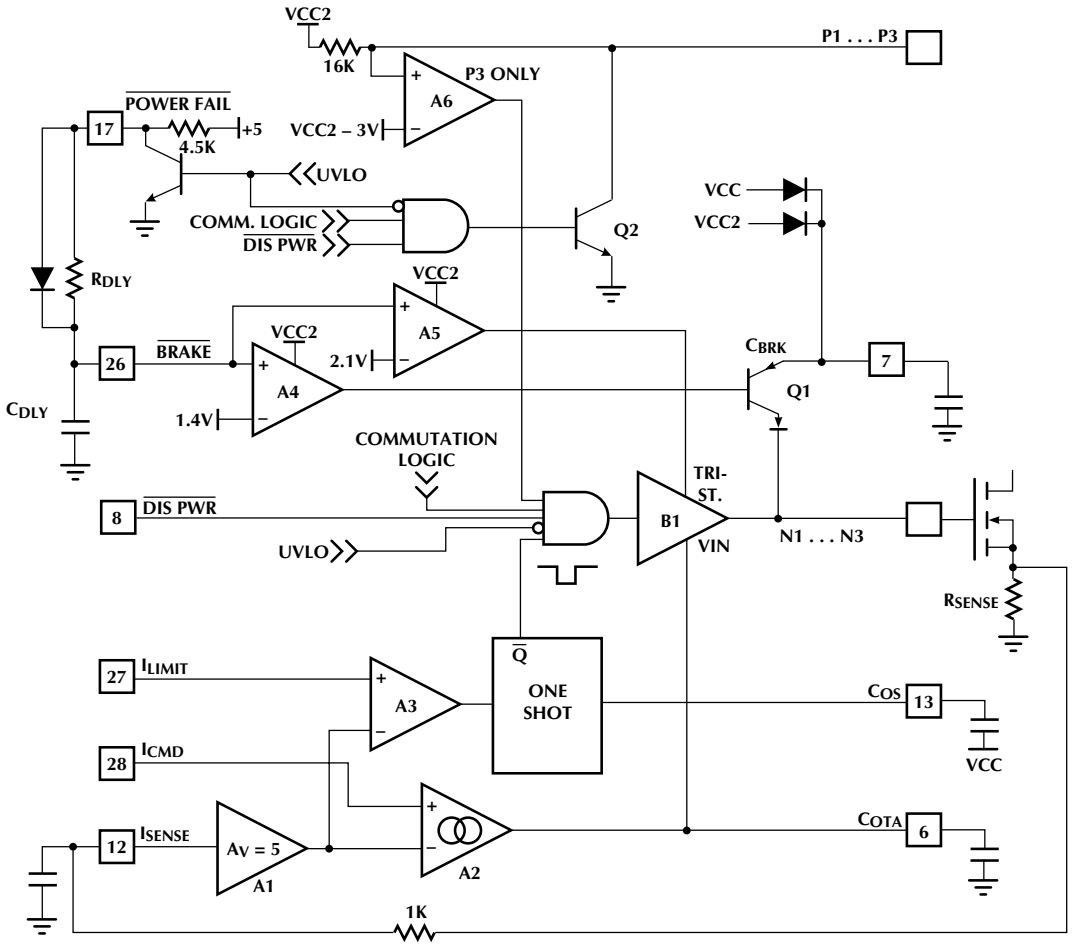


Figure 9. Current Control, Output Drive and Braking Circuits.

APPLICATIONS

Figure 10 shows a typical application of the ML4411 in a hard disk drive spindle control. Although the timing necessary to start the motor in most applications would be generated by a microcontroller, Fig. 11 shows a simple "one shot" start-up timing approach.

Speed control can be accomplished either by:

1. Sensing the VCO OUT frequency with a Microcontroller and adjusting I_{CMD} via an analog output form the Micro (PWM DAC).
2. Using analog circuitry for speed control. (Fig. 12).

OUTPUT STAGE HINTS

In the circuit in Figure 10, Q1, Q2, and Q3 are IRFR9024 or equivalent. Q4, Q5, and Q6 are IRFR024 or equivalent. New MOSFET packaging technology such as the Little Foot® series may decrease the PC board space. These packages, however have much lower thermal inertia and dissipation capabilities than the larger packages, and care should be taken not to exceed their rated current and junction temperature.

Since the output section in a full bridge application consists of three half-H switches, cross-conduction can occur. Cross-conduction is the condition where an N-FET and P-FET in the same phase of the bridge conduct simultaneously. This could happen under two conditions (see figure 13):

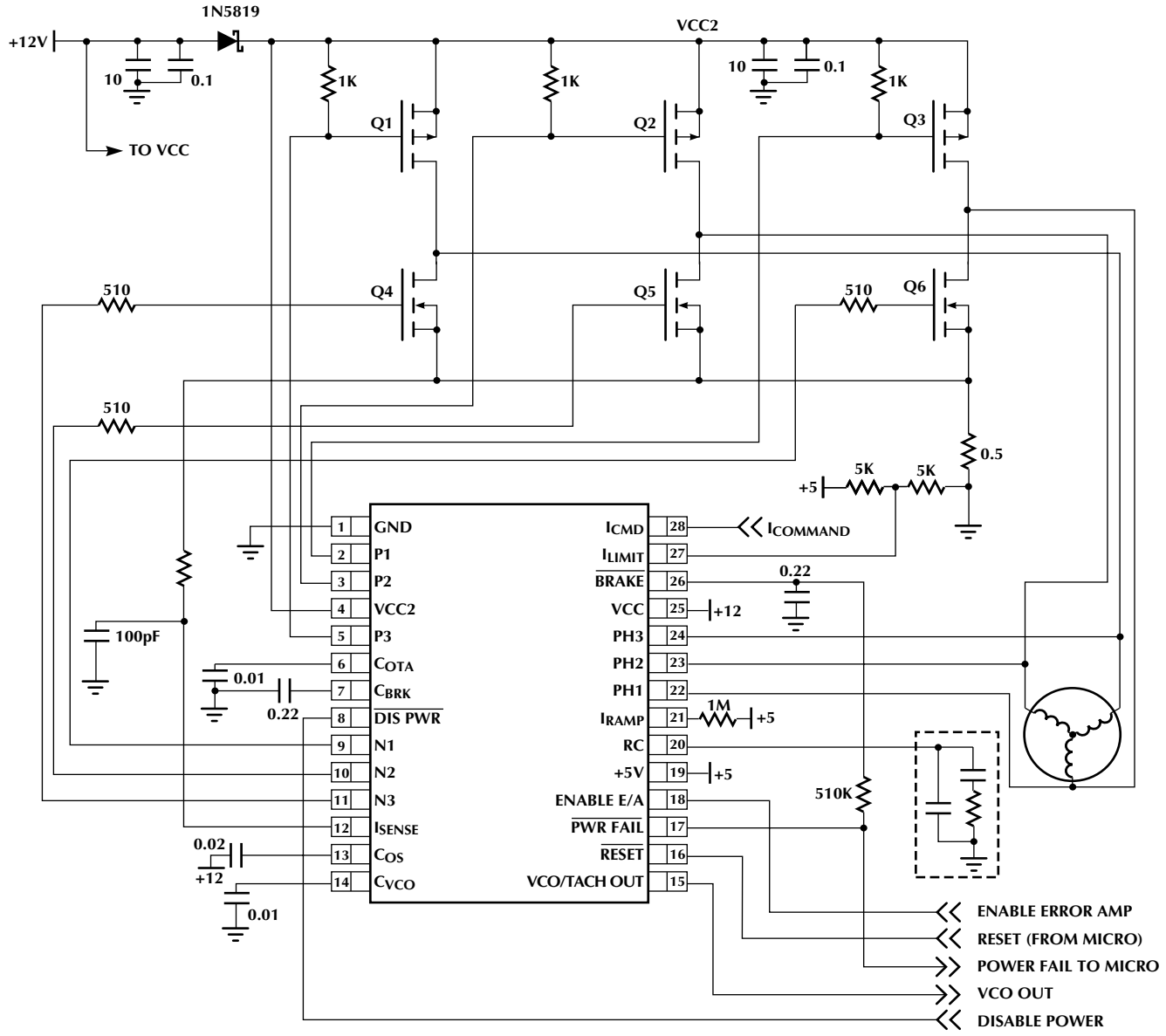


Figure 10. ML4411 Typical Application

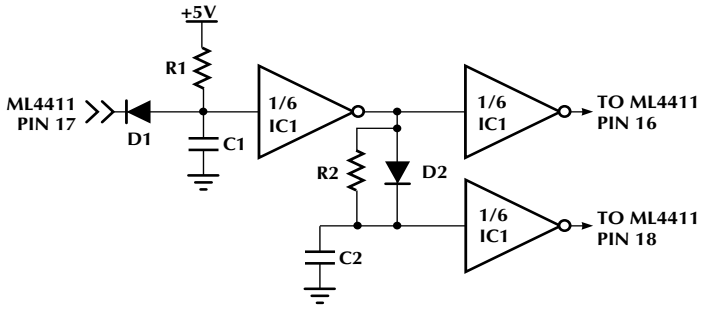
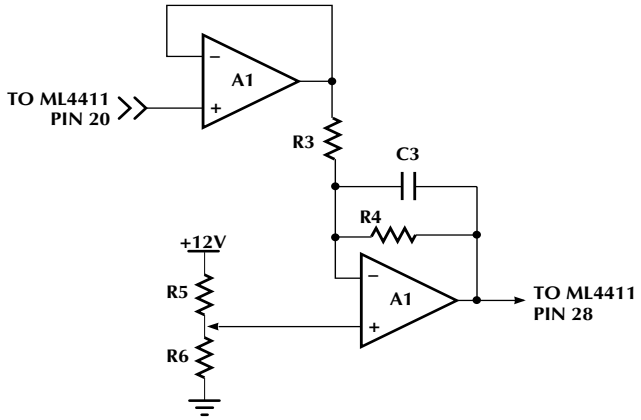


Figure 11. Analog Start-up Circuit



SYMBOL	VALUE
A1	LM358
IC1	74HC14
D1, D2	IN4148
R1	1MΩ
R2	1MΩ
R3	100KΩ

SYMBOL	VALUE
R4	100KΩ
R5	50KΩ
R6	50KΩ
C1	3.3µF
C2	3.3µF
C3	0.47µF

Figure 12. Analog Speed Control

1. When transitioning from mode 0 to mode A (see table 1) P3 goes from on to off at the same time N3 goes from off to on. If the P3 turns off slowly and N3 turns on quickly, cross-conduction may occur. This condition has been prevented inside the IC on the ML4411A through the addition of comparator A6 on the P3 output (Figure 9). This comparator may cause an oscillation when the N3 switches on due to the capacitive coupling effect described below pulling the P3 pin below VCC2-1.4V. To avoid this, use the circuit in Figure 13.
2. When the MOSFET in the same phase switches on gate current flows due to capacitive coupling of current through the MOSFET's drain to gate capacitance. This could cause the device that was off to be turned on.

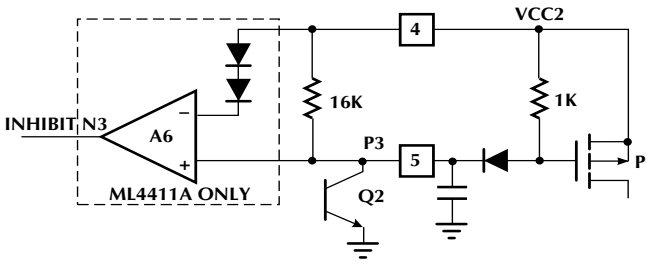


Figure 13. Alternate cross-conduction prevention for ML4411A

In Condition 2 above, the P-Channel MOSFET is pulled up inside the ML4411 with a 16KΩ resistor. If the current through C(CGp) is greater than V_{TH} ÷ 16K when the N-FET turns on, the P-FET could turn on simultaneously, causing cross-conduction. Adding R1 as shown in Figure 14 eliminates this. The size of R1 will depend on the fall time of the phase voltage, and the size of the C(DGp). D1 may be needed for high power applications to limit the negative current pulled (through C(DGn)) out of the substrate diode in the ML4411 when P-FET turns off.

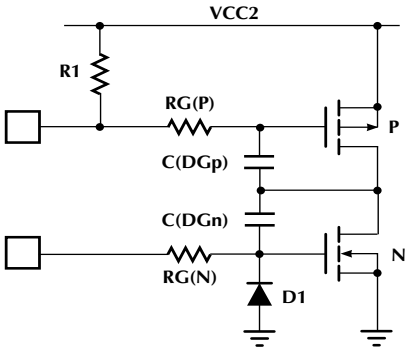


Figure 14. Causes of Cross-conduction

Adding a series damping resistor to the N-FET gate (RGn) will slow the fall time. The damping resistor should be low enough to:

Avoid turning on the N-Channel gate when the PNP turns on via the same mechanism outlined in condition 2 above

Not severely increase the switching losses in the N-FET

UNIPOLAR OPERATION

Unipolar mode offers the potential advantage of lower motor drive cost by only requiring the use of 3 transistors to drive the motor. The ML4411 will operate in unipolar mode (Figure 15) provided the following precautions are taken:

1. The IC supplies should not exceed 12V + 10%.
2. The phase pins on the IC should not exceed the supply voltage.

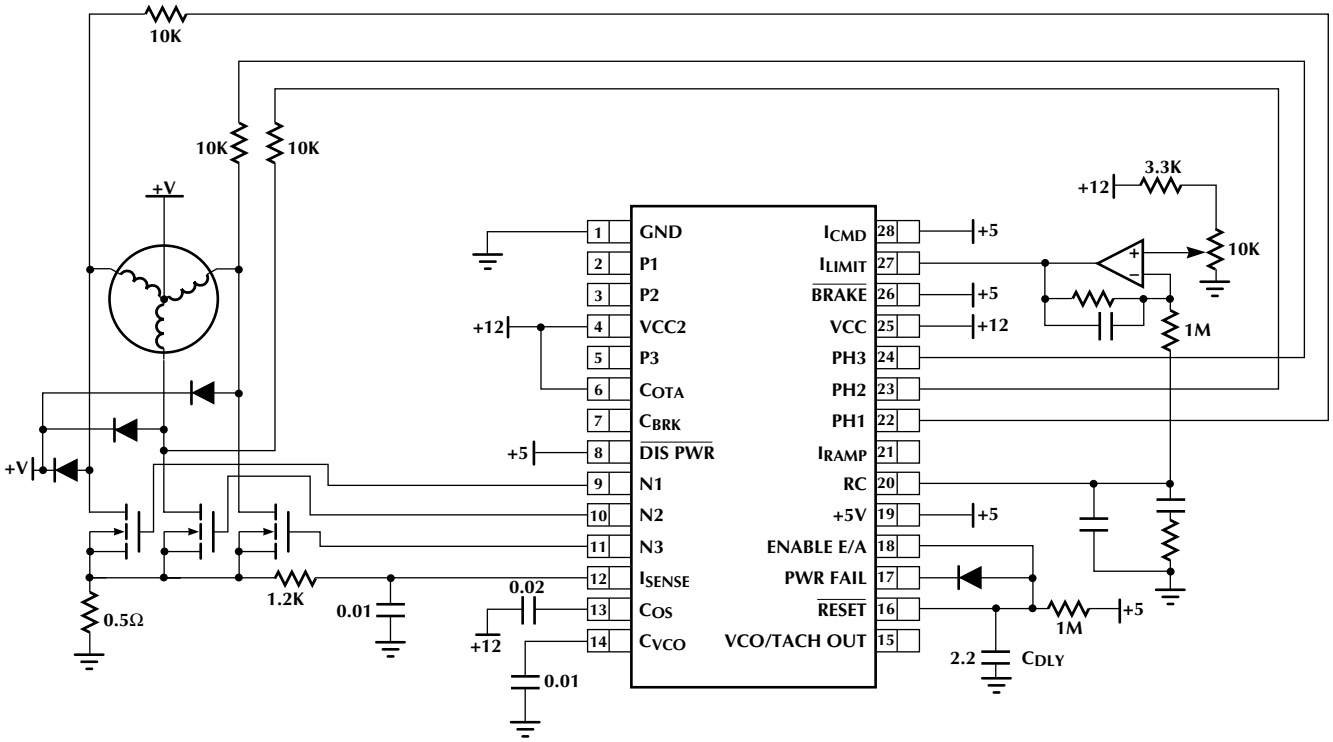


Figure 15. ML4411 Unipolar Drive Application

In unipolar operation, the motor's windings must be allowed to drive freely to:

$$V_{\Phi(MAX)} = V_{SUPPLY\ (MAX)} + V_{EMF\ (MAX)}$$

Therefore, there can be no diodes to clamp the inductive energy to V_{SUPPLY}. This energy must be clamped, however, to avoid an over-voltage condition on the MOSFETs and other components. Typically, a V_{CLAMP} voltage is created to provide the clamping voltage. The inductive energy may either be dissipated (Figure 16) or alternately efficiently regenerated back to the system supply (Figure 17).

The circuit in Figure 15 is designed to minimize the external components necessary, at some compromise to performance. The 3 resistors from the motor phase windings to the PH inputs work with the ML4411's 8KΩ internal resistance to ground to divide the motor's phase voltage down, providing input signals that do not exceed 12V.

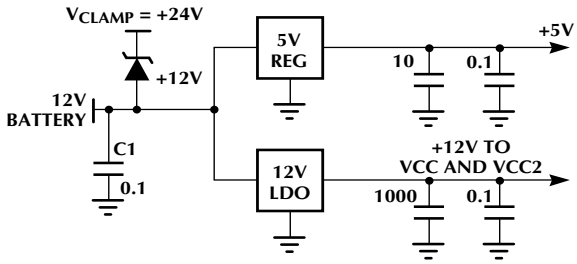


Figure 16. Dissipative Clamping Technique

This circuit uses analog speed regulation. The 1MΩ resistor from Pin 20 to the speed regulation op amp provides the function of injecting current into the VCO loop filter for the open loop stepping phase of start-up operation. The "one shot" circuitry to time the reset is replaced by a diode and RC delay from the rising edge or the $\overline{\text{POWERFAIL}}$ signal. The error amplifier is left enabled continuously since at low speeds its current contribution is negligible. The current injected into the loop filter must be greater than the leakage current from the phase detector amplifier for the motor to start reliably.

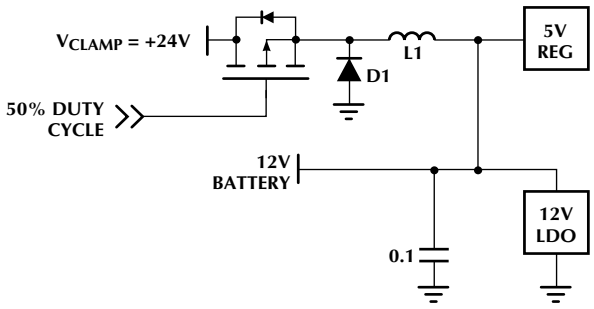


Figure 17. Non-Dissipative Clamping Technique

HIGHER VOLTAGE MOTOR DRIVE

To drive a higher voltage motor, the same precautions regarding ML4411 voltage limitations as were outlined for Unipolar drive above should be followed. Figures 14–16 provide several methods of translating the ML4411's P outputs to drive a higher voltage.

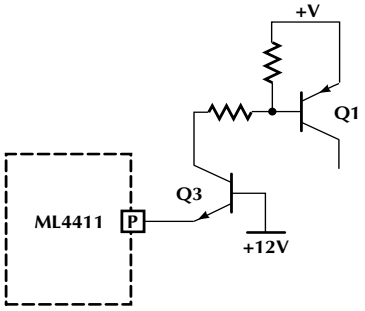


Figure 18. High Voltage Translation using PNP Power Transistor

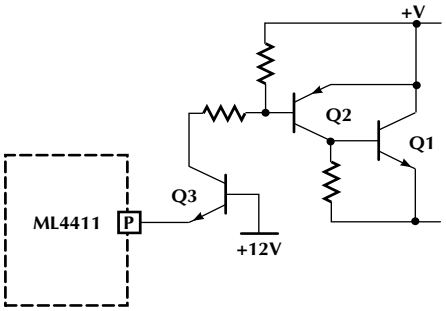


Figure 19. High Voltage Translation using "Composite" PNP Power Transistor

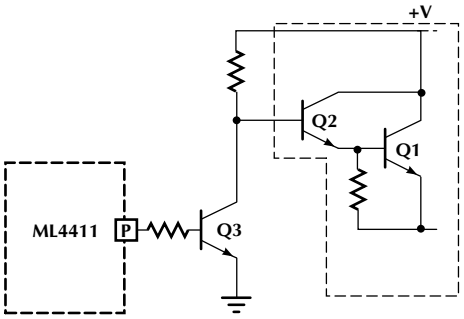
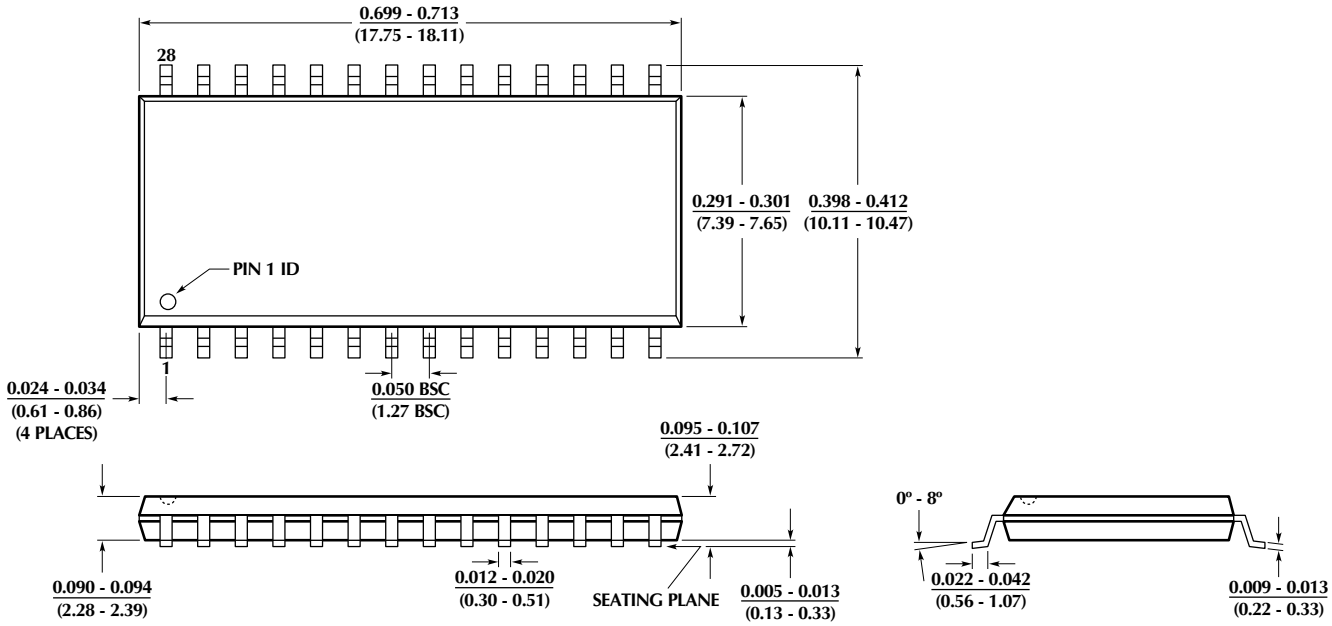


Figure 20. High Voltage Translation with NPN Darlington

PHYSICAL DIMENSIONS inches (millimeters)

Package: S28
28-Pin SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4411CS (Obsolete)	0°C to 70°C	28-Pin Wide SOIC (S28W)
ML4411ACS (End Of Life)	0°C to 70°C	28-Pin Wide SOIC (S28W)