HMU16/883

January 1994

16 x 16-Bit CMOS Parallel Multiplier

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **16 x 16-Bit Parallel Multiplier with Full 32-Bit Product**
- **High-Speed (45ns) Clocked Multiply Time**
- **Low Power CMOS Operation**
  - **I_{CCSB} = 500µA Maximum**
  - **I_{CCOP} = 7.0mA Maximum at 1MHz**
- **HMU16/883 is Compatible with the AM29516, LMU16, IDT7216, and the CY7C516**
- **Supports Two's Complement, Unsigned Magnitude and Mixed Mode Multiplication**
- **TTL Compatible Inputs/Outputs**
- **Three-State Outputs**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HMU16GM-45/883	-55°C to +125°C	68 Lead PGA
HMU16GM-60/883	-55°C to +125°C	68 Lead PGA

Description

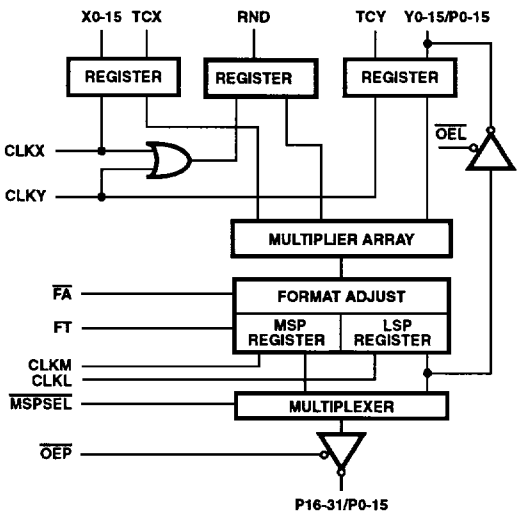
The HMU16/883 is a high speed, low power CMOS 16 x 16-bit parallel multiplier ideal for fast, real time digital signal processing applications. The 16-bit X and Y operands may be independently specified as either two's complement or unsigned magnitude format, thereby allowing mixed mode multiplication operations.

Additional inputs are provided to accommodate format adjustment and rounding of the 32-bit product. The Format Adjust control allows the user to select a 31-bit product with the sign bit replicated in the LSP. The Round control provides for rounding the most significant portion of the result by adding one to the most significant bit of the LSP.

Two 16-bit output registers (MSP and LSP) are provided to hold the most and least significant portions of the result, respectively. These registers may be made transparent for asynchronous operation through the use of the feedthrough control (FT). The two halves of the product may be routed to a single 16-bit three-state output port via the output multiplexer control, and in addition, the LSP is connected to the Y-input port through a separate three-state buffer.

The HMU16/883 utilizes independent clock signals (CLKX, CLKY, CLKL, CLKM) to latch the input operands and output product registers. This configuration maximizes throughput and simplifies bus interfacing. All outputs of the HMU16/883 also offer three-state control for multiplexing onto multiuse system busses.

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2804.2**

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input or Output Voltage Applied ..... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... 300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic PGA Package	42.69°C/W	10.0°C/W

Maximum Package Power Dissipation at +125°C
Ceramic PGA Package ..... 1.17 Watt
Gate Count ..... 4500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

TABLE 1. HMU16/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +4.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	+10	µA
Output or I/O Leakage Current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	+10	µA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 1.0MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.5V (Note 2)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	7.0	mA
Functional Test	FT	(Note 3)	7, 8	-55°C ≤ T_A ≤ +125°C	-	-	

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 5mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} (Clock Inputs) = 3.0, V_{IH} (All other inputs) = 2.6, V_{IL} = 0.4, $V_{OH} \geq$ 1.5V, and $V_{OL} \leq$ 1.5V.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. HMU16/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-45		-60		UNITS
					MIN	MAX	MIN	MAX	
Unclocked Multiply Time	T_{MUC}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	70	-	90	ns
Clocked Multiply Time	T_{MC}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	45	-	60	ns
X, Y, RND Setup Time	T_S		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	18	-	20	-	ns
Clock HIGH Pulse Width	T_{PWH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	20	-	ns
Clock LOW Pulse Width	T_{PWL}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	20	-	ns
MSPSEL to Product Out	T_{PDSEL}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	25	-	30	ns
Output Clock to P	T_{PDP}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	25	-	30	ns
Output Clock to Y	T_{PDY}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	25	-	30	ns
3-State Enable Time	T_{ENA}	(Note 2)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	25	-	30	ns
Clock Low Hold Time CLKXY Relative to CLKML	T_{HCL}	(Note 3)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns

NOTES:

1. AC Testing as follows: V_{CC} = 4.5V and 5.5V. Input levels 0V and 3.0V, Timing reference levels = 1.5V, Output load per test load circuit, with V_1 = 2.4V, R_1 = 500Ω and C_L = 40pF.
2. Transition is measured at ± 200 mV from steady state voltage, Output loading per test load circuit, with V_1 = 1.5V, R_1 = 500Ω and C_L = 40pF.
3. To ensure the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.

TABLE 3. HMU16/883 ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	-45		-60		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz All Measurements are referenced to device GND.	1	$T_A = +25^oC$	-	15	-	15	pF
Output Capacitance	C_{OUT}		1	$T_A = +25^oC$	-	10	-	10	pF
I/O Capacitance	$C_{I/O}$		1	$T_A = +25^oC$	-	10	-	10	pF
X, Y, RND Hold Time	T_H		1, 2	$-55^oC \leq T_A \leq +125^oC$	3	-	3	-	ns
3-State Disable Time	T_{DIS}		1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	25	-	30	ns
Output Rise Time	T_R	From 0.8V to 2.0V	1, 2, 4	$-55^oC \leq T_A \leq +125^oC$	-	10	-	10	ns
Output Fall Time	T_F	From 2.0V to 0.8V	1, 2, 4	$-55^oC \leq T_A \leq +125^oC$	-	10	-	10	ns

NOTES: 1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. Guaranteed, but not 100% tested.

3. Transition is measured at ±200mV from steady state voltage, Output loading per test load circuit, with V_1 = 1.5V, R_1 = 500Ω and C_L = 40pF.

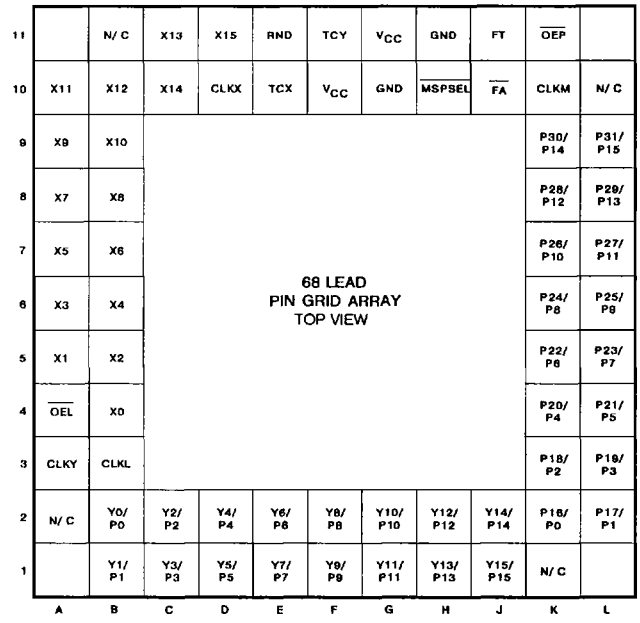
4. Loading is as specified in the test load circuit, with V_1 = 2.4V, R_1 = 500Ω and C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Burn-In Circuit



PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
B6	X4	F6	F1	Y9/P9	F11	K7	P10/P26	$V_{CC}/2$	E11	RND	F1
A6	X3	F5	G2	Y10/P10	F12	L7	P11/P27	$V_{CC}/2$	D10	CLKX	F0
B5	X2	F4	G1	Y11/P11	F13	K8	P12/P28	$V_{CC}/2$	D11	X15	F3
A5	X1	F3	H2	Y12/P12	F14	L8	P13/P29	$V_{CC}/2$	C10	X14	F2
B4	X0	F2	H1	Y13/P13	F15	K9	P14/P30	$V_{CC}/2$	C11	X13	F15
A4	OEL	V_{CC}	J2	Y14/P14	F4	L9	P15/P31	$V_{CC}/2$	B10	X12	F14
B3	CLKL	F0	J1	Y15/P15	F5	K10	CLKM	F0	A10	X11	F13
A3	CLKY	F0	K2	P0/P16	$V_{CC}/2$	K11	$\overline{OEP}$	F1	B9	X10	F12
B2	Y0/P0	F2	L2	P1/P17	$V_{CC}/2$	J10	$\overline{FA}$	F14	A9	X9	F11
B1	Y1/P1	F3	K3	P2/P18	$V_{CC}/2$	J11	FT	F15	B8	X8	F10
C2	Y2/P2	F4	L3	P3/P19	$V_{CC}/2$	H10	$\overline{MSPSEL}$	F14	A8	X7	F9
C1	Y3/P3	F5	K4	P4/P20	$V_{CC}/2$	H11	GND	GND	B7	X6	F8
D2	Y4/P4	F6	L4	P5/P21	$V_{CC}/2$	G10	GND	GND	A7	X5	F7
D1	Y5/P5	F7	K5	P6/P22	$V_{CC}/2$	G11	V_{CC}	V_{CC}	A2	N.C.	NONE
E2	Y6/P6	F8	L5	P7/P23	$V_{CC}/2$	F10	V_{CC}	V_{CC}	K1	N.C.	NONE
E1	Y7/P7	F9	K6	P8/P24	$V_{CC}/2$	F11	TCY	F15	L10	N.C.	NONE
F2	Y8/P8	F10	L6	P9/P25	$V_{CC}/2$	E10	TCX	F15	B11	N.C.	NONE

NOTES:

1. V_{CC} = 5.0V +0.5V/-0.0V with 0.1µF decoupling capacitor to GND.
2. F0 = 100kHz, F1 = F0/2, F2 = F1/2, ...
3. $V_{IH} = V_{CC} - 1V \pm 0.5V$ (Min), V_{IL} = 0.8V (Max)
4. 47kΩ load resistors used on all pins except V_{CC} and GND (Pin-Grid identifiers F10, G10, G11 and H11).

Die Characteristics

DIE DIMENSIONS:
179 x 169 x 19 ± 1mils

METALLIZATION:
Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY: $1.2 \times 10^5 A/cm^2$

Metallization Mask Layout

HMU16/883