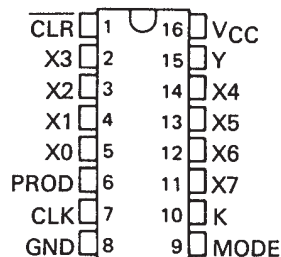


# SN54LS384, SN74LS384 8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

SDLS169 – JANUARY 1981 – REVISED MARCH 1988

- Two's-Complement Multiplication
- Magnitude Only Multiplication
- Cascadable for Any Number of Bits
- 8-Bit Parallel Multiplicand Data Input
- Serial Multiplier Data Input
- Serial Data Output for Multiplication Product
- 40 MHz Typical Maximum Clock Frequency

SN54LS384 . . . J PACKAGE  
SN74LS384 . . . N PACKAGE  
(TOP VIEW)



## description

The 'LS384 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's-complement form to produce a two's-complement product without external correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. These X latches are controlled via the clear input. When the clear input is low, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is high, the latches are closed and are insensitive to X input changes.

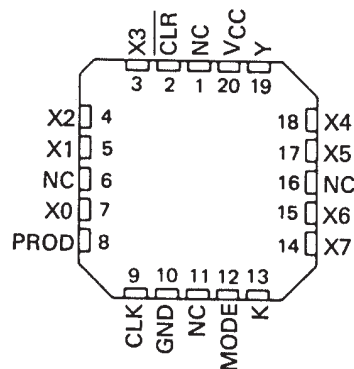
The multiplier word data is passed by the Y input in a serial bit stream, least significant bit first. The product is clocked out the PROD output, least significant bit first.

The multiplication of an m-bit multiplicand by an n-bit multiplier results in an (m + n)-bit product. The 'LS384 must be clocked for m + n clock cycles to produce this two's complement product. The n-bit multiplier (Y-input) sign bit data must be extended for the remaining m bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The PROD output of one device is connected to the K input of the succeeding device when cascading. The mode input is used to indicate which device contains the most significant bit. The mode input is wired high or low depending on the position of the 8-bit slice in the total X word length. The device with the most significant bit is wired low and all lower order bit packages are wired high.

The SN54LS384 will be characterized for operation over the full military temperature range from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS384 will be characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54LS384 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

# SN54LS384, SN74LS384

## 8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

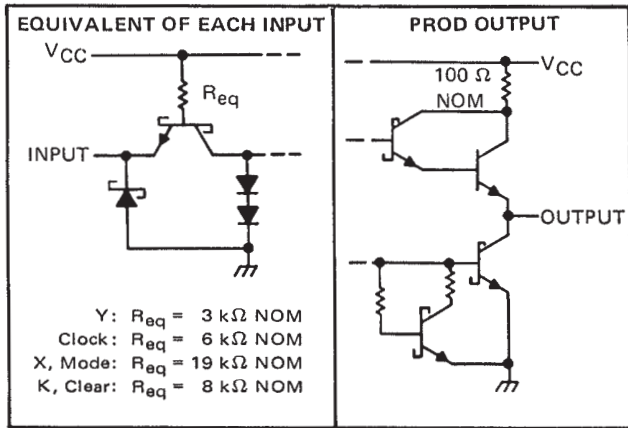
SDLS169 – JANUARY 1981 – REVISED MARCH 1988

FUNCTION TABLE

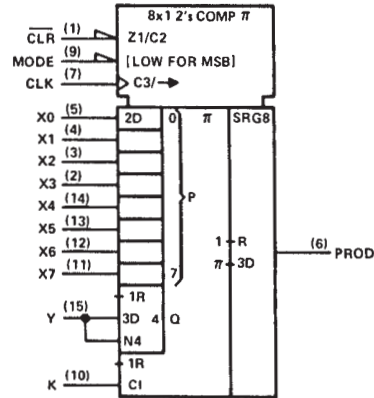
INPUTS				INTERNAL $Y_{-1}$	OUTPUT PROD	FUNCTION
CLR	CLK	$X_i$	Y			
L	X	Data	X	L	L	Load new multiplicand and clear internal sum and carry registers
H	↑	X	L	L	Output per	Shift sum register
H	↑	X	L	H		Add multiplicand to sum register and shift
H	↑	X	H	L	Booth's algorithm	Subtract multiplicand from sum register and shift
H	↑	X	H	H		Shift sum register

H = high-level, L = low-level, X = irrelevant, ↑ = low-to-high-level transition

### schematics of inputs and outputs



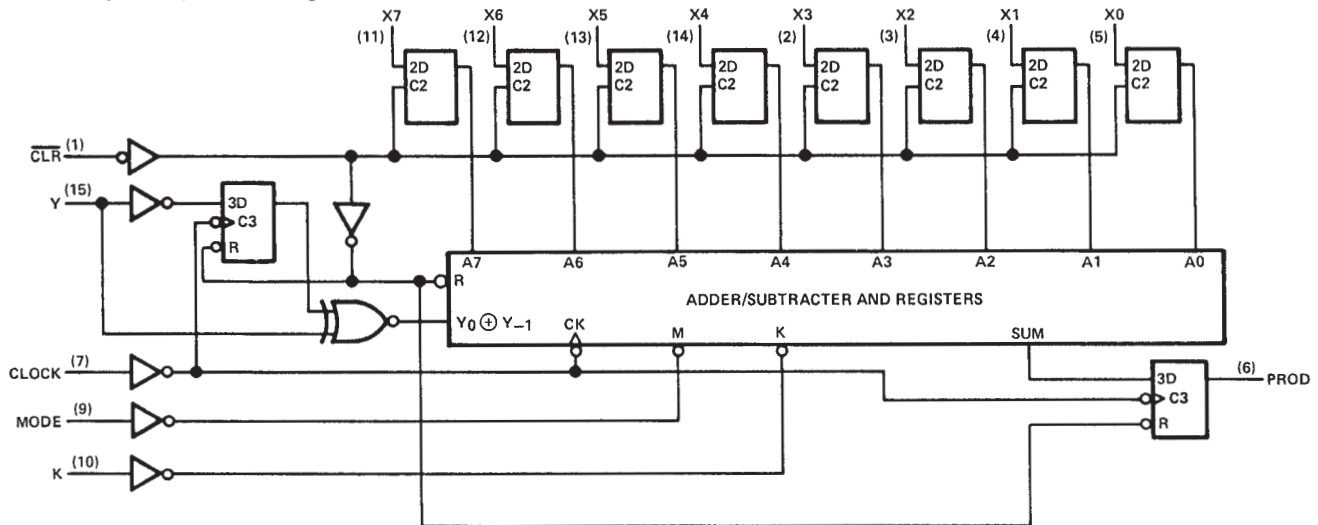
### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J and N packages.

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54LS384	-55°C to 125°C
SN74LS384	0°C to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values are with respect to network ground terminal.  
2. Input voltages must be zero or positive with respect to network ground terminal.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54LS384, SN74LS384

## 8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

SDLS169 – JANUARY 1981 – REVISED MARCH 1988

### recommended operating conditions

		SN54LS384			SN74LS384			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$					-400			$\mu A$
Low-level output current, $I_{OL}$					8			mA
Clock frequency, $f_{clock}$		0	25		0	25		MHz
Setup time, $t_{su}$		Y before Clock $\uparrow$		45		38		ns
		K before Clock $\uparrow$		30		24		
		X before Clear $\uparrow$		23		19		
Clear inactive-state set up time before Clock $\uparrow$		30			20			ns
Hold time, $t_h$		Y after Clock $\uparrow$		0		0		
		K after Clock $\uparrow$		0		0		
		X after Clear $\uparrow$		2		2		
Pulse width, $t_w$		Clock high		20		20		ns
		Clock low		20		20		
		Clear low		38		33		
Operating free-air temperature, $T_A$		-55		125		0		$^{\circ}C$

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>†</sup>	SN54LS384			SN74LS384			UNIT	
			MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX		
$V_{IH}$	High-level input voltage		2			2			V	
$V_{IL}$	Low-level input voltage		0.7			0.8			V	
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5			-1.5			V	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = -400 \mu A$	2.5	3.4		2.7	3.4		V	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	0.25		0.4	0.25		0.4	V	
		$I_{OL} = 4 \text{ mA}$				0.35		0.5		
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1			1			mA	
$I_{IH}$	High-level input current	X, Mode K, Clear Clock Y $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	20			20			$\mu A$	
			30			30				
			40			40				
			80			80				
$I_{IL}$	Low-level input current	X, Mode K, Clear Clock Y $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-0.48			-0.48			mA	
			-1.2			-1.2				
			-1.6			-1.6				
			-3.2			-3.2				
$I_{OS}$	Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$	-20	-100	-20	-100		mA		
$I_{CC}$	Supply current	$V_{CC} = \text{MAX},$ See Note 3	91		132		91		132	mA

<sup>†</sup>For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$ .

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3:  $I_{CC}$  is measured with the clear input grounded and all other inputs and outputs open.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$	Maximum clock frequency		25	40		MHz
$t_{PLH}$	Propagation delay time, low-to-high-level output from clock	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega,$ See Note 4	15		23	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from clock		15		23	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from clear		17		25	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



# SN54LS384, SN74LS384

## 8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

SDLS169 – JANUARY 1981 – REVISED MARCH 1988

### TYPICAL APPLICATION DATA

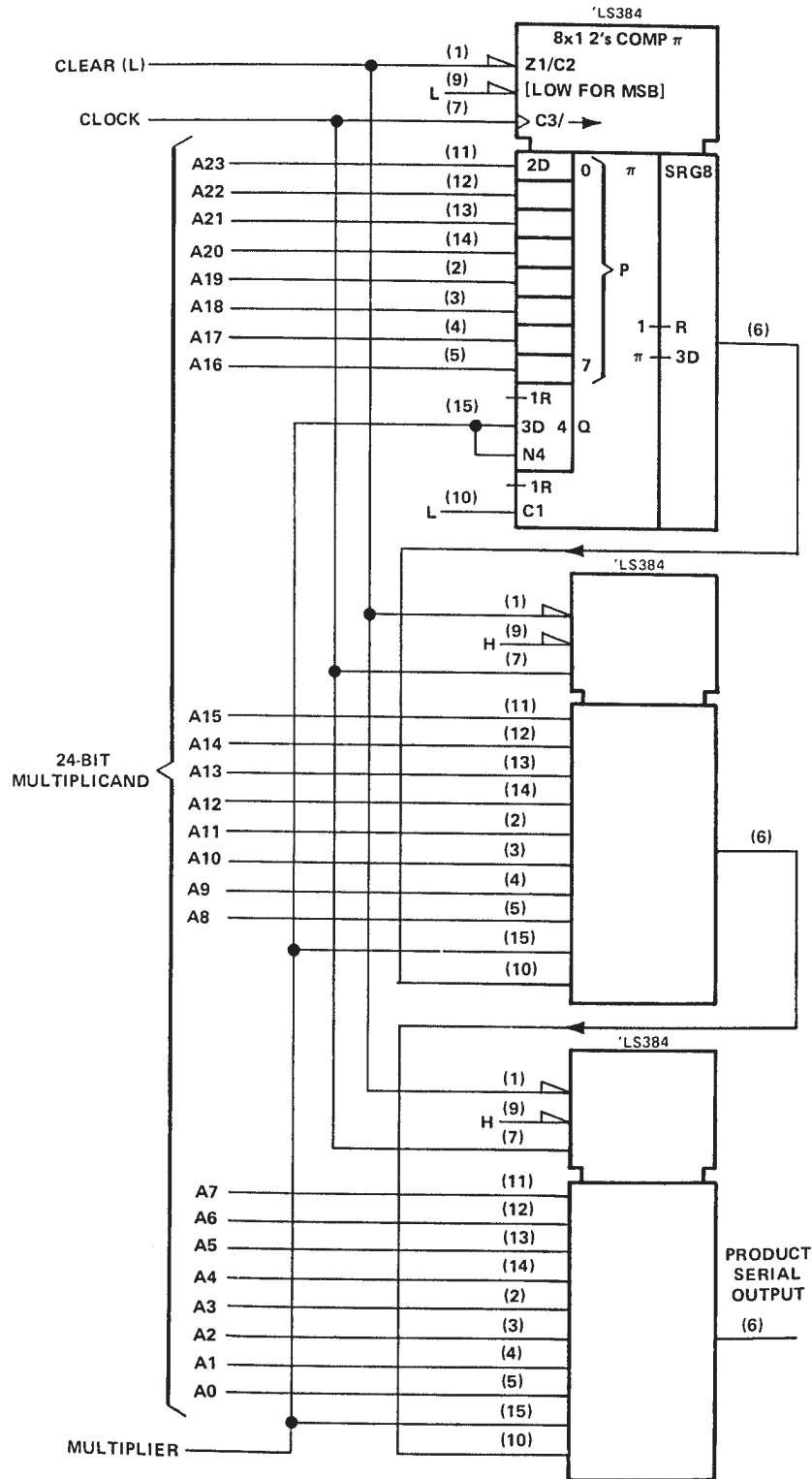


FIGURE 1—BASIC 24-BIT SERIAL/PARALLEL CONNECTION



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54LS384, SN74LS384

## 8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

SDLS169 – JANUARY 1981 – REVISED MARCH 1988

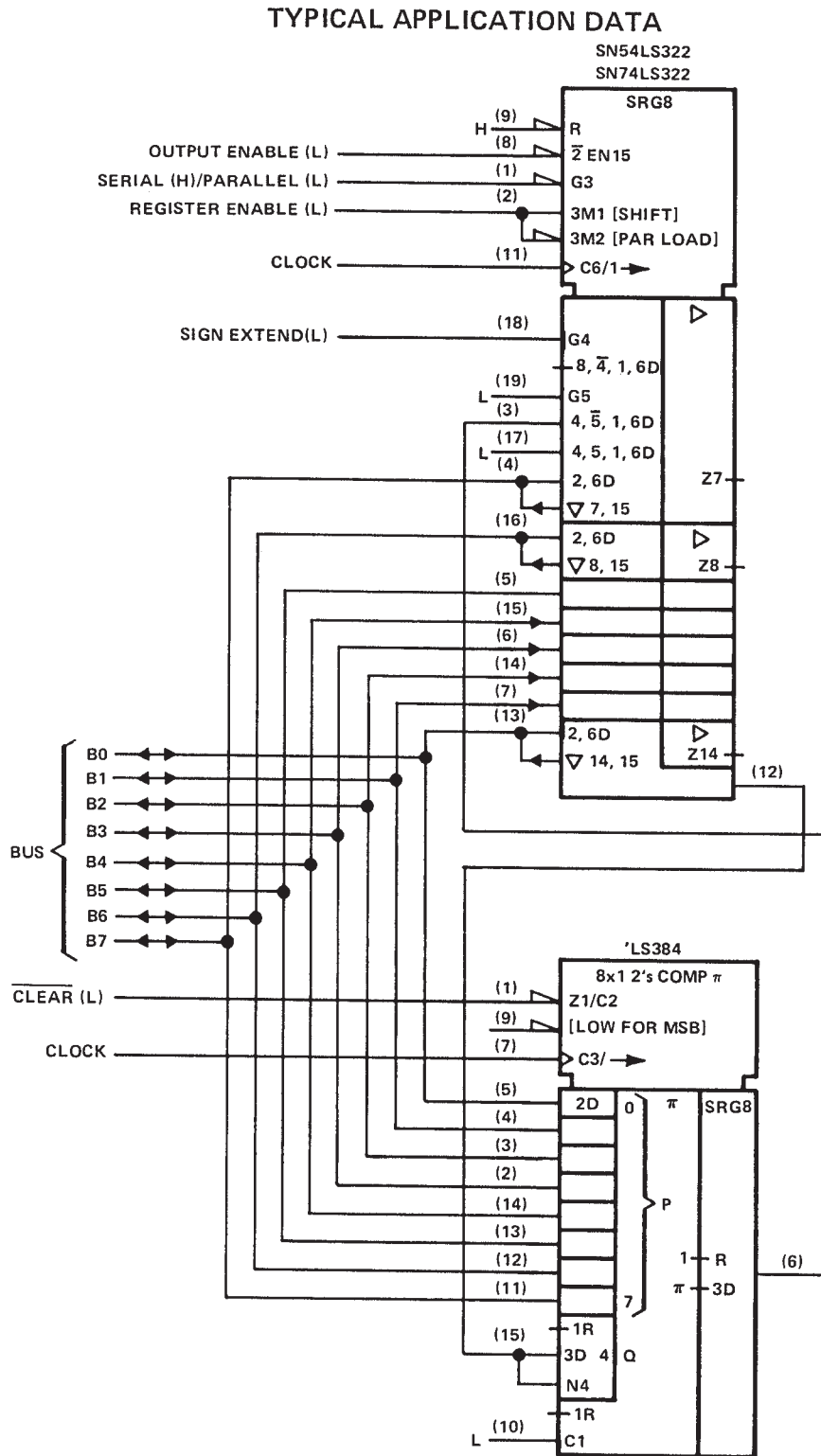


FIGURE 2—8-BIT BY 8-BIT MULTIPLIER, BUS ORGANIZED,  
WITH 8-BIT TRUNCATED PRODUCT

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.