STANDARD MICROSYSTEMS CORPORATION

SR 5015-XXX

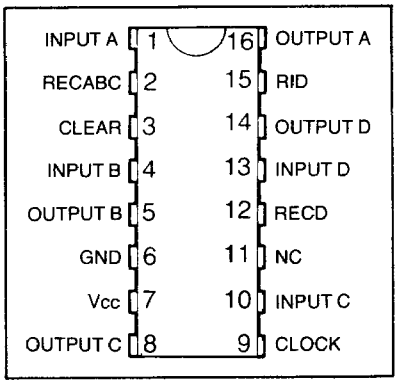
SR 5015-80
SR 5015-81
SR 5015-133

Quad Static Shift Register

FEATURES

- ☐ COPLAMOS® N Channel Silicon Gate Technology
- ☐ Variable Length—Single Mask Programmable—1 to 134 bits
- ☐ Directly TTL-compatible on all inputs, outputs, and clock
- ☐ Clear function
- ☐ Operation guaranteed from DC to 1.0 MHz
- ☐ Recirculate logic on-chip
- ☐ Single +5.0V power supply
- ☐ Low clock input capacitance
- ☐ 16 pin ceramic DIP Package
- ☐ Pin for Pin replacement for AMI S2182, 83, 85

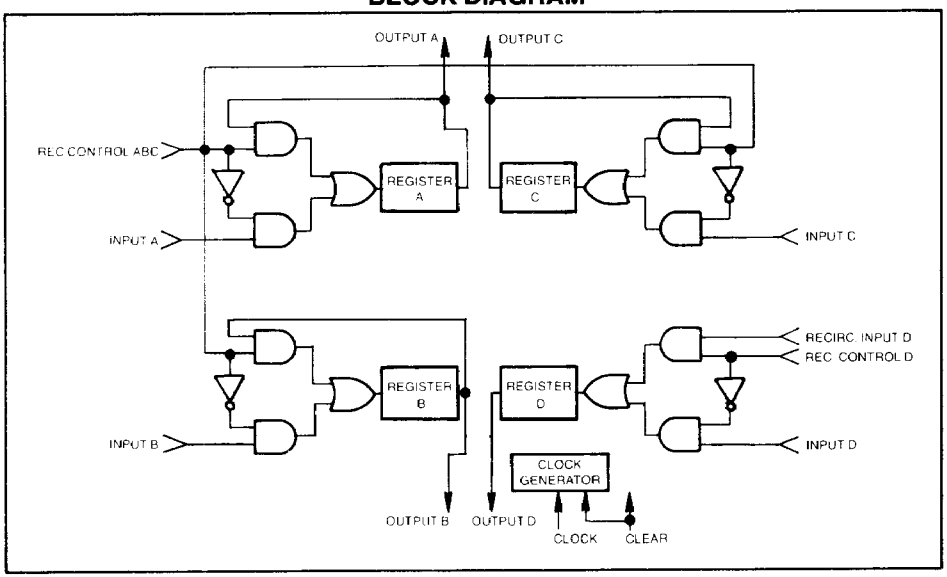
PIN CONFIGURATION



APPLICATIONS

- ☐ Memory Buffering
- ☐ Unique Buffering Lengths
- ☐ Terminals

BLOCK DIAGRAM



SECTION VIII

General Description

The SMC SR 5015-XXX is a quad static shift register family fabricated using SMC's COPLAMOS® N channel silicon gate process which provides a higher functional density and speed on a monolithic chip than conventional MOS technology. The COPLAMOS® process provides high speed operation, low power dissipation, low clock input capacitance, and single +5 volt power supply operation.

These shift registers can be driven by either T^2L circuits or by MOS circuits and provide driving capability to MOS or T^2L circuits. This device consists of four separate static shift registers with independent input and output terminals and logic for loading, recirculating or shifting information. The SR 5015-80, SR 5015-81, and SR 5015-133 are respectively 80, 81, and 133 bit quad shift registers.

The recirculate control pin is common for registers A, B, and C. Register D has an independent recirculate control pin as well as a recirculate input pin.

A clear pin has been provided that will cause the shift register to be cleared when the pin is at V_{CC}. A single T^2L clock is required for operation.

The transfer of data into the register is accomplished on the low-to-high transition of the clock with the recirculate control low. For long term data storage the clock may be stopped and held in either logic state. Recirculate occurs when the recirculate control is high. Output data appears on the low-to-high transition of the clock pulse.

Bits 81 and 133 are available for flag storage.

This device has been designed to be used in high speed buffer storage systems and small recirculating memories.

Special custom configurations are achieved via single mask programming in lengths of 1 to 134 bits.

MAXIMUM GUARANTEED RATINGS*

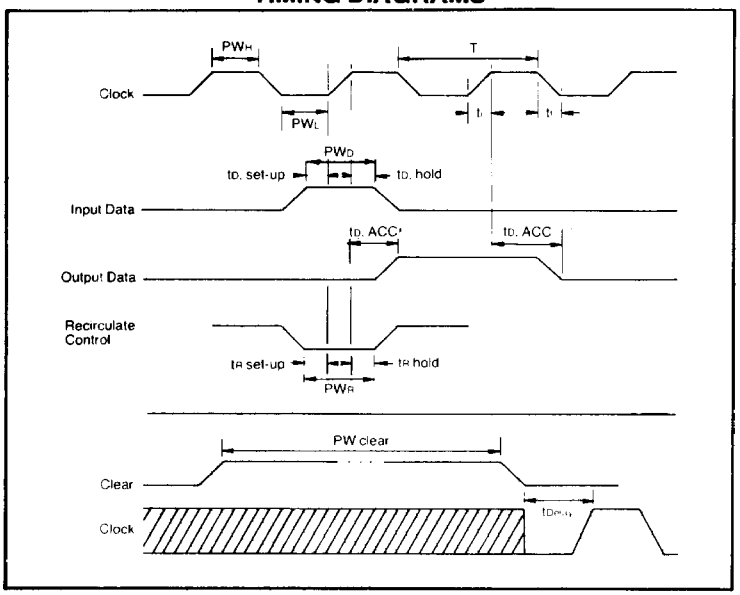
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+8.0V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}= +5V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. Characteristics					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC}−1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level, V_{OL}			0.4	V	I_{OL}=1.6ma
High Level, V_{OH}	V_{CC}−1.5	4.0		V	I_{OH}=100μa
INPUT LEAKAGE CURRENT			1.0	μa	V_{IN}=V_{CC}
CLOCK, CLEAR			25	pf	
All Other			10	pf	
POWER SUPPLY CURRENT			80	ma	
A.C. Characteristics					T_A= +25°C
CLOCK					
PW_H	300			ns	
PW_L	600			ns	
Transition, t_r, t_f		0.02	1.0	μs	
Repetition Rate, 1/T	0		1.0	MHz	
t_1 Delay	300			ns	
INPUT DATA					
t_D, set-up	100			ns	
t_D, hold	200			ns	
PW_D	300			ns	
OUTPUT DATA					
t_D, ACC		200	350	ns	
RECIRCULATE CONTROL					
t_R, set-up	200			ns	
t_R, hold	300			ns	
PW_R	500			ns	
CLEAR					
PW_{CLEAR}	20			μs	

TIMING DIAGRAMS

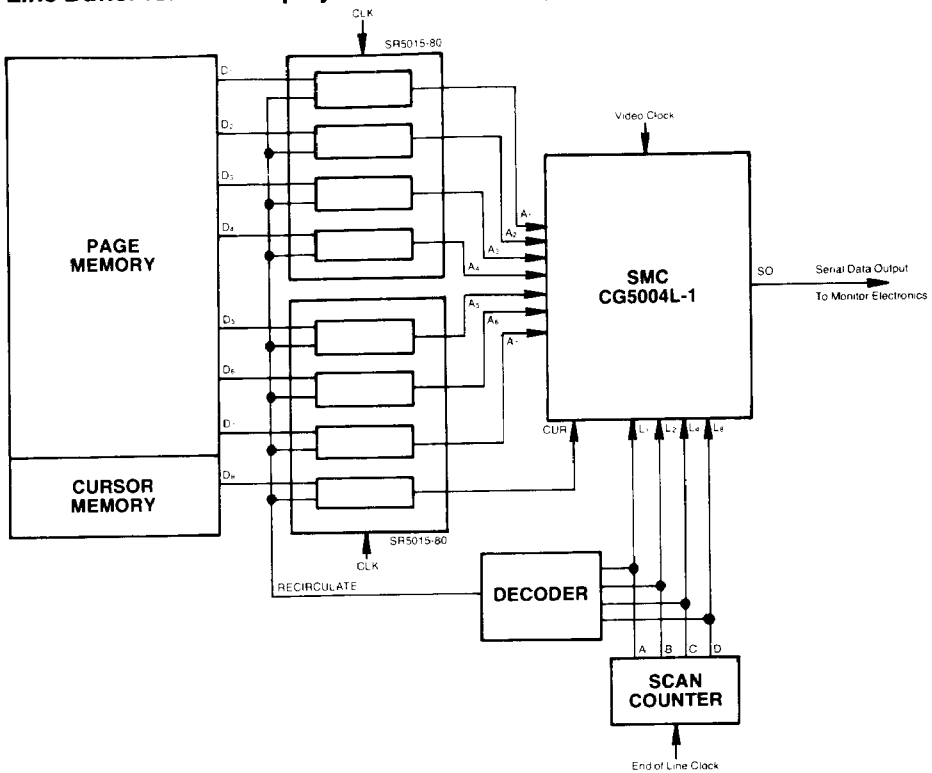


Description of Pin Functions

Pin No.	Symbol	Name	Function
1	A	Input A	Input signal which is either high or low depending on what word is to be loaded into shift register.
2	RECABC	Recirculate ABC	Input signal when high disconnects inputs from registers and connects outputs to inputs, thus recirculating data. Recirculates only A, B, C outputs.
3	CLR	Clear	Input signal when high forces outputs to a low state immediately and clears all the registers.
4	B	Input B	Input signal for B register.
5	O_B	Output B	Output signal for B register.
6	GND	GND	Power supply Ground.
7	V_{CC}	+5 Volt	5 volt power supply.
8	O_C	Output C	Output signal for C register.
9	CLK	Clock Input	Input signal which is normally low and pulses high to shift data into the registers. The data is clocked in on low to high edge of clock.
10	C	Input C	Input signal for C register.
11	NC	NC	
12	RECD	Recirculate Control D	Input signal which is normally low and, when goes high, disconnects Input D to register and connects Recirculate Input D to register.
13	D	Input D	Input signal for D register.
14	O_D	Output D	Output signal for D register.
15	RID	Recirculate Input D	Input signal which is the input to the D register when Recirculate Control D is high: RECD=1.
16	O_A	Output A	Output signal for A register.

APPLICATIONS

Line Buffer for CRT Display . . . 80 Characters per line.



Line Buffer for Matrix Printer . . . 132 Characters per line.