HARRIS

BUZ71

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 14A, 50V
- $r_{DS(on)} = 0.1\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

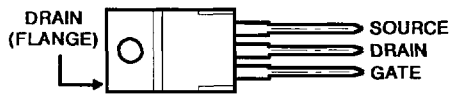
Description

The BUZ71 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ71 is supplied in the JEDEC TO-220AB plastic package.

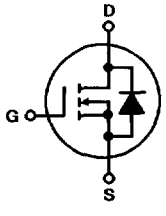
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ71	UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	50	V
Continuous Drain Current, T_C = +55°C	I_D	14	A
Pulsed Drain Current, T_C = +25°C	I_{DM}	56	A
Single Pulse Avalanche Energy*, EAS		100	mj
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation, T_C = +25°C	P_D	40	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

*V_{DD} = 10V, starting T_j = 25°C, L = 820μHy, I_{peak} = 14A, see Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number 2418

ELECTRICAL CHARACTERISTICS At Case Temperature (T_C) = +25°C Unless Otherwise Specified.

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	VGS = 0 V ID = 0.25 mA	50	-	-	V
Gate-Threshold Voltage	VGS(th)	VDS = VGS ID = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	IDSS	Tj = 25°C Tj = 125°C VDS = 50 V, VGS = 0 V	- -	20 100	250 1000	µA
Gate-Source Leakage Current	IGSS	VGS = 20 V VDS = 0 V	-	10	100	nA
Drain-Source on Resistance	rDS(on)	VGS = 10 V ID = 9A	-	0.09	0.1	Ω
Forward Transconductance	gfs	VDS = 25 V ID = 9 A	3.0	5.2	-	S
Input Capacitance	Ciss	VGS = 0 V	-	480	650	pF
Output Capacitance	Coss	VDS = 25 V	-	280	450	
Reverse Transfer Capacitance	Crss	f = 1 MHZ	-	160	280	
Turn-On Time ton	td(on)	Vcc = 30 V	-	20	30	ns
(ton = td(on) + tr)	tr	ID = 3 A	-	55	85	
Turn-Off Time toff	td(off)	VGS = 10 V	-	70	90	
(toff = td(off) = tr)	tr	RGS = 50 Ω	-	80	110	
Thermal Resistance, Junction-to-Case	RθJC			≤3.1		°C/W
Thermal Resistance, Junction-to-Ambient	RθJA			≤75		

*VDD = 10 V, starting Tj = 25°C, L = 820 µHy, Ipeak = 14 A, see figure 14 & 15.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	IDR	Tc = 25°C	-	-	14	A
Pulsed Reverse Drain Current	IDRM		-	-	56	
Diode Forward Voltage	VSD	IF = 2 x IDR VGS = 0 V, Tj = 25°C	-	1.6	1.8	V
Reverse Recovery Time	trr	Tj = 25°C, IF = IDR	-	120	-	ns
Reverse Recovered Charge	QRR	dIF/dt = 100 A/µs, VR = 30 V	-	0.15	-	µC

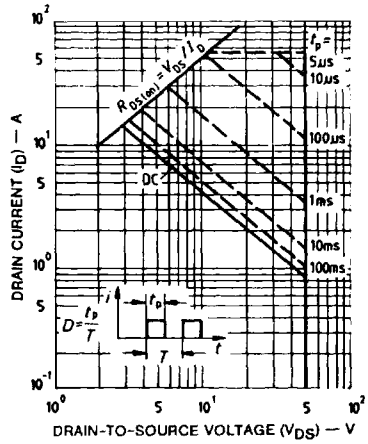


Figure 1 - Maximum safe operating areas for all types.

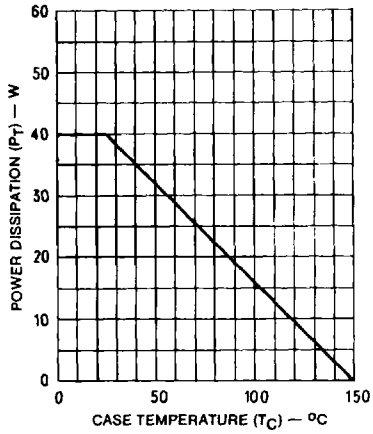


Figure 2 - Power vs temperature derating curve for all types.

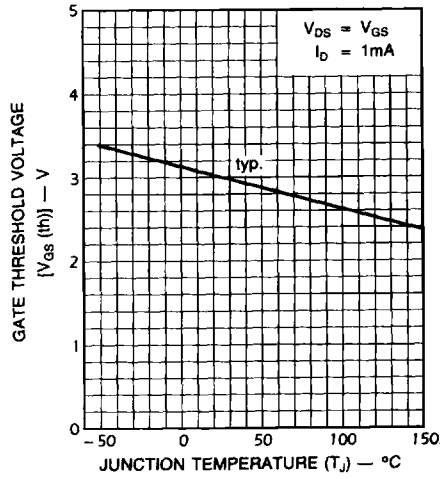


Figure 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

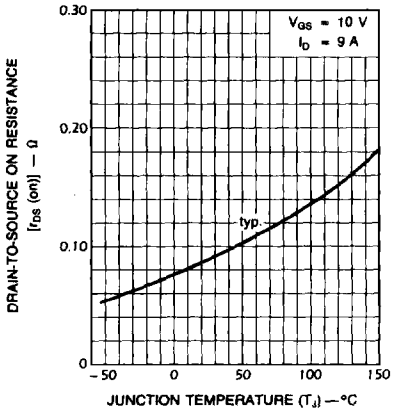


Figure 4 - Normalized drain-to-source on resistance to junction temperature for all types.

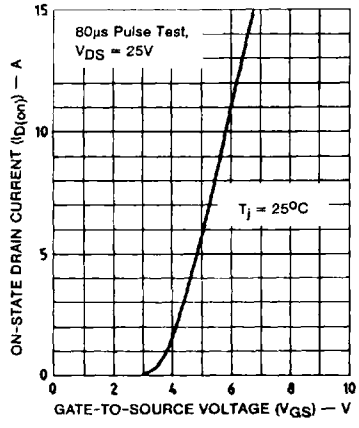


Figure 5 - Typical transfer characteristics for all types.

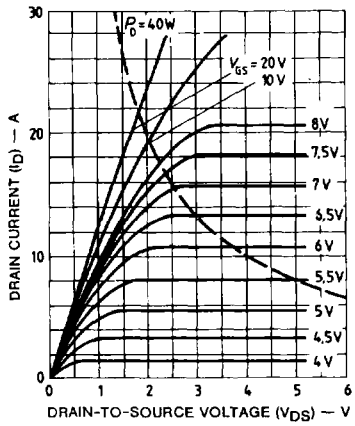


Figure 6 - Typical output characteristics.

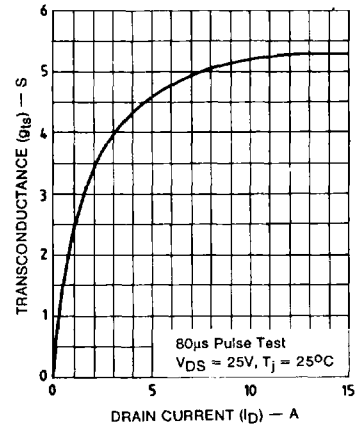


Figure 7 - Typical transconductance vs drain current.

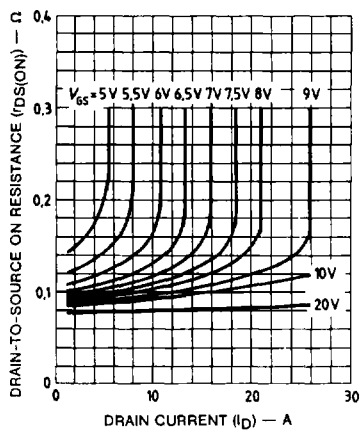


Figure 8 - Typical on-resistance vs drain current.

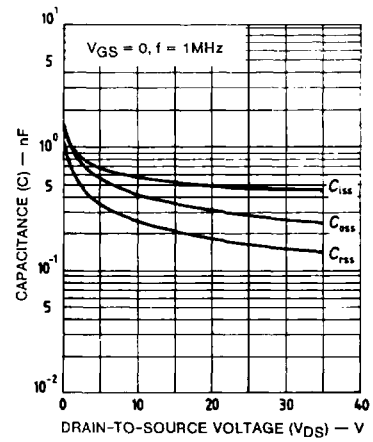


Figure 9 - Typical capacitance vs drain-to-source voltage.

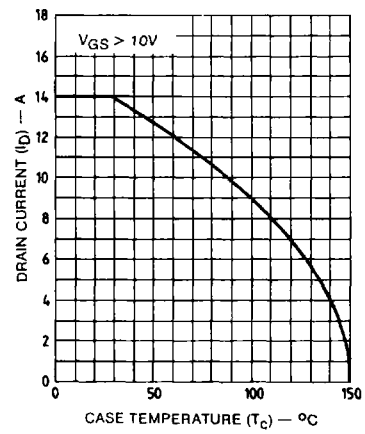


Figure 10 - Maximum drain current vs case temperature.

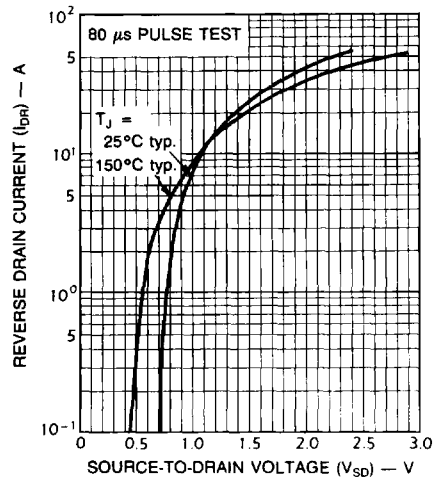


Figure 11 - Typical source-drain diode forward voltage.

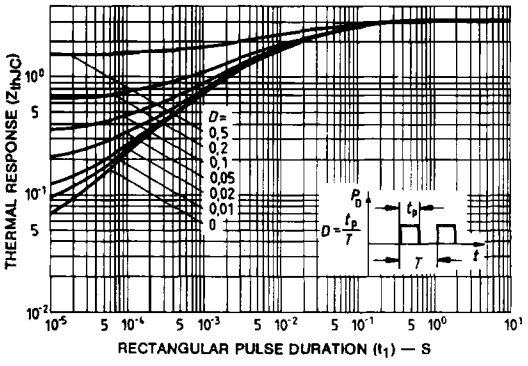


Figure 12 – Maximum effective transient thermal impedance, junction-to-case vs pulse duration

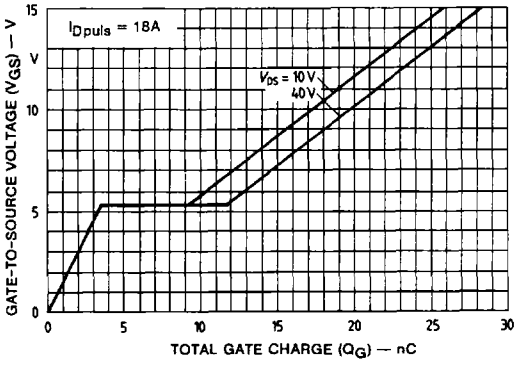


Figure 13 – Typical gate charge vs gate-to-source voltage.

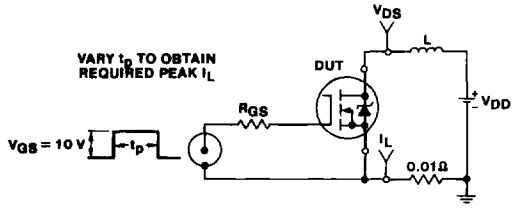


Figure 14 – Unclamped energy test circuit.

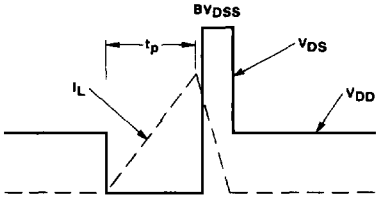


Figure 15 – Unclamped energy test waveforms.