TVS Diode

Transient Voltage Suppressor Diodes

ESD3V3XU1U Series

Uni-directional Ultra Low Capacitance ESD / Transient Protection Diode

ESD3V3XU1UL
ESD3V3XU1US

Data Sheet

Revision 1.1, 2011-10-19
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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.1, 2011-10-19 Table3-2; Table3-4; Figure3-4 updated	
Revision 1.0	**2011.09.07**

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Last Trademarks Update 2010-10-26

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1 Uni-directional Ultra Low Capacitance ESD / Transient Protection Diode

1.1 Features

- ESD / transient protection of high speed data lines exceeding:
  - IEC61000-4-2 (ESD): ±20 kV (air / contact)
  - IEC61000-4-4 (EFT): 2.5 kV / 50 A (5/50 ns)
  - IEC61000-4-5 (surge): 3 A (8/20 µs)
- Maximum working voltage: V_{RWM} = 3.3 V
- Ultra low capacitance C_L = 0.4 pF (typical)
- Very low clamping voltage: V_{CL}= 8 V at I_{PP} = 16 A (typical) [2]
- Very low dynamic resistance: R_{DYN} = 0.19 Ω (typical) [2]
- Pb-free and halogen-free package (RoHS compliant)

1.2 Application Examples

- USB 3.0, 10/100/1000 Ethernet, Firewire, DVI, HDMI, S-ATA, DisplayPort
- Mobile HDMI Link, MDDI, MIPI, SWP / NFC

2 Product Description

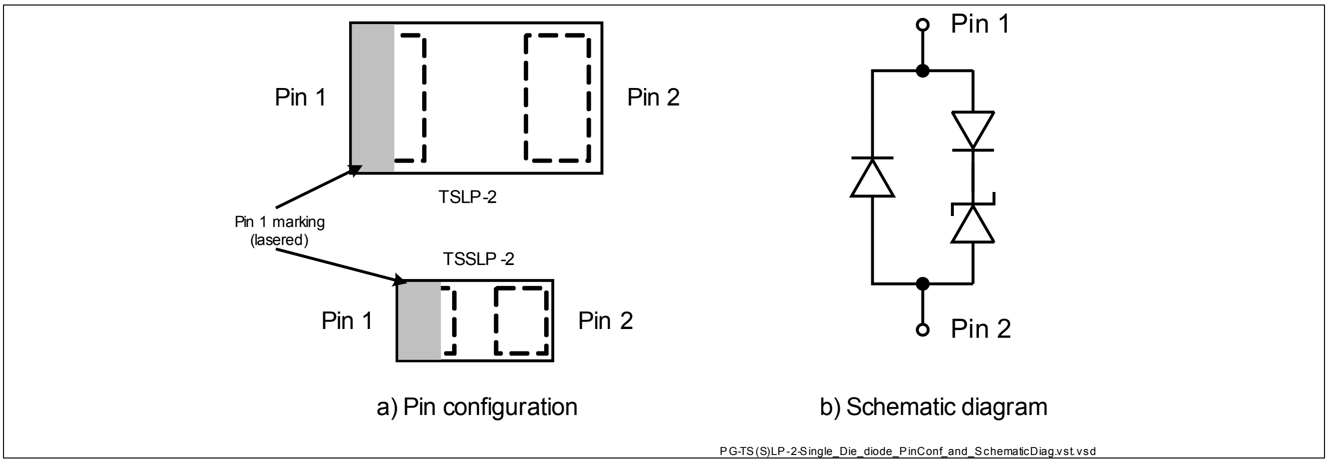


Figure 2-1 Pin Configuration and Schematic Diagram

Table 2-1 Ordering Information

Type	Package	Configuration	Marking code
ESD3V3XU1UL	PG-TSLP-2-17	1 line, uni-directional	X1
ESD3V3XU1US	PG-TSSLP-2-1	1 line, uni-directional	K

3 Characteristics

Table 3-1 Maximum Rating at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD (air / contact) discharge[1]	V_{ESD}	–	–	20	kV
Peak pulse current (t_p = 8/20 µs)[2]	I_{PP}	–	–	3	A
Operating temperature range	T_{OP}	-40	–	125	°C
Storage temperature	T_{stg}	-65	–	150	°C

1) V_{ESD} according to IEC61000-4-2 (R = 330 Ω, C = 150 pF)

2) I_{PP} according to IEC61000-4-5

3.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

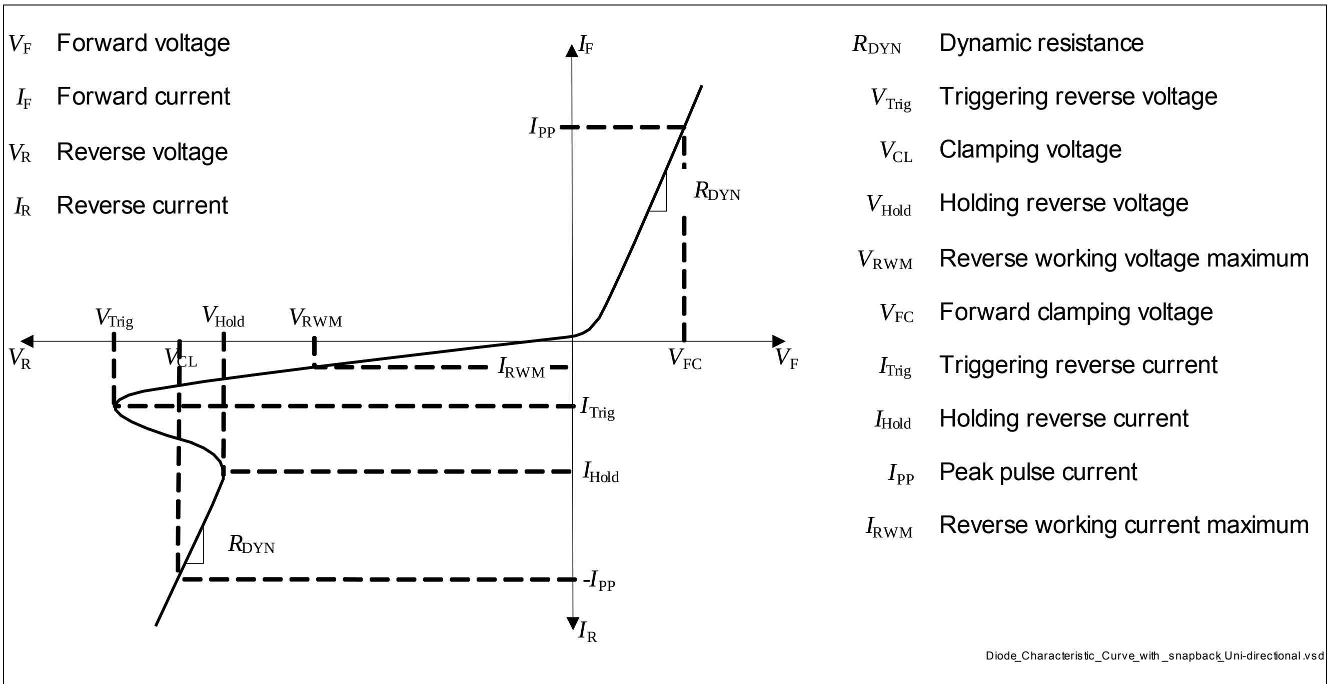


Figure 3-1 Definitions of electrical characteristics

Table 3-2 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	3.3	V	Pin 1 to Pin 2
Reverse current	I_R	–	1	50	nA	V_R = 3.3 V, from Pin 1 to Pin 2
Reverse breakdown voltage	V_{BR}	–	6.5	–	V	I_R = 1 mA from Pin 1 to Pin 2 voltage forced

Table 3-3 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	0.4	0.65	pF	V_R = 0 V, f = 1 MHz
		–	0.4	0.65	pF	V_R = 0 V, f = 1 GHz
Series inductance	L_S	–	0.4	–	nH	ESD3V3XU1US
		–	0.2	–	nH	ESD3V3XU1UL

Table 3-4 ESD Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Trigger voltage1) [2]	V_{TRIG}	–	7.2	–	V	TLP, from Pin 1 to Pin 2
Reverse clamping voltage1) [2]	V_{CL}	–	8	–	V	TLP, I_{PP} = 16 A, from Pin 1 to Pin 2
		–	11	–	V	TLP, I_{PP} = 30 A, from Pin 1 to Pin 2
Forward clamping voltage1) [2]	V_{FC}	–	6	–	V	TLP, I_{PP} = 16 A, from Pin 2 to Pin 1
		–	9	–	V	TLP, I_{PP} = 30 A, from Pin 2 to Pin 1
Dynamic resistance1) [2]	R_{DYN}	–	0.19	–	Ω	TLP, Pin 1 to Pin 2
		–	0.23	–	Ω	TLP, Pin 2 to Pin 1

1)Please refer to Application Note AN210. ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP), t_p = 100ns, t_r = 0.6 ns, I_{TLP} and V_{TLP} averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic TLP characteristic between I_{PP1} = 10 A and I_{PP2} = 40 A.

3.2 Typical Characteristics at T_A=25°C, unless otherwise specified

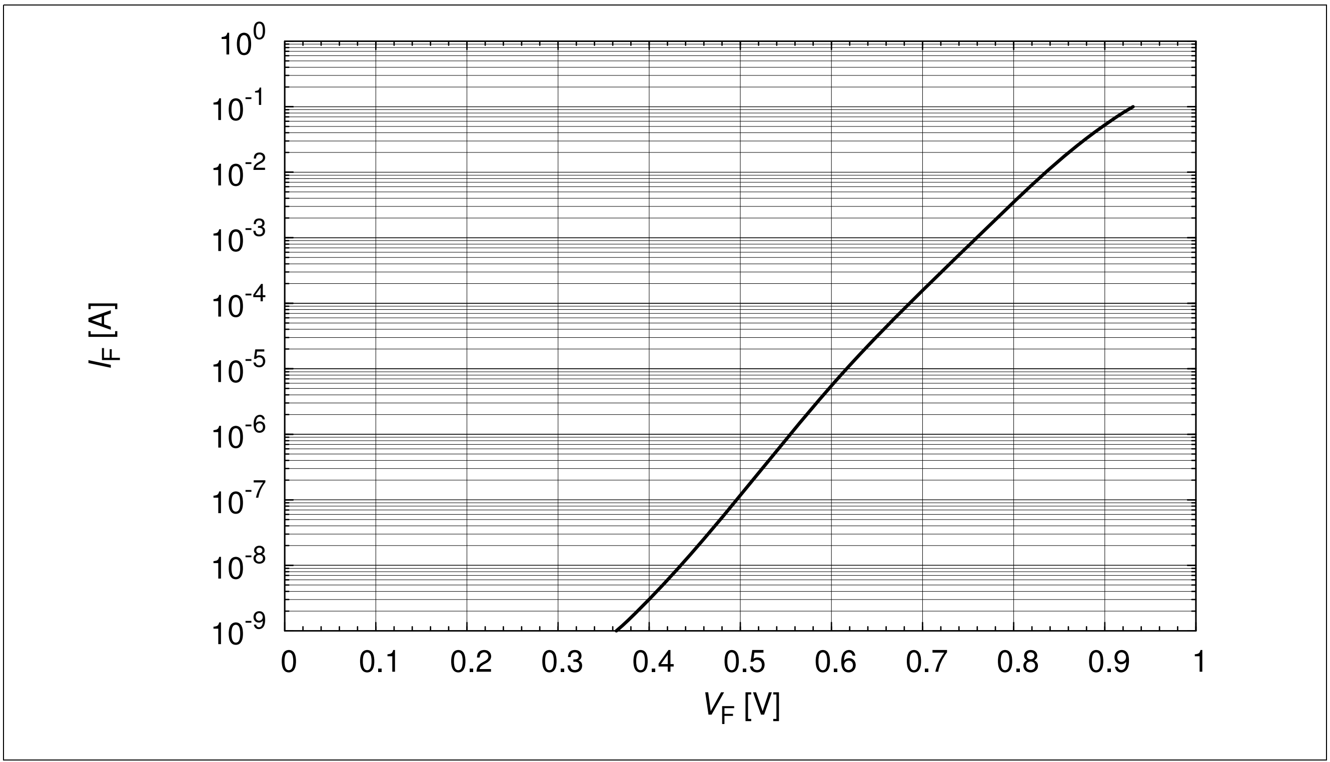


Figure 3-2 Forward current, I_F = (V_F)

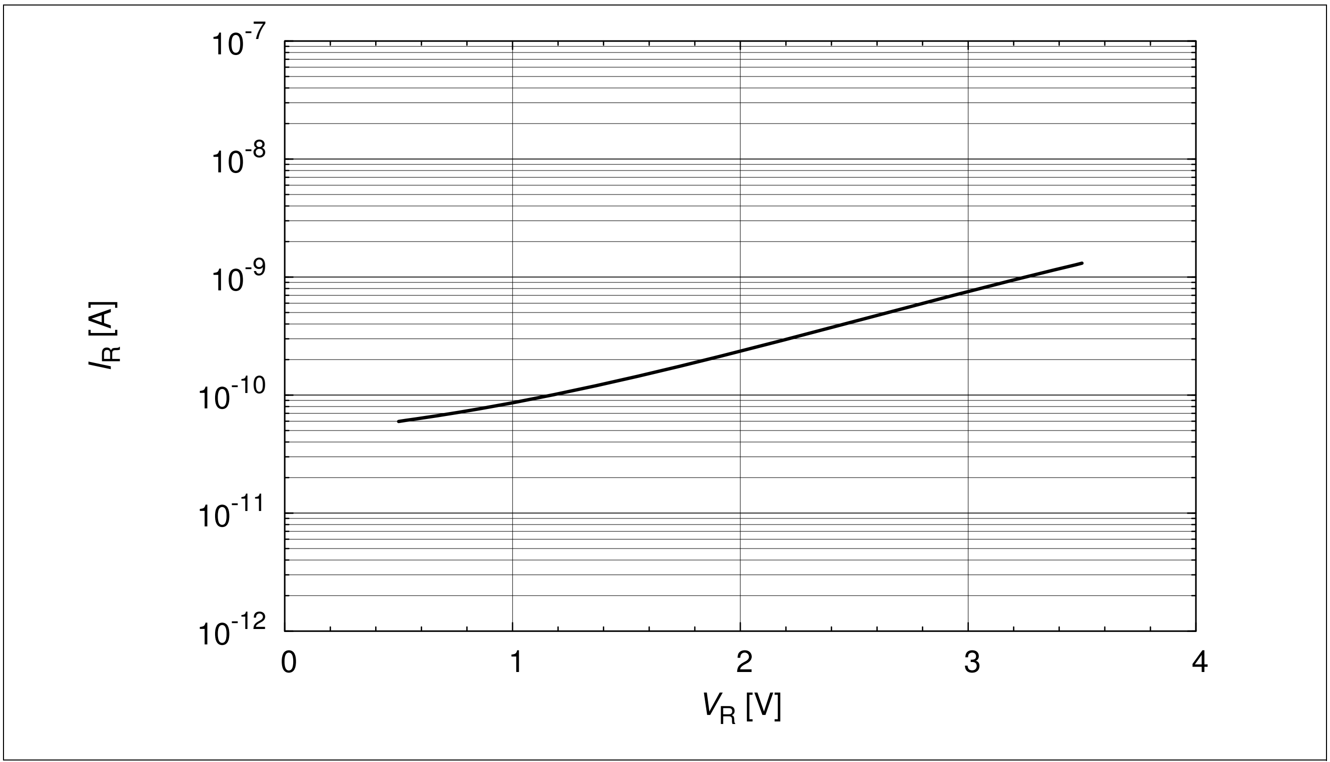


Figure 3-3 Reverse current, I_R = (V_R)

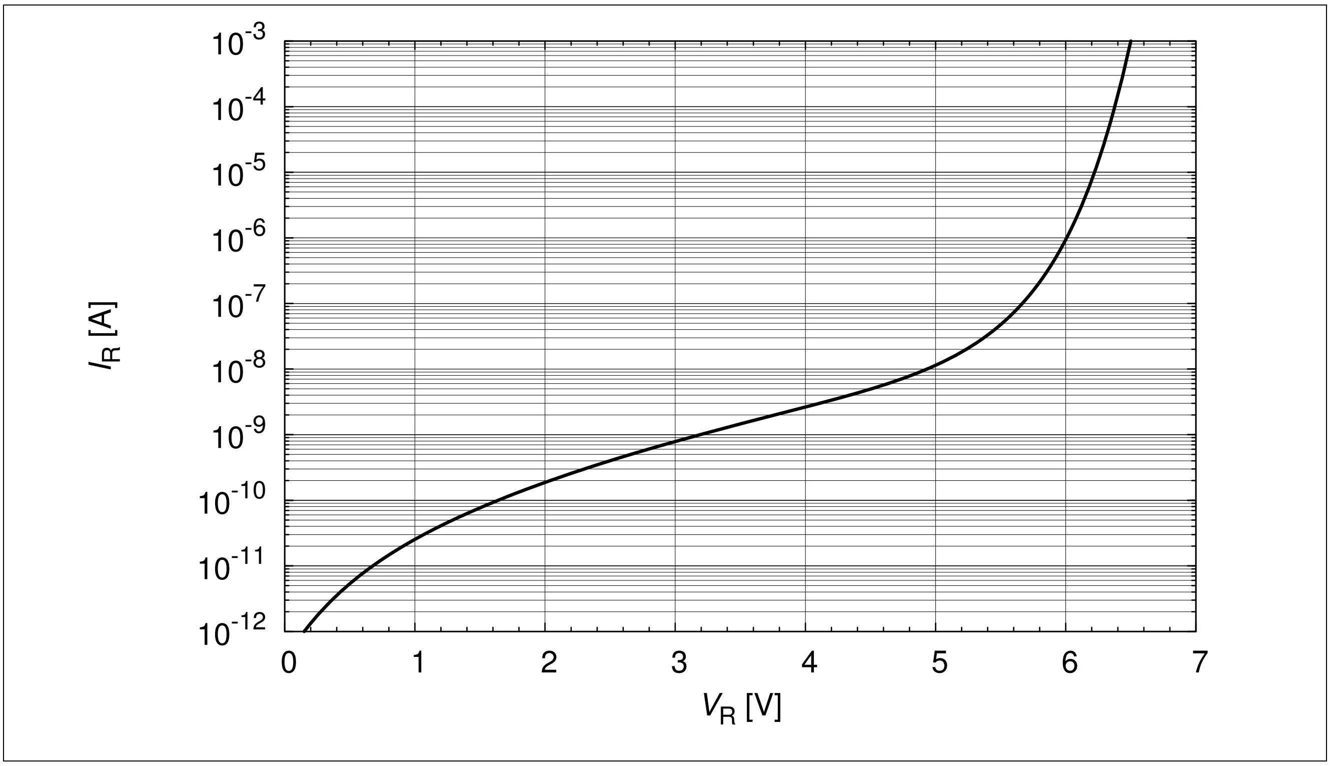


Figure 3-4 Reverse voltage characteristic, I_R = (V_R)

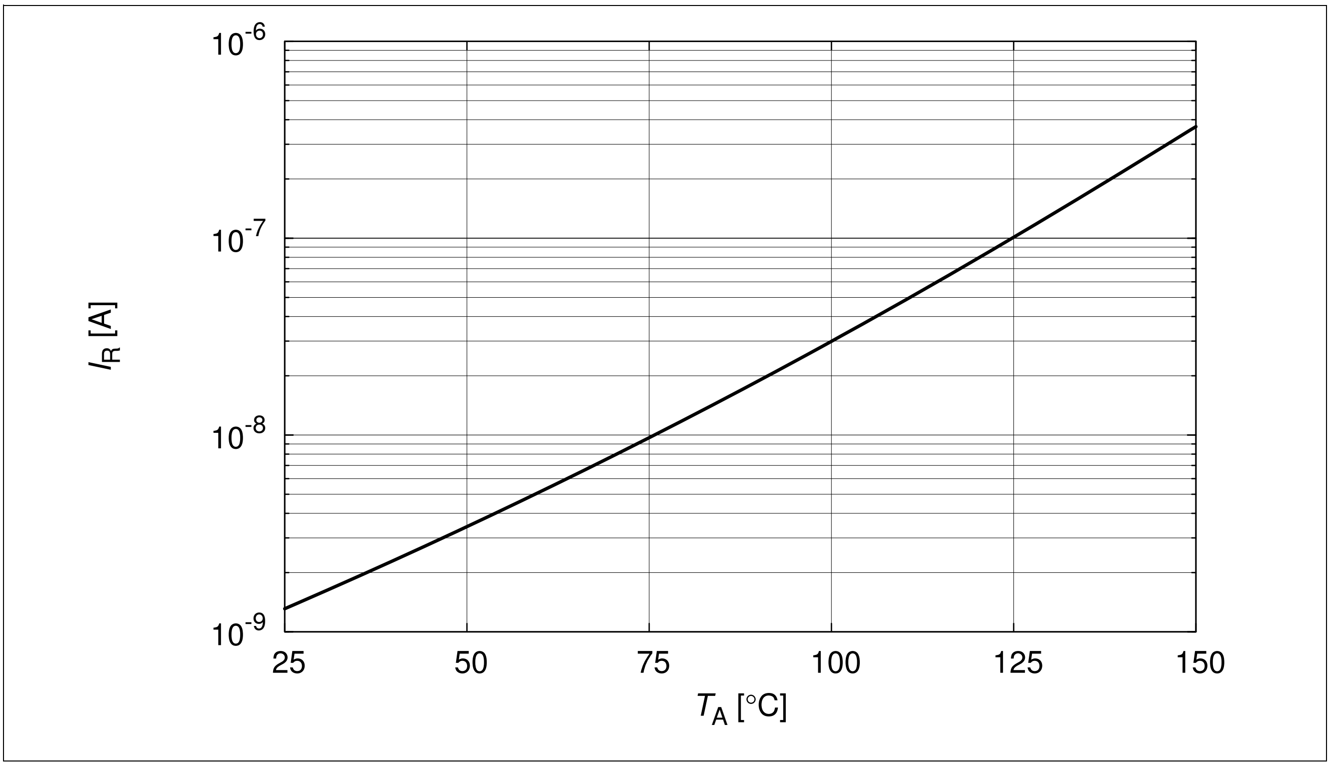


Figure 3-5 Reverse current $I_R = f(T_A)$, V_R = 3.3 V

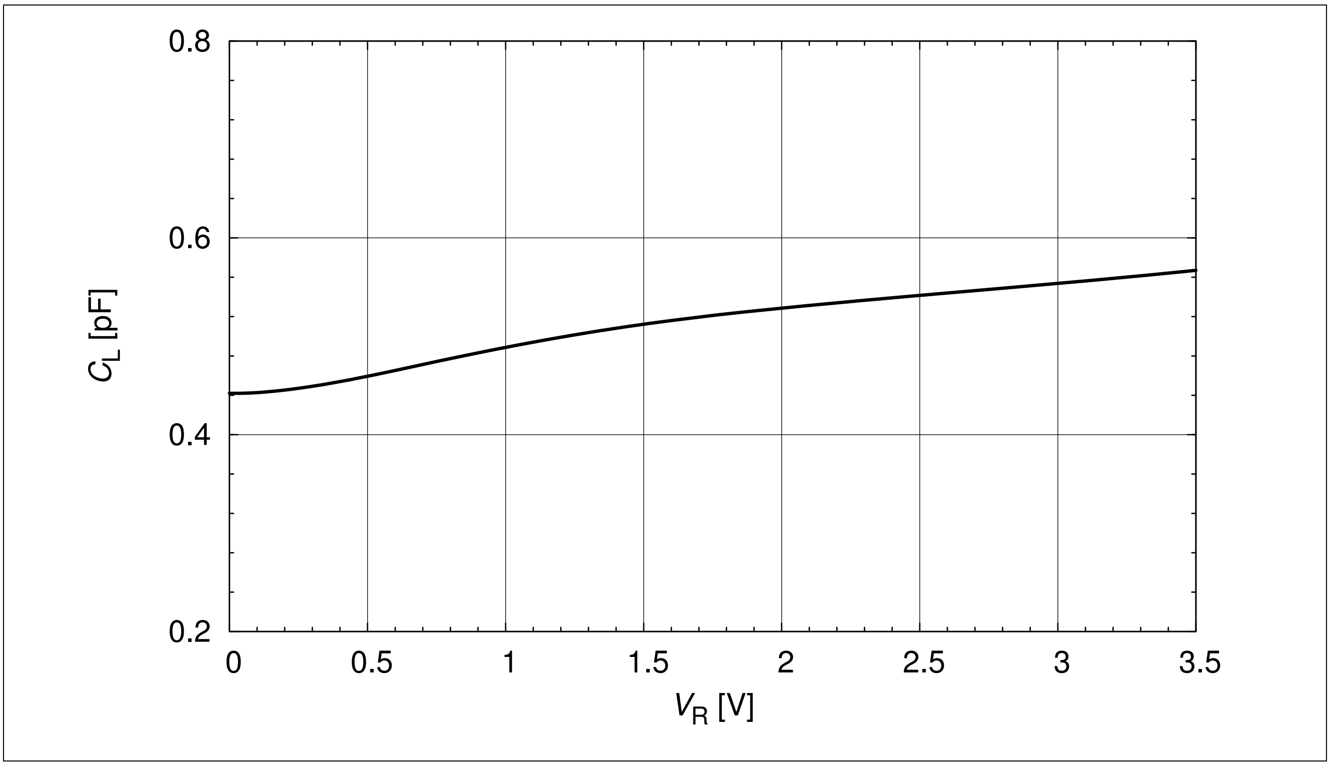


Figure 3-6 Line capacitance $C_L = f(V_R)$, f = 1MHz, from pin 1 to pin 2

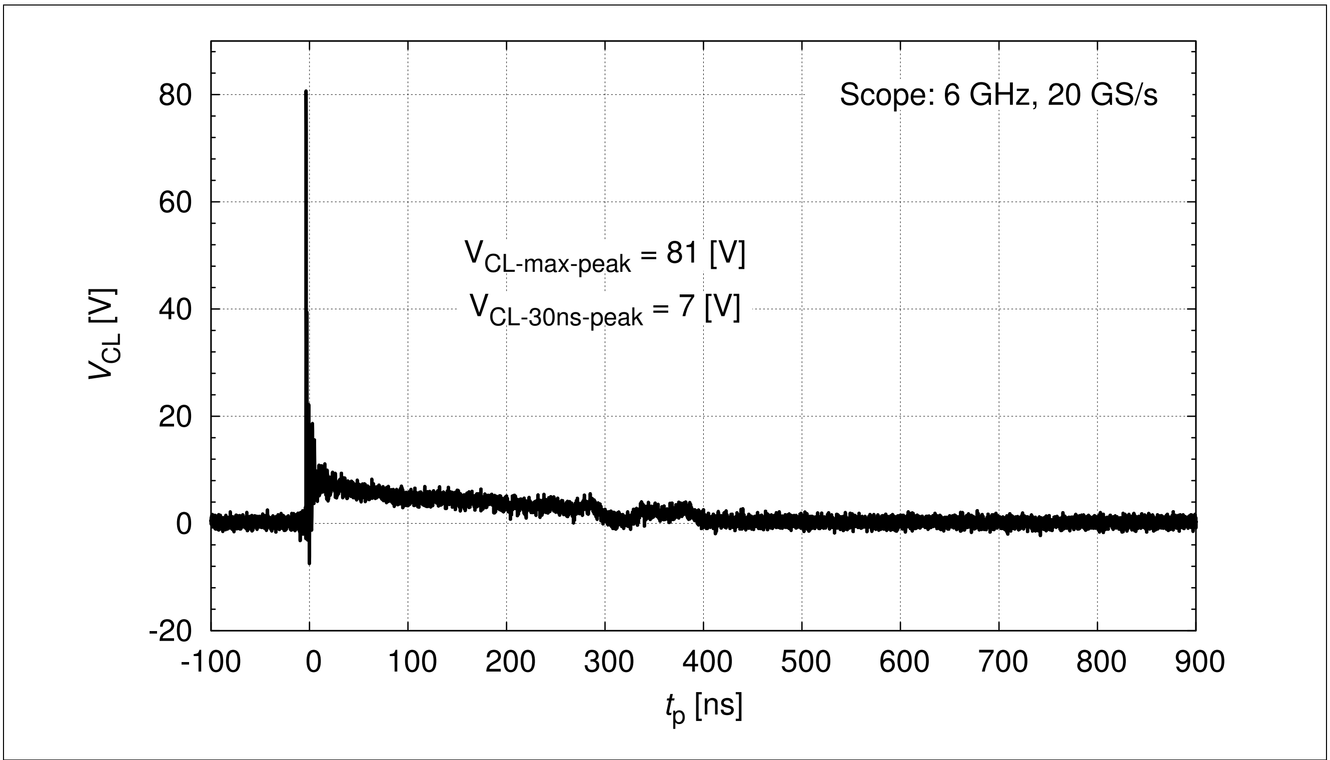


Figure 3-7 IEC61000-4-2 V_{CL} = *f*(*t*), 8 kV positive pulse from pin 1 to pin 2

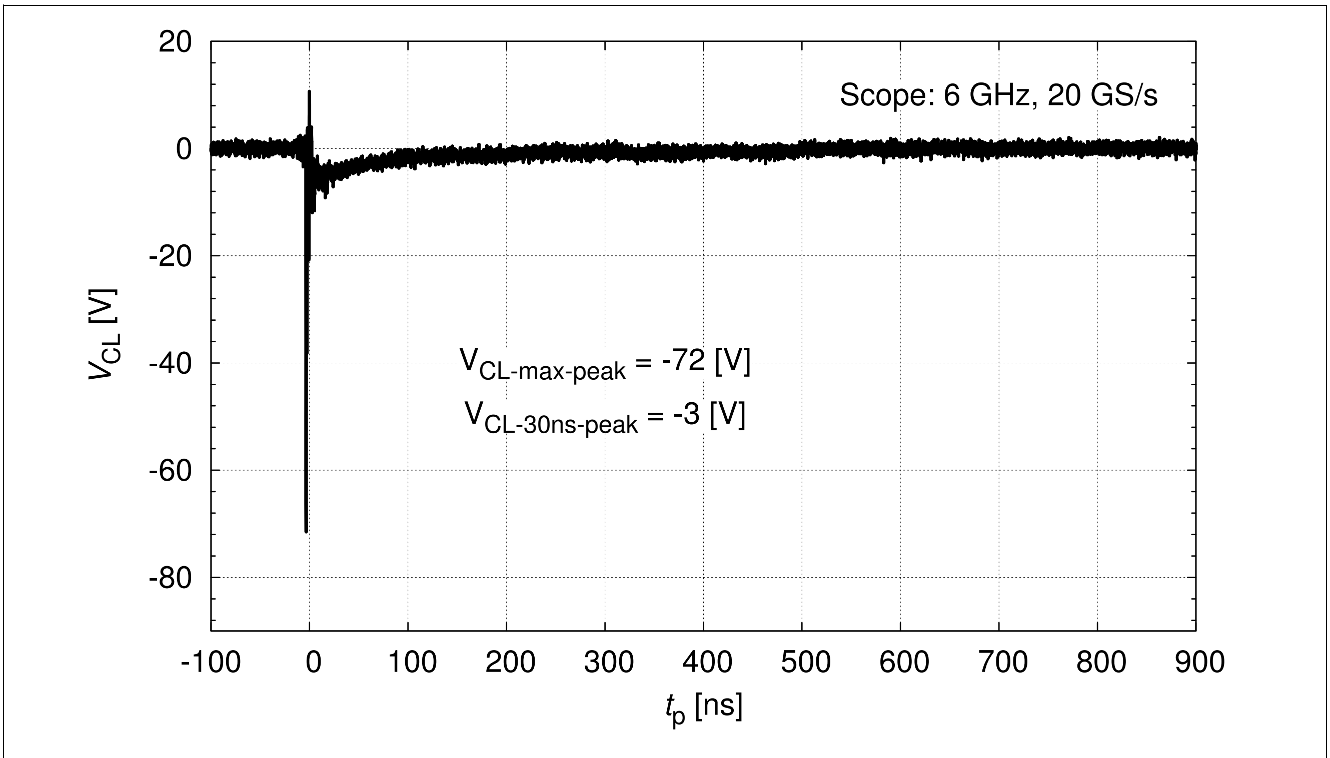


Figure 3-8 IEC61000-4-2 V_{CL} = *f*(*t*), 8 kV negative pulse from pin 1 to pin 2

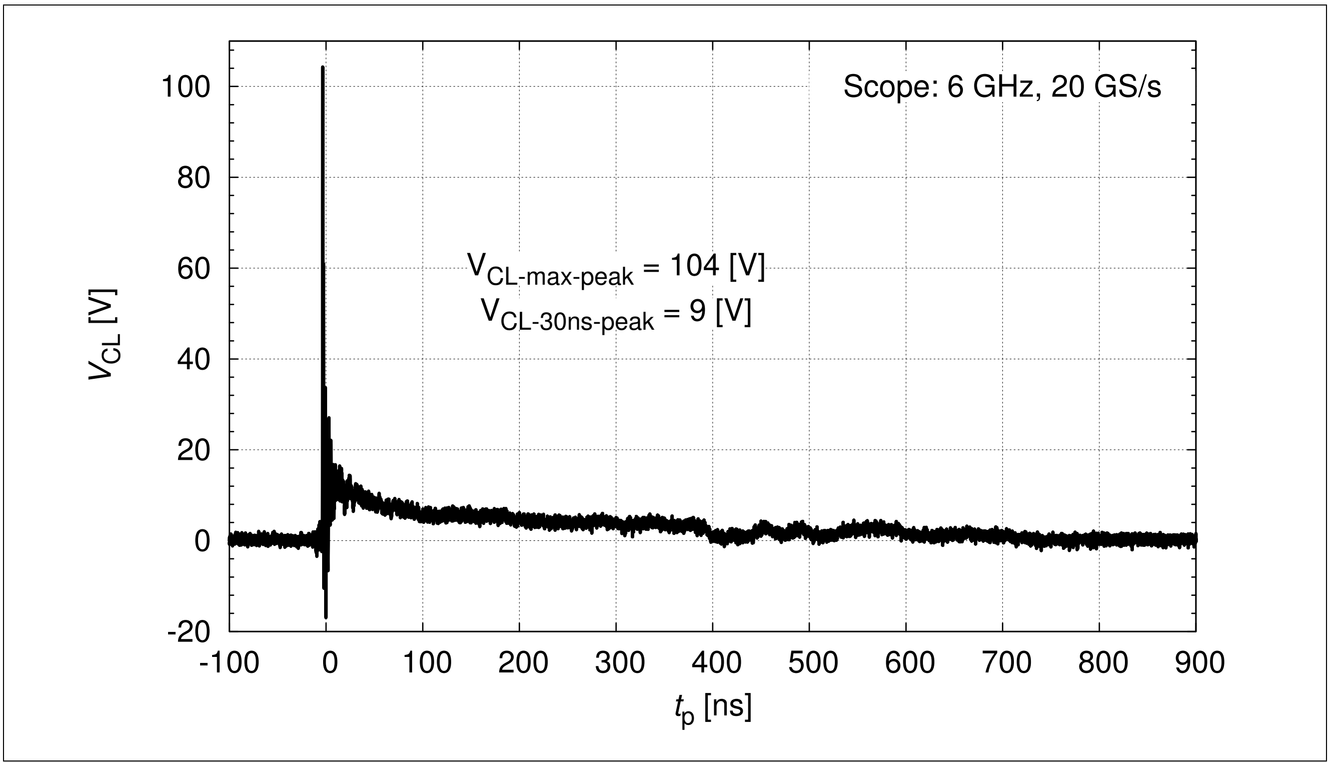


Figure 3-9 IEC61000-4-2 V_{CL} = $f(t)$, 15 kV positive pulse from pin 1 to pin 2

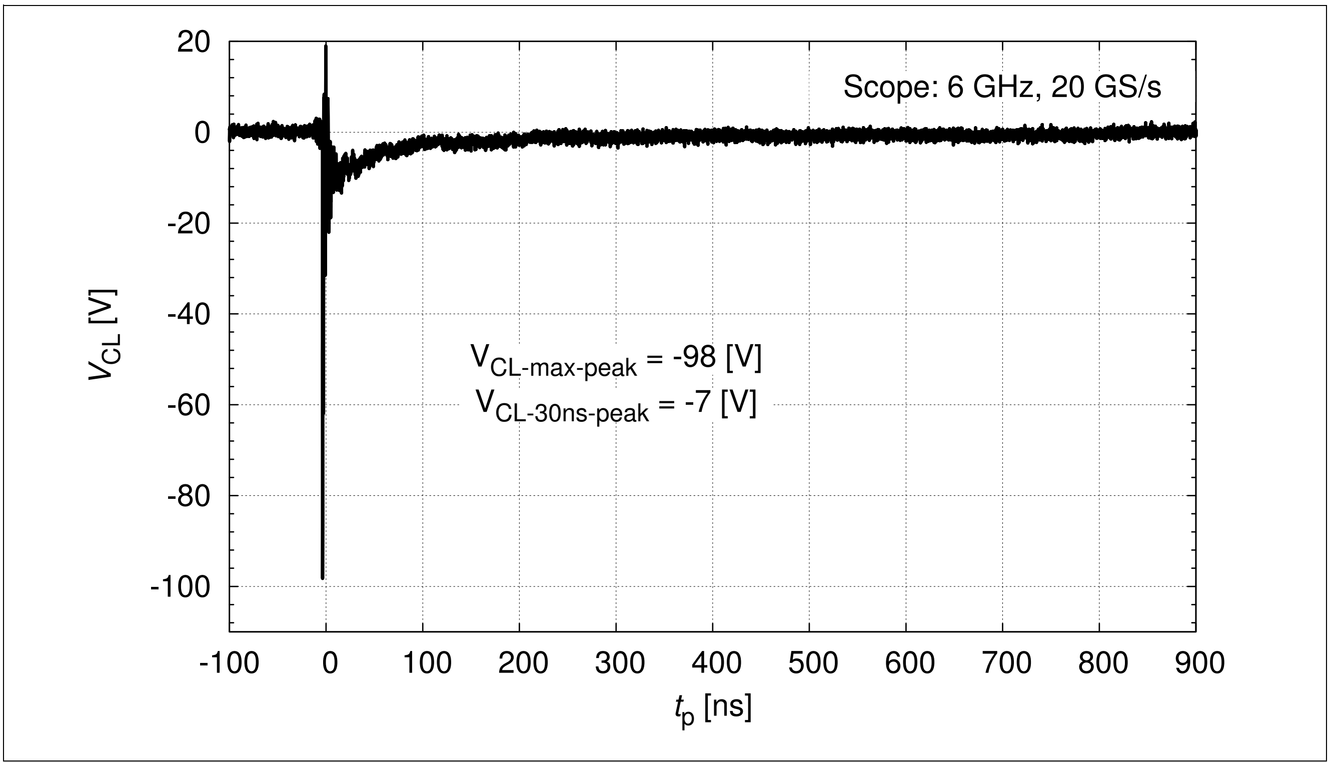


Figure 3-10 IEC61000-4-2 V_{CL} = $f(t)$, 15 kV negative pulse from pin 1 to pin 2

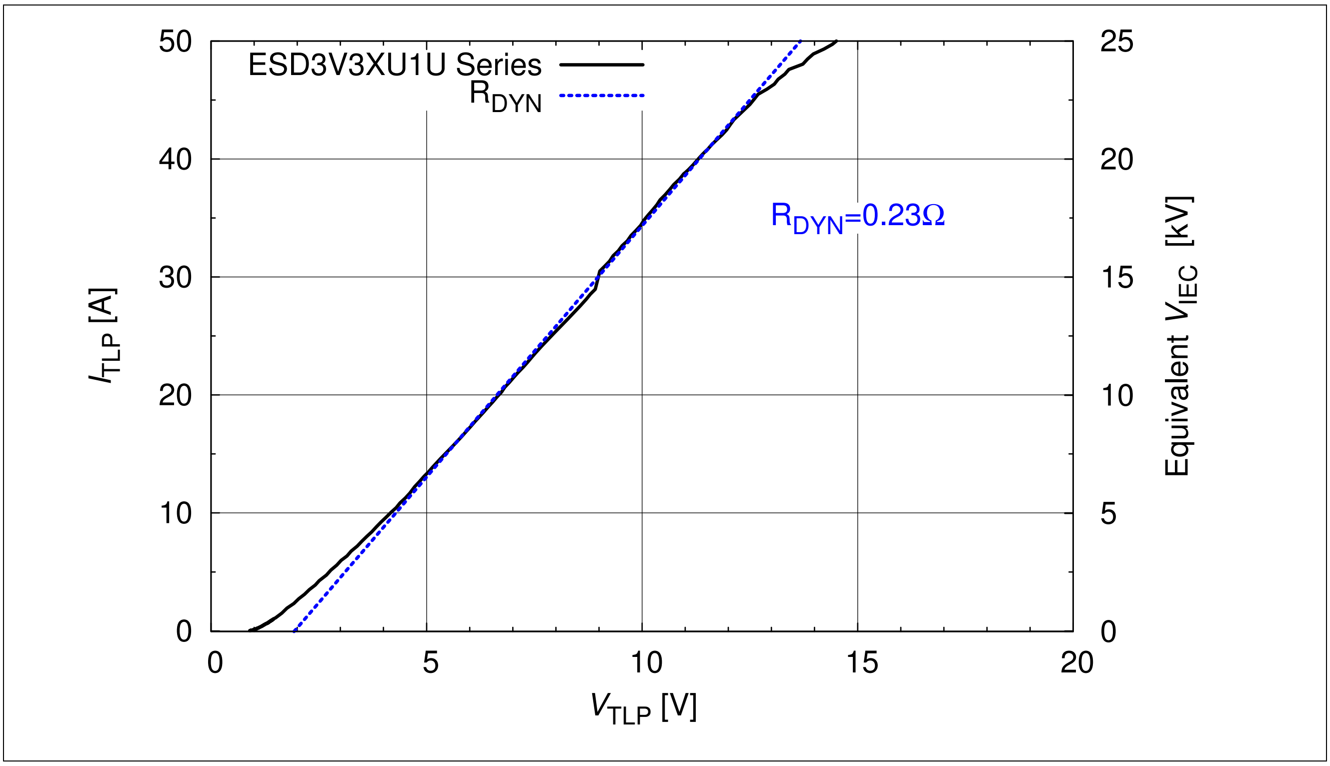


Figure 3-11 Clamping voltage $V_{TLP} = f(I_{TLP})$, from pin 2 to pin 1 Note: [2]

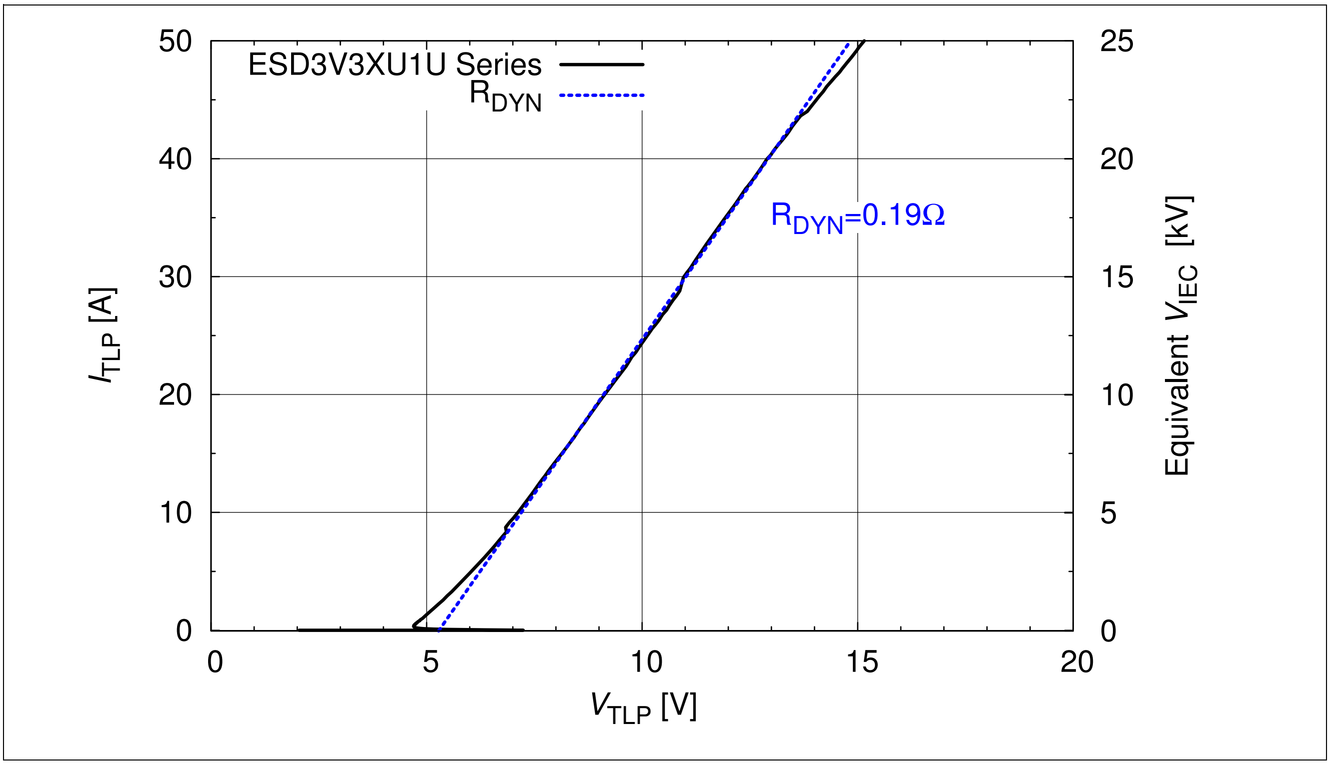


Figure 3-12 Clamping voltage $V_{TLP} = f(I_{TLP})$, from pin 1 to pin 2 Note: [2]

Note: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 600 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP charactertistic between I_{PP1} = 10 A and I_{PP2} = 40 A. The equivalent stress level V_{IEC} according IEC 61000-4-2 (R = 330 Ω, C = 150 pF) is calculated at the broad peak of the IEC waveform at t = 30 ns with 2 A / kV

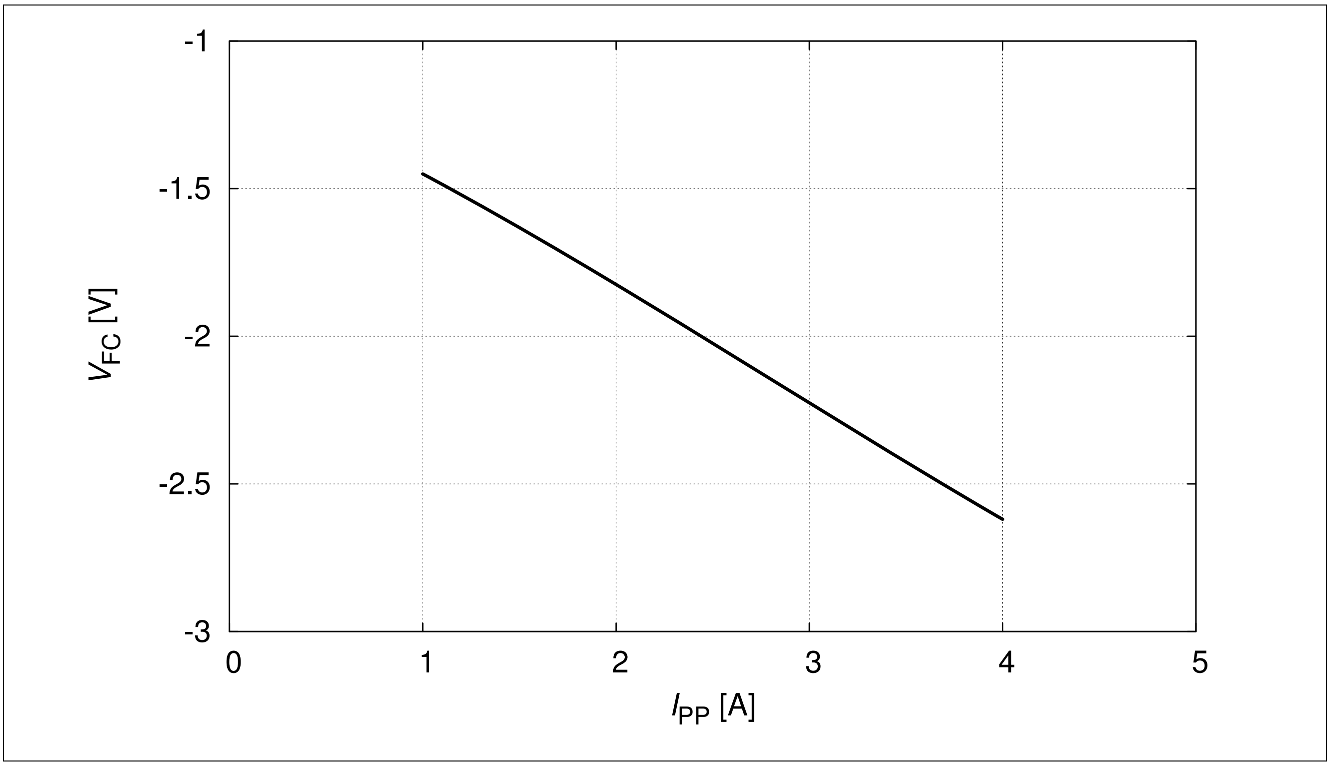


Figure 3-13 Forward clamping voltage $I_{PP} = f(V_{FC})$, from pin 1 to pin 2 according to IEC61000-4-5 (8/20 µs)

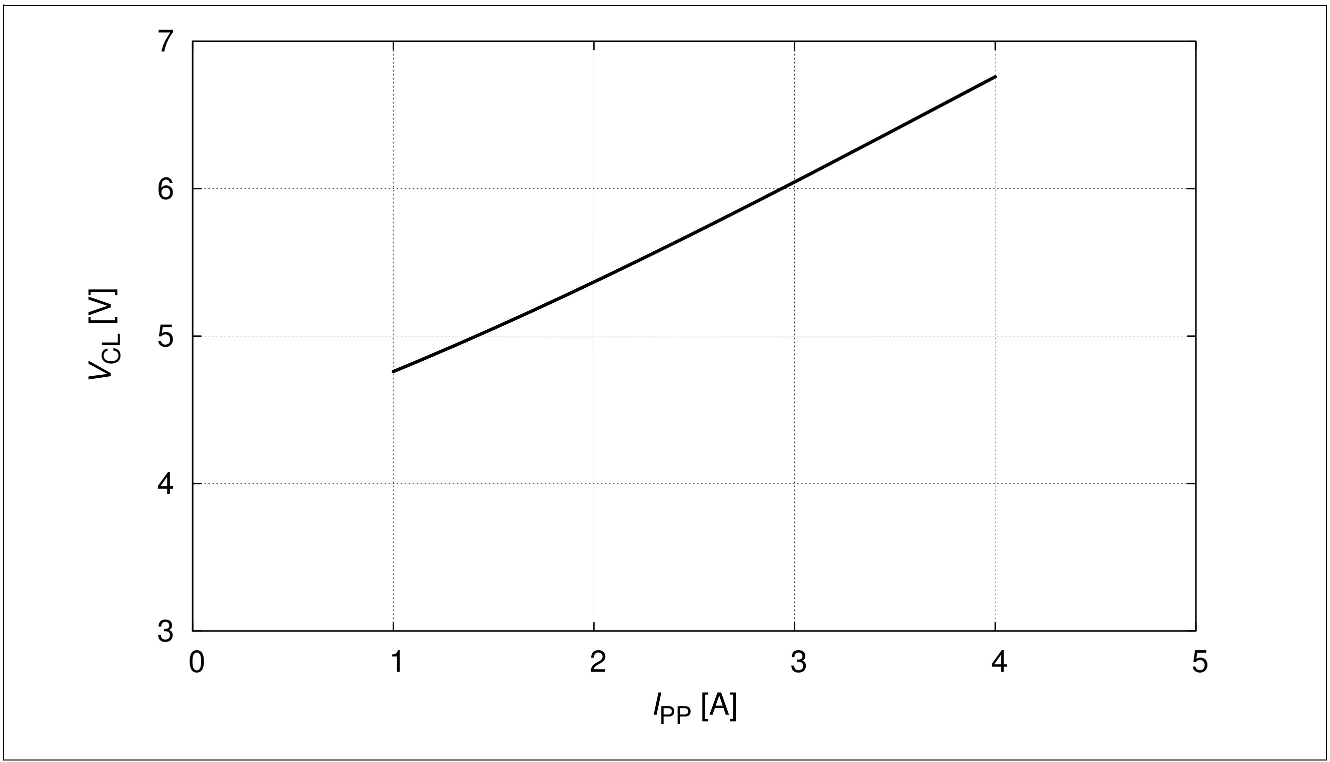


Figure 3-14 Reverse clamping voltage $I_{PP} = f(V_{CL})$, from pin 1 to pin 2 according to IEC61000-4-5 (8/20 µs)

4 Application Information

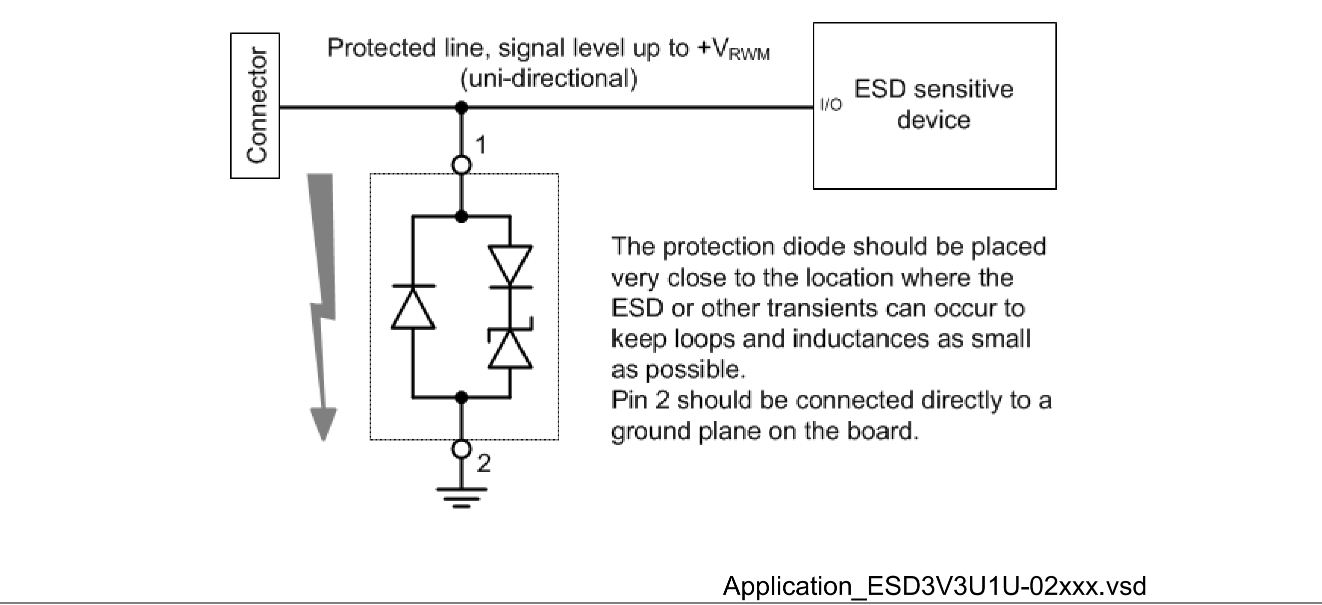


Figure 4-1 Single line, uni-directional ESD / Transient protection

5 Package Information

5.1 PG-TSLP-2-17 (mm) [3]

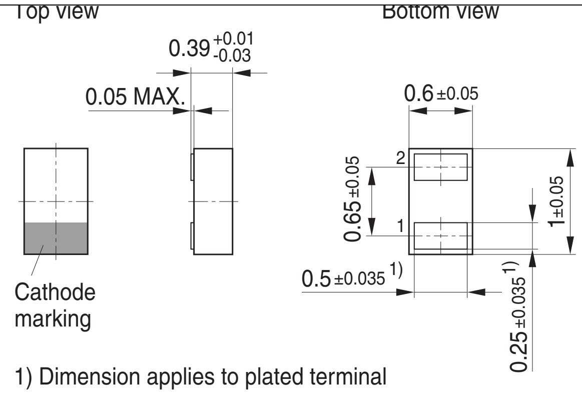


Figure 5-1 PG-TSLP-2-17: Package overview

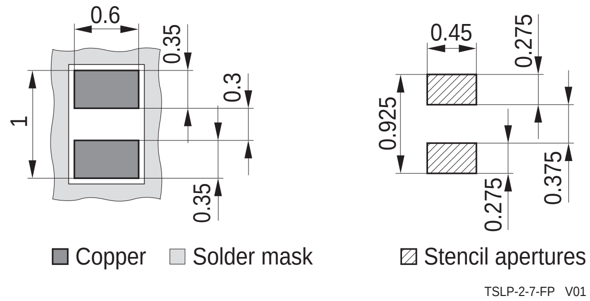


Figure 5-2 PG-TSLP-2-17: Footprint

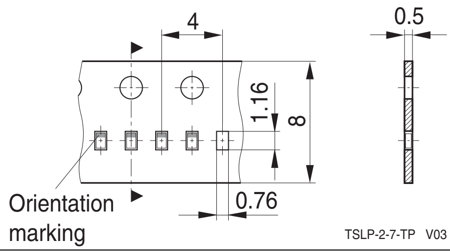


Figure 5-3 PG-TSLP-2-17: Packing

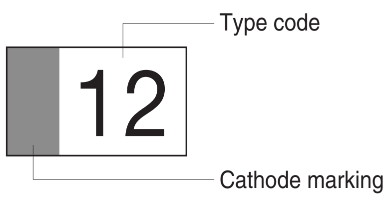


Figure 5-4 PG-TSLP-2-17: Marking (example)

5.2 PG-TSSLP-2-1 (mm) [3]

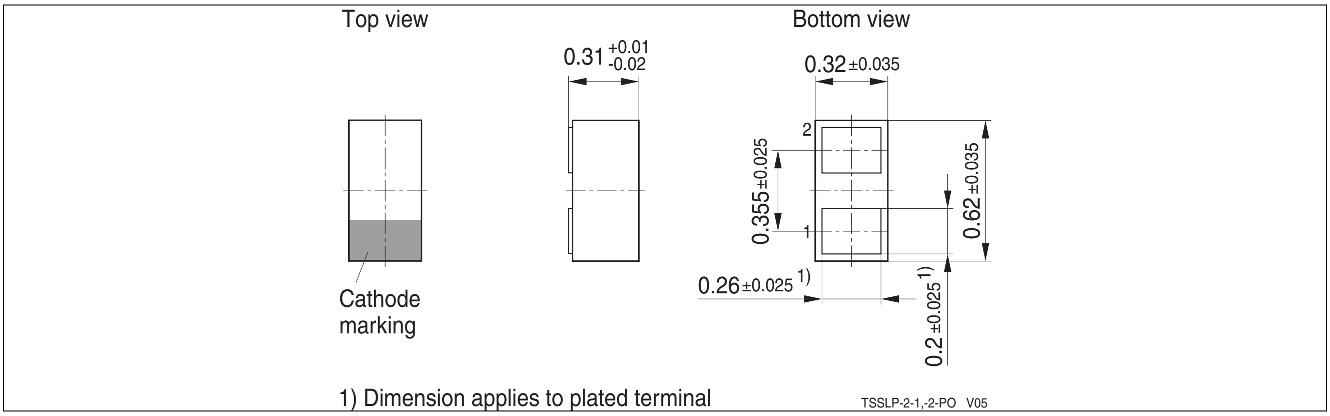


Figure 5-5 PG-TSSLP-2-1: Package overview

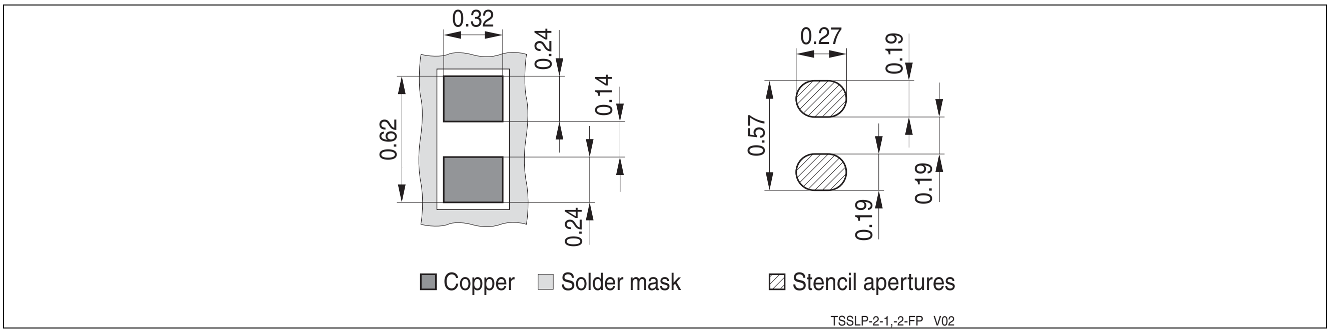
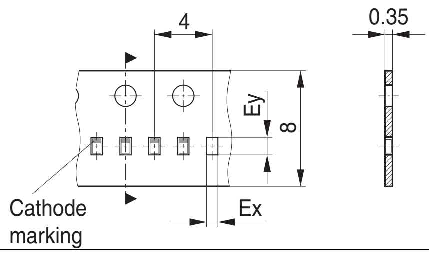


Figure 5-6 PG-TSSLP-2-1: Footprint



Tape type	Ex	Ey
Punched Tape	0.43	0.73
Embossed Tape	0.37	0.67

Deliveries can be both tape types (no selection possible).
Specification allows identical processing (pick & place) by users.

TSSLP-2-1,-2-TP V03

Figure 5-7 PG-TSSLP-2-1: Packing

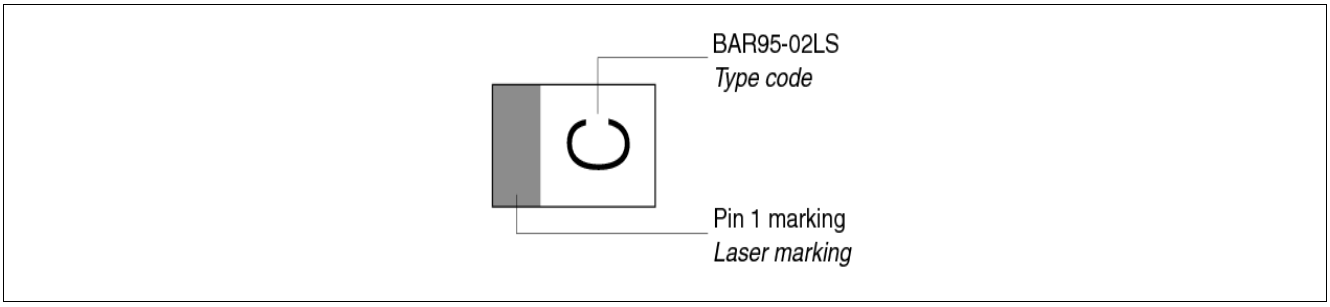


Figure 5-8 PG-TSSLP-2-1: Marking (example)

References

[1] On-chip ESD protection for integrated circuits, Albert Z. H. Wang, ISBN:0-7923-7647-1

[2] Infineon AG - **Application Note AN210:** Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

[3] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Package

Terminology

C_L	Line capacitance
DVI	Digital Visual Interface
EFT	Electrical Fast Transient
ESD	Electrostatic Discharge
HDMI	High Definition Multimedia Interface
IEC	International Electrotechnical Commission
I_{PP}	Peak pulse current
I_R	Reverse current
I_{RWM}	Reverse working current maximum
MDDI	Mobile Display Digital Interface
MIPI	Mobile Industrial Processor Interface
NFC	Near Field Communication
PCB	Printed Circuit Board
R_{DYN}	Dynamic resistance
RoHS	Restriction of Hazardous Substances Directive
S-ATA	Serial Advanced Technology Attachment
SWP	Single Wire Protocol
T_A	Ambient temperature
TLP	Transmission Line Pulse
T_{OP}	Operation temperature
t_p	Pulse duration
t_r	Pulse rise time
T_{stg}	Storage temperature
USB	Universal Serial Bus
V_{CL}	Reverse clamping voltage
V_{ESD}	Electrostatic discharge voltage
V_{FC}	Forward Clamping Voltage
V_{Hold}	Holding Voltage
V_{IEC}	Equivalent stress level according IEC61000-4-2 (R = 330 Ω, C = 150 pF)
V_R	Reverse voltage
V_{RWM}	Reverse working voltage maximum
V_{Trig}	Triggering Voltage
Z_0	Impedance

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