

**Rochester Electronics
Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN54F299, SN74F299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDFS071A – MARCH 1987 – REVISED OCTOBER 1993

- **Four Modes of Operation:**
 - Hold (Store)
 - Shift Right
 - Shift Left
 - Load Data
- Operates With Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Direct Overriding Clear
- **Applications:**
 - Stacked or Push-Down Registers
 - Buffer Storage
 - Accumulator Registers
- **Package Options Include Plastic**
 - Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

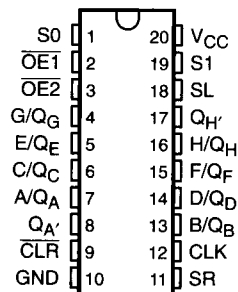
description

These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select (S_0 , S_1) inputs and two output-enable ($\overline{OE1}$, $\overline{OE2}$) inputs can be used to choose the modes of operation listed in the function table.

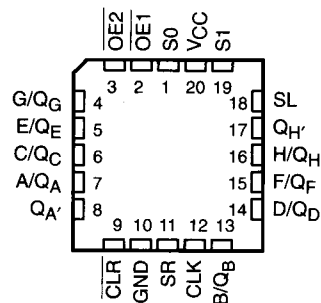
Synchronous parallel loading is accomplished by taking both S_0 and S_1 high. This places the 3-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs when the clear (\overline{CLR}) input is low. Taking either $\overline{OE1}$ or $\overline{OE2}$ high disables the outputs but has no effect on clearing, shifting, or storage of data.

The SN54F299 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74F299 is characterized for operation from 0°C to 70°C .

SN54F299 . . . J PACKAGE
SN74F299 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F299 . . . FK PACKAGE
(TOP VIEW)



SN54F299, SN74F299

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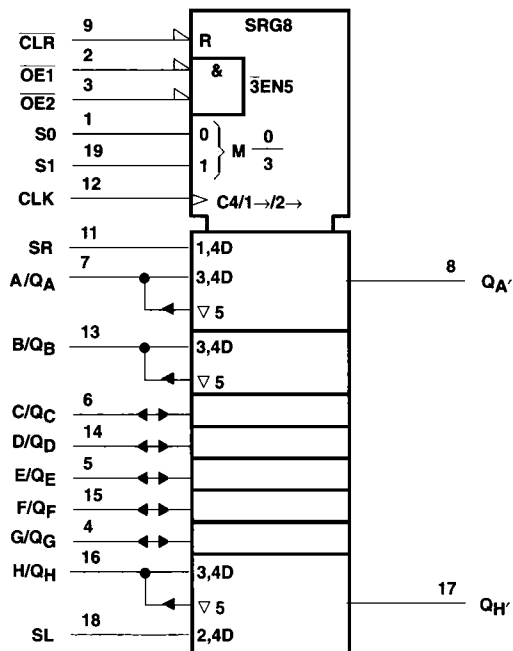
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	CLR	S1	S0	OE1†	OE2†	CLK	SL	SR	A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
	H	X	X	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
Shift Right	H	L	H	L	L	↑	X	H	H	QA _n	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	H	QG _n
Shift Left	H	H	L	L	L	↑	H	X	L	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	QH _n	QB _n	H
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

† When one or both output-enable inputs are high the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

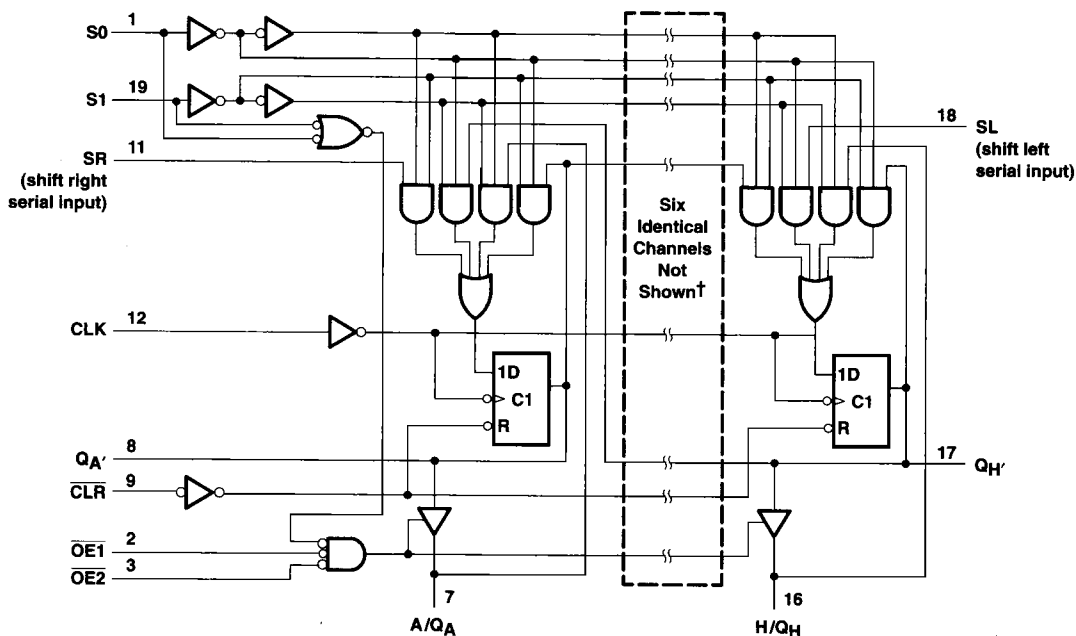
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logic diagram (positive logic)



† I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state	–0.5 V to 5.5 V
Voltage range applied to any output in the high state	–0.5 V to V_{CC}
Current into any output in the low state: Q_A' or Q_H'	40 mA
SN54F299 (Q_A thru Q_H)	40 mA
SN74F299 (Q_A thru Q_H)	48 mA
Operating free-air temperature range: SN54F299	–55°C to 125°C
SN74F299	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

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8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

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recommended operating conditions

			SN54F299			SN74F299			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
I _{IK}	Input clamp current				–18			–18	mA
I _{OH}	High-level output current	Q _A ' or Q _H '			–1			–1	mA
		Q _A thru Q _H			–3			–3	
I _{OL}	Low-level output current	Q _A ' or Q _H '			20			20	mA
		Q _A thru Q _H			20			24	
T _A	Operating free-air temperature		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				SN54F299			SN74F299			UNIT
						MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V,	I _I = –18 mA					–1.2			–1.2	V
V _{OH}	Q _A ' or Q _H '	V _{CC} = 4.5 V	I _{OH} = –1 mA		2.5	3.4		2.5	3.4			V
	Q _A thru Q _H		I _{OH} = –1 mA		2.5	3.4		2.5	3.4			
			I _{OH} = –3 mA		2.4	3.3		2.4	3.3			
	Any output	V _{CC} = 4.75 V,	I _{OH} = –1 mA to –3 mA						2.7			
V _{OL}	Q _A ' or Q _H '	V _{CC} = 4.5 V	I _{OL} = 20 mA			0.3	0.5		0.3	0.5		V
	Q _A thru Q _H		I _{OL} = 20 mA			0.3	0.5					
			I _{OL} = 24 mA						0.35	0.5		
I _I	A thru H	V _{CC} = 5.5 V	V _I = 5.5 V				1				1	mA
	Any other		V _I = 7 V				0.1				0.1	
I _{IH} ‡	A thru H	V _{CC} = 5.5 V,	V _I = 2.7 V				70				70	μA
	Any other						20				20	
I _{IL} ‡	A thru H	V _{CC} = 5.5 V,	V _I = 0.5 V				–0.65				–0.65	mA
	S0 or S1						–1.2				–1.2	
	Any other						–0.6				–0.6	
I _{OS} §		V _{CC} = 5.5 V,	V _O = 0		–60		–150		–60		–150	mA
I _{CC}		V _{CC} = 5.5 V,	See Note 2			68	95		68	95		mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports (Q_A thru Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with OE1, OE2, and CLK at 4.5 V.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		SN54F299		SN74F299		UNIT
				'F299						
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	70	0	65	0	70	MHz
t_w	Pulse duration	CLK high or low		7		8		7		ns
		$\overline{\text{CLR}}$ low		7		8		7		
t_{su}	Setup time before CLK \uparrow	S0 or S1	High or low	8.5		9.5		8.5		ns
		A/Q _A thru H/Q _H , SR, or SL	High or low	5.5		6.5		5.5		
	Inactive-state setup time before CLK $\uparrow\uparrow$	$\overline{\text{CLR}}$	High	7		13		7		
t_h	Hold time after CLK \uparrow	S0 or S1	High or low	0		0		0		ns
		A/Q _A thru H/Q _H , SR, or SL	High or low	2		2		2		

$\uparrow\uparrow$ Inactive-state setup time is also referred to as recovery time.

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 5 V, CL = 50 pF, RL = 500 Ω, TA = 25°C			VCC = 4.5 V to 5.5 V, CL = 50 pF, RL = 500 Ω, TA = MIN to MAX‡				UNIT
			'F299			SN54F299		SN74F299		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
fmax			70	100		65		70		MHz
tPLH	CLK	QA' or QH'	3.2	6.6	9	2.7	10.5	3.2	10	ns
tPHL			2.7	6.1	8.5	2.2	10	2.7	9.5	
tPLH	CLK	QA thru QH	3.2	6.6	9	2.7	11	3.2	10	ns
tPHL			4.2	8.1	11	3.7	12.5	4.2	12	
tPHL	CLR	QA' or QH'	3.7	7.1	9.5	3.2	11.5	3.7	10.5	ns
		QA thru QH	5.7	10.6	14	5	15.5	5.7	15	
tPZH	OE1 or OE2	QA thru QH	2.7	5.6	8	2.2	10.5	2.7	9	ns
tPZL			3.2	6.6	10	2.7	12	3.2	11	
tPHZ	OE1 or OE2	QA thru QH	1.7	4.1	6	1.7	9	1.7	7	ns
tPLZ			1.2	3.6	5.5	1.2	7.5	1.2	6.5	

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

