HARRIS SEMICONDUCTOR

IRFPG40, IRFPG42

4.3A and 3.9A, 1000V, 3.5 and 4.2 Ohm, N-Channel Power MOSFETs

January 1998

Features

- **IRFPG40: 4.3A, 1000V, $r_{DS(ON)}$ = 3.5Ω**
- **IRFPG42: 3.9A, 1000V, $r_{DS(ON)}$ = 4.2Ω**
- **UIS SOA Rating Curve (Single Pulse)**
- **-55°C to 150°C Operating and Storage Temperature**
- **Related Literature**
  - **TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"**

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFPG40	TO-247	IRFPG40
IRFPG42	TO-247	IRFPG42

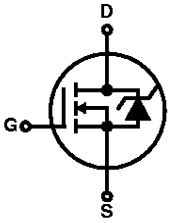
NOTE: When ordering, include the entire part number.

Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

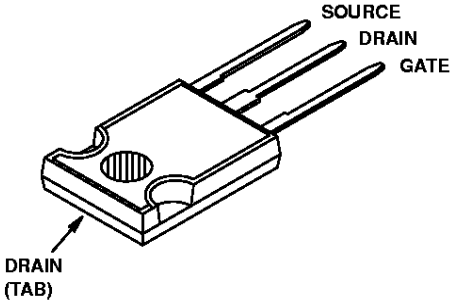
Formerly developmental type TA09850.

Symbol



Packaging

JEDEC STYLE TO-247



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2879.1**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		IRFPG40	IRFPG42	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	1000	1000	V
Drain to Gate Voltage (Note 1)	V_{DGR}	1000	1000	V
Continuous Drain Current	I_D	4.3	3.9	A
Pulsed Drain Current (Note 3)	I_{DM}	17	16	A
Gate to Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/ ^{o}C
Single Pulse Avalanche Energy Rating (Note 3)	E_{AS}	490	490	mJ
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	^{o}C
Maximum Temperature for Soldering				
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	^{o}C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V, (Figure 9)	1000	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	25	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 150^oC$	-	250	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 2.5A, V_{GS} = 10V, (Figures 7, 8)	-		
IRFPG40			-	3.5	Ω
IRFPG42			-	4.2	Ω
Forward Transconductance (Note 2)	g_{fs}	I_D = 2.5A, V_{DS} = 100V, (Figure 11)	3.5	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 500V, I = 3.9A, R_G = 9.1Ω, R_L = 120Ω V_{GS} = 10V, (See Figures 16, 17)	-	30	ns
Rise Time	t_r		-	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	170	ns
Fall Time	t_f		-	50	ns
Total Gate Charge	$Q_{g(TOT)}$	ID = 3.9A, VDS = 800V, VGS = 10V, (Figure 13, 18, 19)	-	120	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	0.83	^{o}C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	40	^{o}C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 4.3A (Figure 12)	-	1.8	V
Reverse Recovery Time	t_{rr}	I_{SD} = 3.9A, dI_{SD}/dt = 100A/µs	-	1000	ns

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.
4. V_{DD} = 25V, starting $T_J = 25^oC$, L = 640µH, R_G = 25Ω, peak I_{AS}= 9.2A (Figures 3, 14, 15).

Typical Performance Curves Unless Otherwise Specified

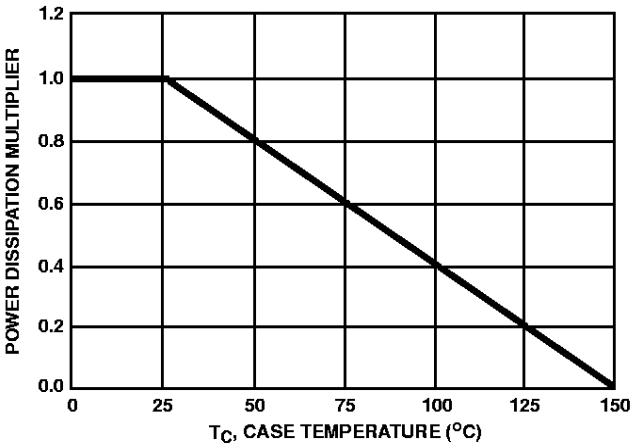


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

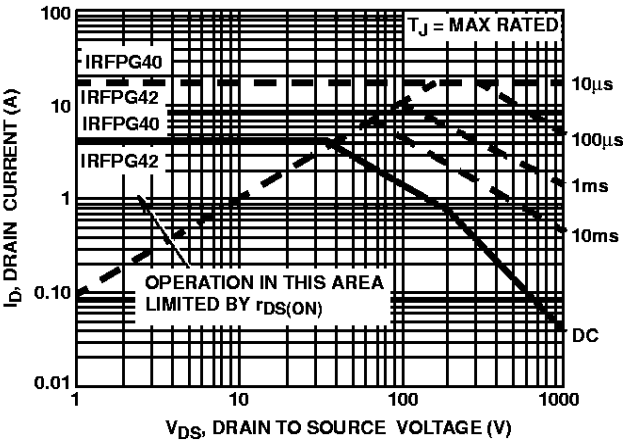


FIGURE 2. FORWARD BIAS SAFE OPERATING AREA

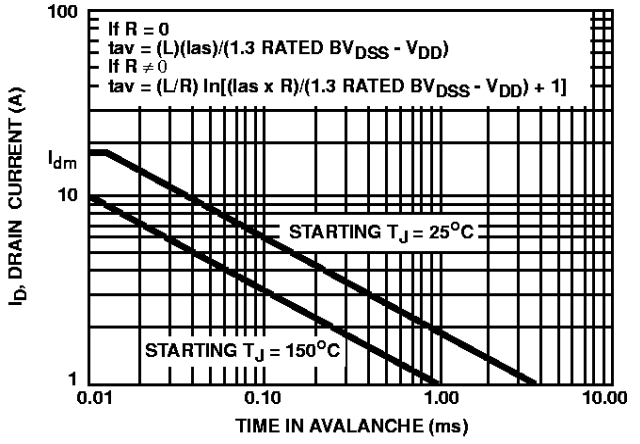


FIGURE 3. UNCLAMPED INDUCTIVE SWITCHING SOA

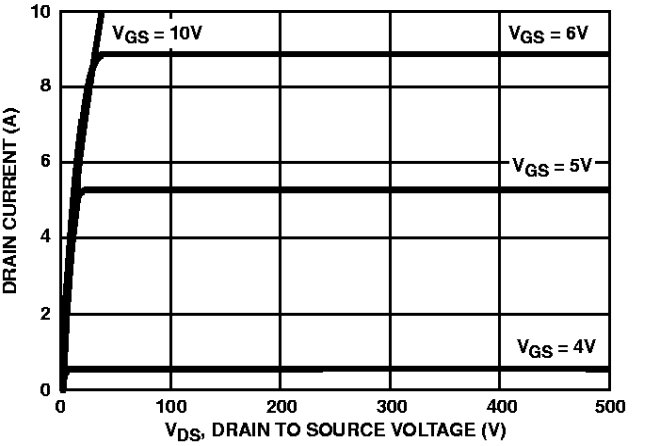


FIGURE 4. OUTPUT CHARACTERISTICS

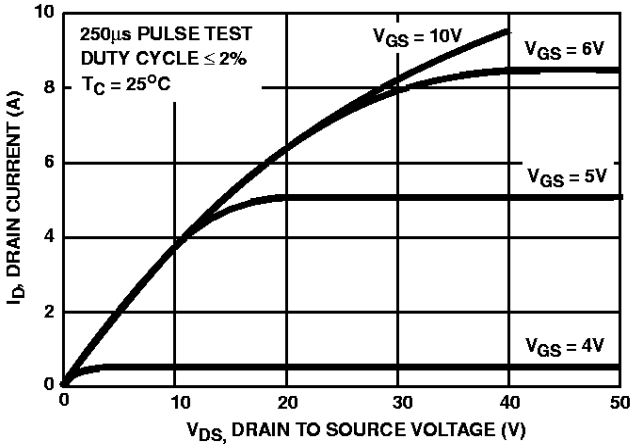


FIGURE 5. SATURATION CHARACTERISTICS

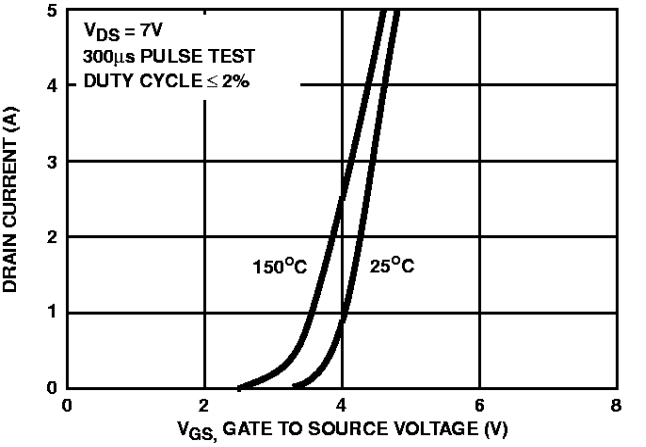


FIGURE 6. TRANSFER CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

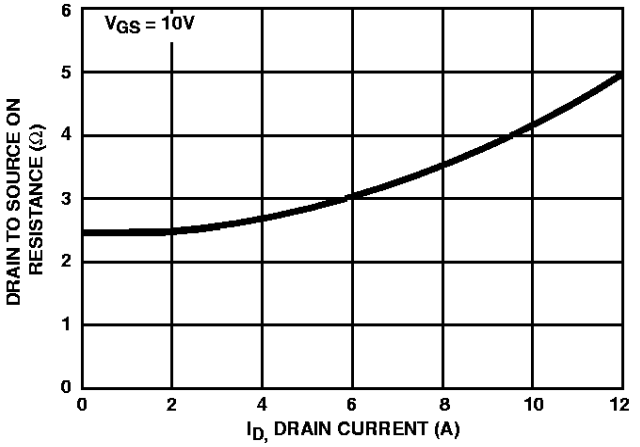


FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

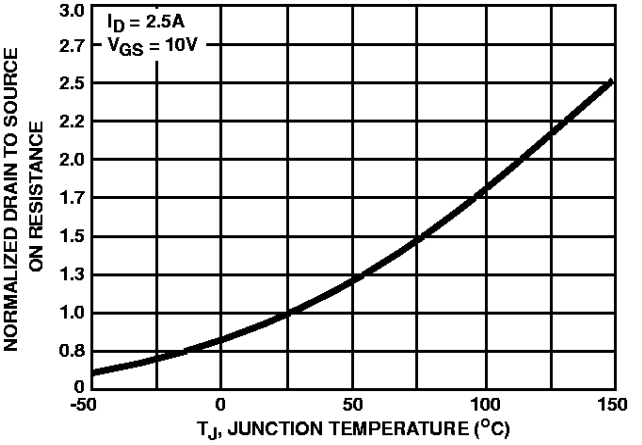


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

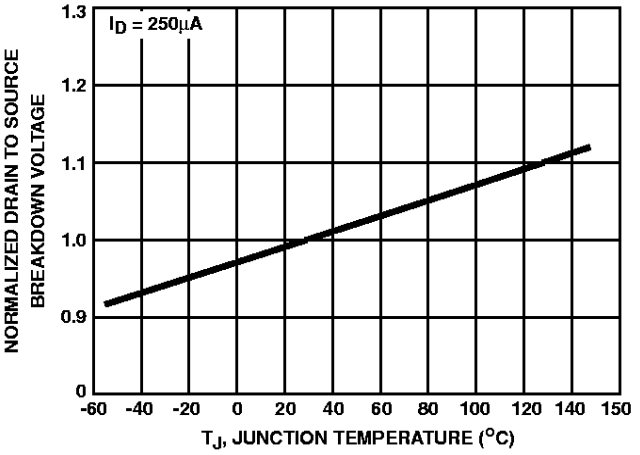


FIGURE 9. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs. JUNCTION TEMPERATURE

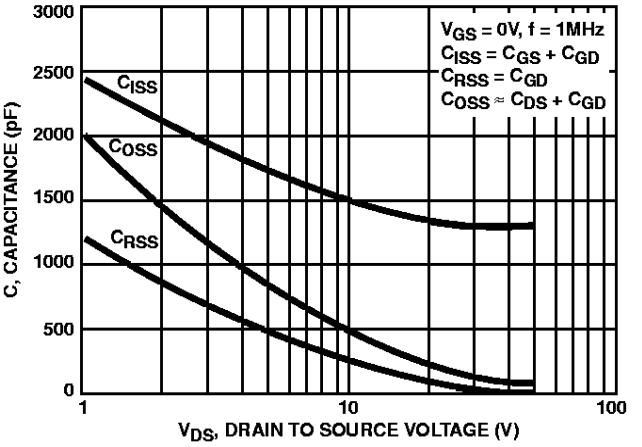


FIGURE 10. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

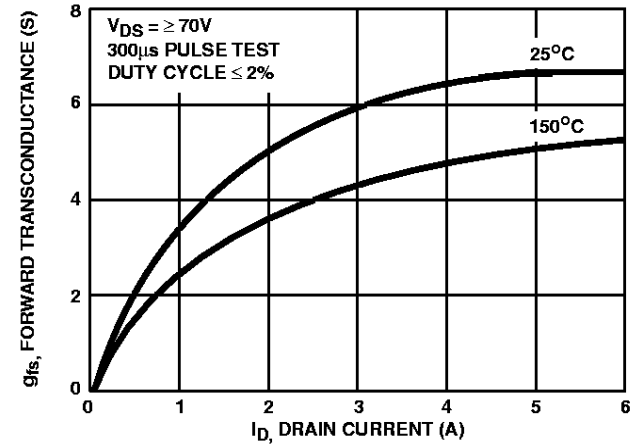


FIGURE 11. TRANSCONDUCTANCE vs DRAIN CURRENT

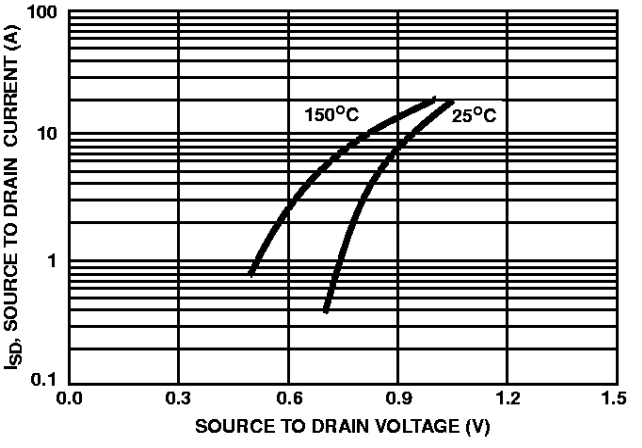


FIGURE 12. SOURCE TO DRAIN DIODE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

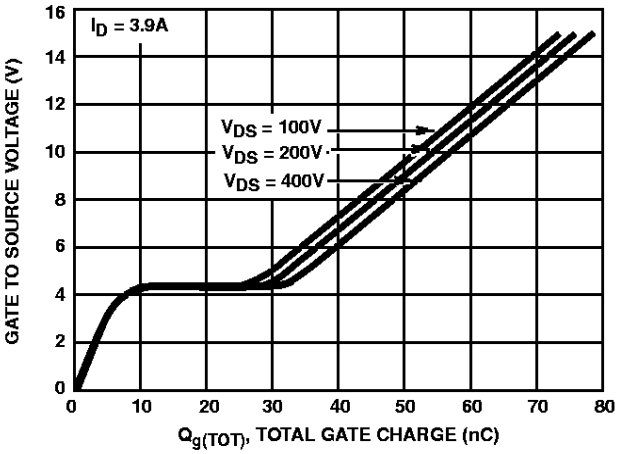


FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

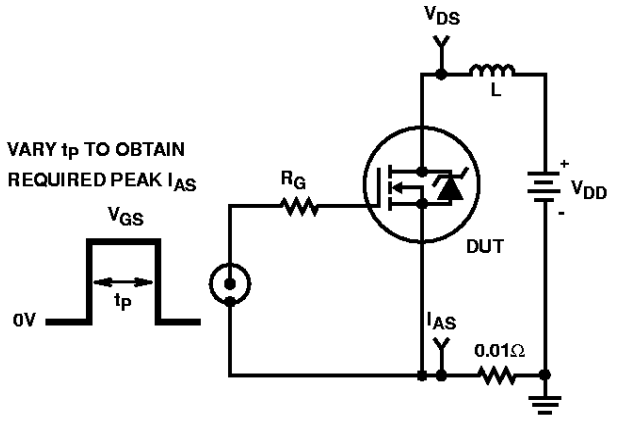


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

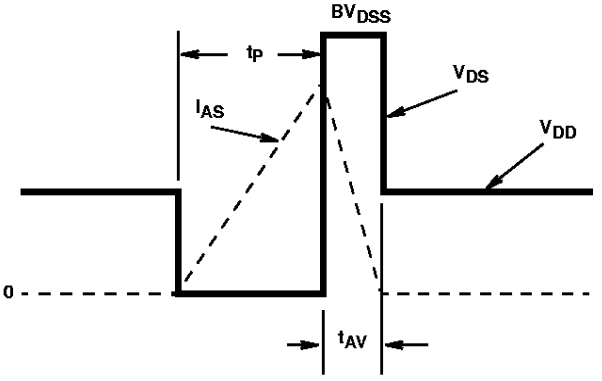


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

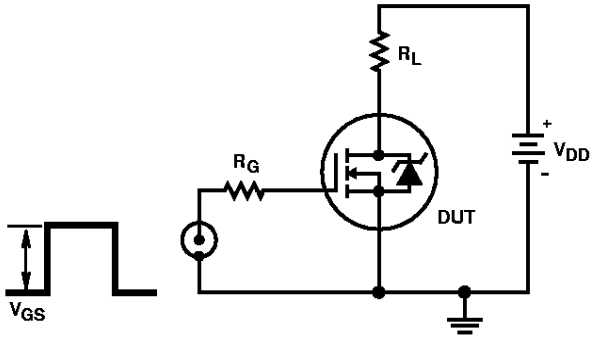


FIGURE 16. SWITCHING TIME TEST CIRCUIT

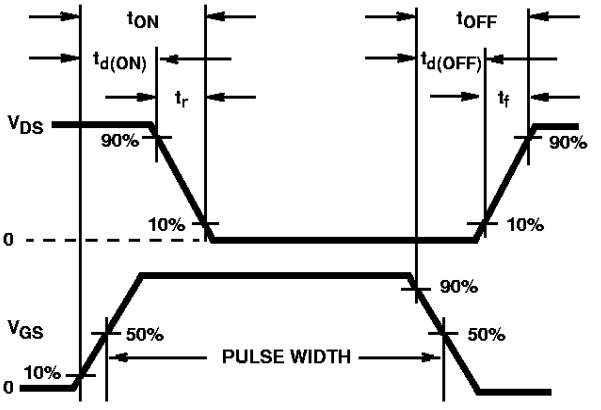


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

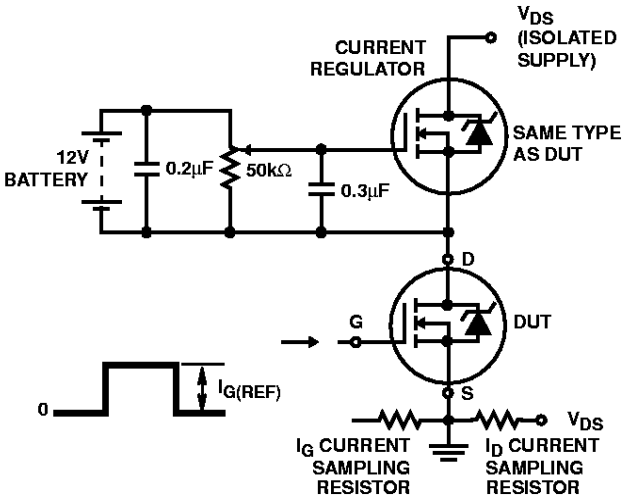


FIGURE 18. GATE CHARGE TEST CIRCUIT

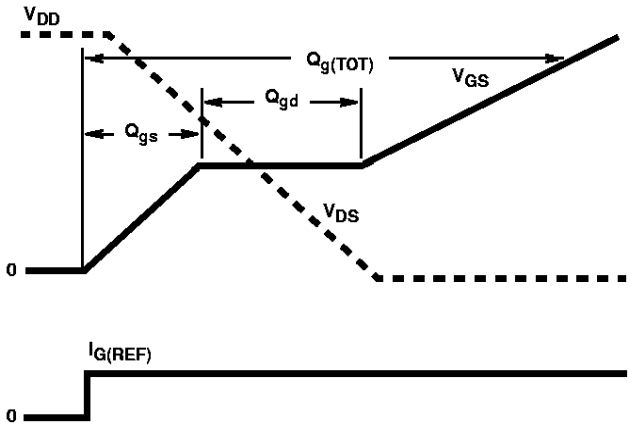


FIGURE 19. GATE CHARGE WAVEFORMS