Rochester Electronics®

Datasheet

54AC11623, 74AC11623

Octal Bus Transceivers with 3-State Outputs

These octal bus transceivers are designed for asynchronous two-way communication between data buses, The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending upon the logic levels at the enable inputs ($\bar{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\bar{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the AC11623.

The 54AC11623 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC11623 is characterized for operation from -40°C to 85°C.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

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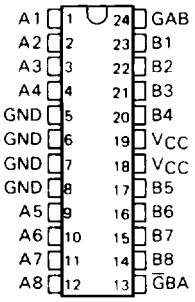
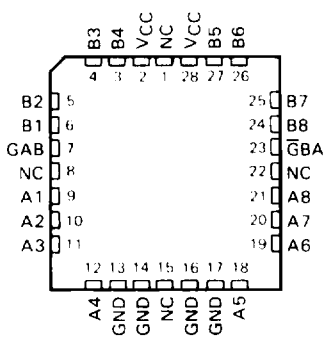
- **Local Bus-Latch Capability**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11623 . . . JT PACKAGE
74AC11623 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11623 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending upon the logic levels at the enable inputs ($\overline{G}BA$ and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of $\overline{G}BA$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the AC11623.

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FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{G}BA$	GAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

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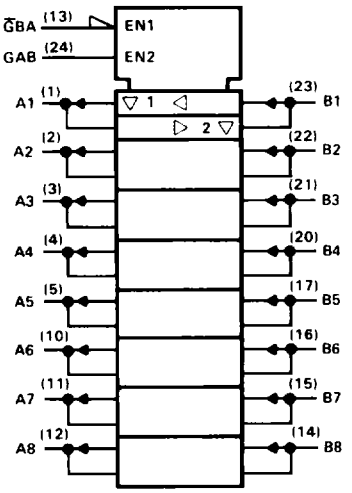
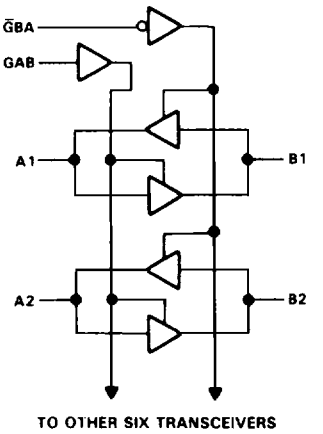
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11623			74AC11623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11623		74AC11623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = −50 mA†	5.5 V				3.85				
		I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports‡	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	$\overline{G}$BA or GAB	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	$\overline{G}$BA or GAB	V_I = V_{CC} or GND	5 V		4						pF
C_{io}	A or B ports	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡For I/O ports, the parameter I_{OZ} includes the input leakage current.

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11623		74AC11623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	6.8	9.2	1.5	11.4	1.5	10.5	ns
t_{PHL}			1.5	6.3	8.2	1.5	10.6	1.5	9.3	
t_{PZH}	$\overline{G}$BA	A	1.5	8	10.6	1.5	13.3	1.5	12.2	ns
t_{PZL}			1.5	7.9	10.4	1.5	12.5	1.5	11.6	
t_{PHZ}	$\overline{G}$BA	A	1.5	7	8.7	1.5	9.7	1.5	9.3	ns
t_{PLZ}			1.5	8	9.9	1.5	11.3	1.5	10.7	
t_{PZH}	GAB	B	1.5	8.2	10.4	1.5	13.2	1.5	12	ns
t_{PZL}			1.5	8.3	10.8	1.5	13.2	1.5	12.2	
t_{PHZ}	GAB	B	1.5	7	8.8	1.5	9.8	1.5	9.4	ns
t_{PLZ}			1.5	8	9.9	1.5	11.1	1.5	10.6	

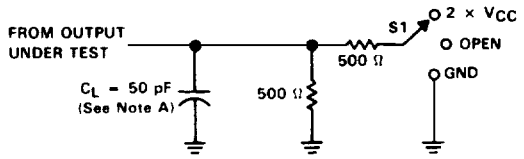
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11623		74AC11623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	4.9	6.8	1.5	8.4	1.5	7.8	ns
t_{PHL}			1.5	4.6	6.4	1.5	7.7	1.5	7.1	
t_{PZH}	$\overline{G}$BA	A	1.5	5.8	7.9	1.5	9.8	1.5	9	ns
t_{PZL}			1.5	5.9	8.1	1.5	9.9	1.5	9.1	
t_{PHZ}	$\overline{G}$BA	A	1.5	6.1	7.7	1.5	8.6	1.5	8.3	ns
t_{PLZ}			1.5	6.6	8.2	1.5	9.3	1.5	8.8	
t_{PZH}	GAB	B	1.5	6.2	8	1.5	10	1.5	9.2	ns
t_{PZL}			1.5	6.1	8.3	1.5	10.2	1.5	9.4	
t_{PHZ}	GAB	B	1.5	6.2	7.8	1.5	8.7	1.5	8.3	ns
t_{PLZ}			1.5	6.5	8.1	1.5	9.2	1.5	8.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

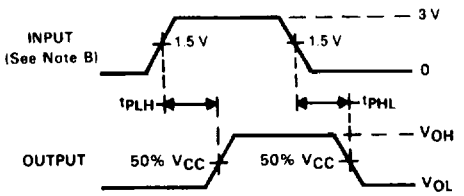
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L 50 pF, f 1 MHz	49	pF
		Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION

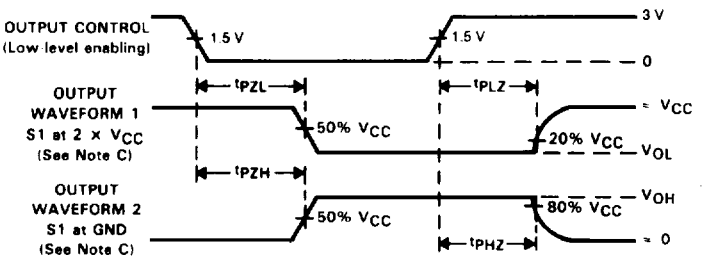


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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