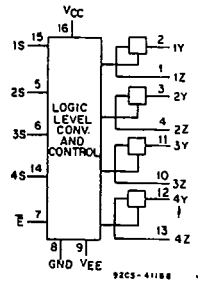
File Number **1916**

CD54/74HC4316
CD54/74HCT4316

T-51-11-00

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad Analog Switch with Level Translation

Type Features:
- *Wide analog-input-voltage range (V_{CC}-V_{EE}): 0-10 V*
- *Low "ON" resistance: 45 Ω typ. @ V_{CC}=4.5 V*
  35 Ω typ. @ V_{CC}=6 V
  30 Ω typ. @ V_{CC}-V_{EE}=9 V
- *Fast switching and propagation delay times*
- *Low "OFF" leakage current*
- *Built-in "Break-before-make" switching*
- *Logic-level translation to enable 5 V logic to accommodate ±5 V analog signals*

The RCA CD54/74HC/HCT4316 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

In addition these devices contain logic-level translation circuits that provide for analog signal switching of voltages between ±5 V via 5 V logic. Each switch is turned on by a high-level voltage on its select input (S) when the common Enable (E) is Low. A High E disables all switches. The digital inputs can swing between V_{CC} and Gnd; the analog inputs/outputs can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. Voltage ranges are shown in Figs. 2 and 3.

The CD54HC4316 and CD54HCT4316 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4316 and CD74HCT4316 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +125° C
- *CD54HC/CD74HC types:*
  2 V to 10 V operation
  High noise immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT types:*
  Direct LSTTL input logic compatibility
  V_{IL} = 0.8 V max., V_{IH} = 2 V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}
- *Alternate Source is Philips/Signetics*

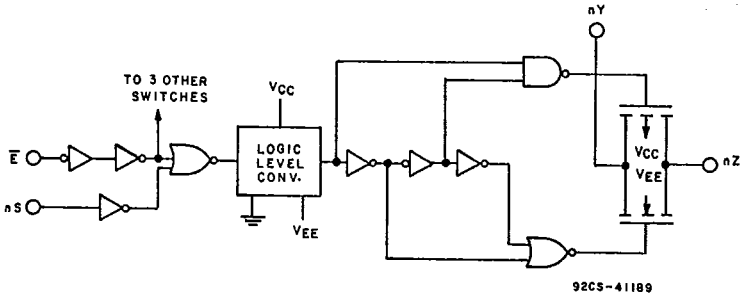


Fig. 1 - Logic diagram (one switch).

TRUTH TABLE

INPUTS		SWITCH
$\overline{E}$	S	
L	L	OFF
L	H	ON
H	X	OFF

H = High Level Voltage
L = Low Level Voltage
X = Don't Care

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MAXIMUM RATINGS, *Absolute-Maximum Values: (All voltages referenced to Gnd unless otherwise shown)*

DC SUPPLY-VOLTAGE (V_{CC}-V_{EE}) ..... -0.5 to +10.5 V
DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to +7 V
DC SUPPLY-VOLTAGE (V_{EE}) ..... +0.5 to -7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC SWITCH DIODE CURRENT, I_{OK} (FOR $V_I < V_{EE}$ -0.5 V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC SWITCH CURRENT (FOR $V_I > V_{EE}$ -0.5 V OR $V_I < V_{CC}$ +0.5 V) ..... +25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±50 mA
DC V_{EE} CURRENT (I_{EE}) ..... -20 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A=Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
Supply-Voltage Range (For T_A=Full Package-Temperature Range) V_{CC}-V_{EE} CD54/74HC Types, CD54/74HCT Types, See Fig. 2	2	10	V
Supply-Voltage Range (For T_A=Full Package-Temperature Range) V_{EE}:* CD54/74HC Types, CD54/74HCT, See Fig. 3	0	-6	V
DC Input Control Voltage, V_I	Gnd	V_{CC}	V
Analog Switch I/O Voltage, V_{IS}	V_{EE}	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+125	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

Recommended Operating Area as a Function of Supply Voltages

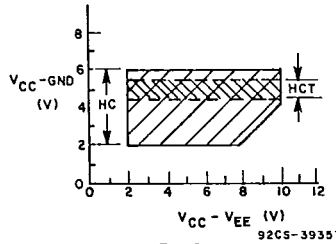

Fig. 2

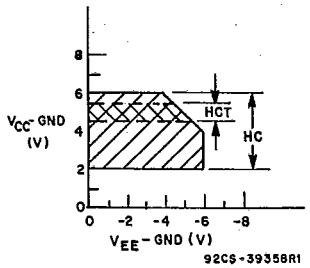

Fig. 3

CD54/74HC4316
CD54/74HCT4316

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS				74HC/54HC			74HC		54HC -55/ +125°C		TEST CONDITIONS				74HCT/54HCT			74HCT		54HCT -55/ +125°C		UNITS
	V_{IS} V	V_I V	V_{EE} V	V_{CC} V	+25°C			-40/ +85°C		74HC -40/ +125°C		V_{IS} V	V_I V	V_{EE} V	V_{CC} V	+25°C			-40/ +85°C		74HCT -40/ +125°C		
					Min	Typ	Max	Min	Max	Min	Max					Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}				2	1.5	—	—	1.5	—	1.5	—				4.5 to 5.5	2	—	—	2	—	2	—	V
				4.5	3.15	—	—	3.15	—	3.15	—												
				6	4.2	—	—	4.2	—	4.2	—												
Low-Level Input Voltage V_{IL}				2	—	—	0.5	—	0.5	—	0.5				4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
				4.5	—	—	1.35	—	1.35	—	1.35												
				6	—	—	1.8	—	1.8	—	1.8												
"On" Resistance I_O = 1 mA R_{on} (Fig. 4 & 5)	V_{CC} or V_{EE}	V_{IL} or V_{IH}	0	4.5	—	45	180	—	225	—	270			0	4.5	—	45	180	—	225	—	270	Ω
			0	6	—	35	160	—	200	—	240			—	—	—	—	—	—	—	—	—	
			-4.5	4.5	—	30	135	—	170	—	205			-4.5	4.5	—	30	135	—	170	—	205	
	V_{CC} to V_{EE}		0	4.5	—	85	320	—	400	—	480			0	4.5	—	85	320	—	400	—	480	Ω
			0	6	—	55	240	—	300	—	360			—	—	—	—	—	—	—	—	—	
			-4.5	4.5	—	35	170	—	215	—	255			-4.5	4.5	—	35	170	—	215	—	255	
Maximum "On" Resistance between any two channels ΔR_{on}			0	4.5	—	10	—	—	—	—	—			0	4.5	—	10	—	—	—	—	—	Ω
			0	6	—	8.5	—	—	—	—	—			—	—	—	—	—	—	—	—	—	
			-4.5	4.5	—	5	—	—	—	—	—			-4.5	4.5	—	5	—	—	—	—	—	
Switch Off Leakage Current I_{IZ}	V_{CC}-V_{EE}	V_{IL} or V_{IH}	0	6	—	—	±0.1	—	±1	—	±1			0	6	—	—	±0.1	—	±1	—	±1	μA
			-5	5	—	—	±0.1	—	±1	—	±1			-5	5	—	—	±0.1	—	±1	—	±1	
Control Input Leakage Current I_{IL}	—	V_{CC} or Gnd	0	6	—	—	±0.1	—	±1	—	±1	—	**		5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC} I_O = 0	When V_{IS} = V_{EE}, V_{OS} = V_{CC}, When V_{IS} = V_{CC}, V_{OS} = V_{EE}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	Same as HC	Same as HC	0	5.5	—	—	8	—	80	—	160	μA
			-5	5	—	—	16	—	160	—	320			-4.5	5.5	—	—	16	—	160	—	320	
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*													V_{CC}-2.1		4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

**Any voltage between V_{CC} and Gnd.

HCT Input Loading Table

Input	Unit Loads*
All	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r,t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES HC	TYPICAL VALUES HCT	UNITS
Turn "ON" Time	$\overline{E}$ to Out	t_{PZH}	17	18	ns
	nS to Out		14	17	
Turn "ON" Time	$\overline{E}$ to Out	t_{PZL}	17	24	
	nS to Out		14	18	
Turn "OFF" Time	$\overline{E}$ to Out	t_{PLZ}, t_{PHZ}	17	21	
	nS to Out		14	18	
Power Dissipation Capacitance*		C_{PD}	42	47	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where

f_i = input frequency

f_o = output frequency

C_L = output load capacitance

C_S = switch capacitance

V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC		V_{EE}	V_{CC}	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay	t_{PLH}	0	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
Switch In to Out	t_{PHL}	0	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		0	6	—	10	—	—	—	13	—	—	—	15	—	—	
		-4.5	4.5	—	8	—	8	—	10	—	10	—	12	—	12	
Turn "ON" Time	t_{PZH}	0	2	—	205	—	—	—	255	—	—	—	310	—	—	
$\overline{E}$ to Out		0	4.5	—	41	—	44	—	51	—	55	—	62	—	66	
		0	6	—	35	—	—	—	43	—	—	—	53	—	—	
		-4.5	4.5	—	37	—	42	—	47	—	53	—	56	—	63	
	t_{PZL}	0	2	—	205	—	—	—	255	—	—	—	310	—	—	
		0	4.5	—	41	—	56	—	51	—	70	—	62	—	85	
		0	6	—	35	—	—	—	43	—	—	—	53	—	—	
		-4.5	4.5	—	37	—	42	—	47	—	53	—	56	—	63	
Turn "ON" Time	t_{PZH}	0	2	—	175	—	—	—	220	—	—	—	265	—	—	
nS to Out		0	4.5	—	35	—	40	—	44	—	53	—	53	—	60	
		0	6	—	30	—	—	—	37	—	—	—	45	—	—	
		-4.5	4.5	—	34	—	34	—	43	—	43	—	51	—	51	
	t_{PZL}	0	2	—	175	—	—	—	220	—	—	—	265	—	—	
		0	4.5	—	35	—	50	—	44	—	63	—	53	—	75	
		0	6	—	30	—	—	—	37	—	—	—	45	—	—	
		-4.5	4.5	—	34	—	34	—	43	—	43	—	51	—	51	
Turn "OFF" Time		0	2	—	205	—	—	—	255	—	—	—	310	—	—	
$\overline{E}$ to Out		0	4.5	—	41	—	50	—	51	—	63	—	62	—	75	
		0	6	—	35	—	—	—	43	—	—	—	53	—	—	
	t_{PLZ},	-4.5	4.5	—	37	—	46	—	47	—	58	—	56	—	69	
Turn "OFF" Time	t_{PHZ}	0	2	—	175	—	—	—	220	—	—	—	265	—	—	
nS to Out		0	4.5	—	35	—	44	—	44	—	55	—	53	—	66	
		0	6	—	30	—	—	—	37	—	—	—	45	—	—	
		-4.5	4.5	—	34	—	40	—	43	—	50	—	51	—	60	
Input (Control) Capacitance	C_I	—	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

ANALOG CHANNEL CHARACTERISTICS - Typical Values at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS	V_{CC} V	HC	HCT	UNITS
Switch Frequency Response Bandwidth at -3 dB (Fig. 15)	Fig. 6 Notes 1 and 2	4.5	>200	>200	MHz
Crosstalk Between Any Two Switches (Fig. 16)	Fig. 7 Notes 2 and 3	4.5	TBE	TBE	dB
Total Harmonic Distortion	1 kHz, V_{IS}=4 V_{pp}	4.5	0.078	0.078	%
	Fig. 8 V_{IS}=8 V_{pp}	9	0.018	0.018	
Control to Switch Feedthrough Noise	Fig. 9	4.5	TBE	TBE	mV
		9	TBE	TBE	
Switch "OFF" Signal Feedthrough (Fig. 16)	Fig. 10 Notes 2 and 3	4.5	-62	-62	dB
Switch Input Capacitance Cs	—	—	5	5	pF

Notes:

1. Adjust input level for 0 dBm at output, f = 1 MHz.
2. V_{IS} is centered at $V_{CC}/2$.
3. Adjust input for 0 dBm at V_{IS}.

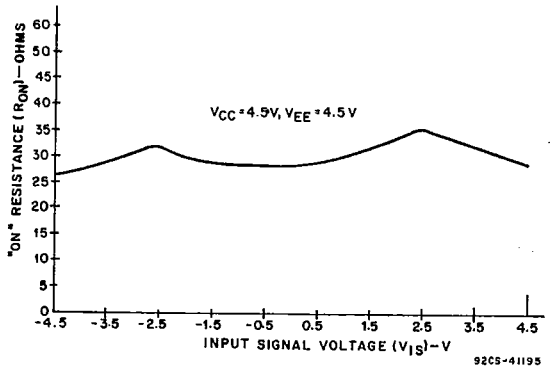

Fig. 4 - Typical "ON" resistance vs. input signal voltage.

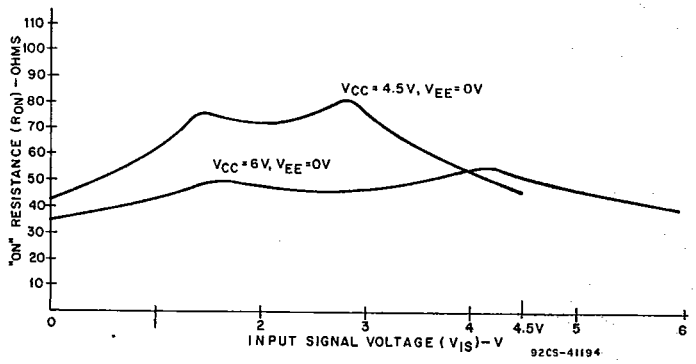

Fig. 5 - Typical "ON" resistance vs. input signal voltage.

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ANALOG TEST CIRCUITS

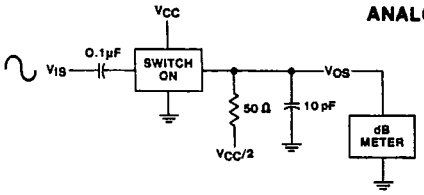


Fig. 6 - Frequency response test circuit.

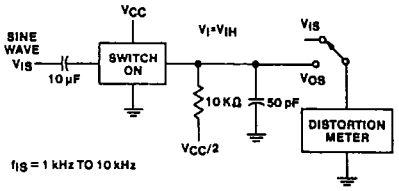


Fig. 8 - Total harmonic distortion test circuit.

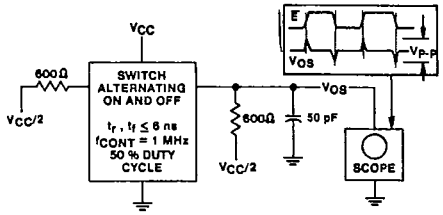


Fig. 9 - Control-to-switch feedthrough noise test circuit.

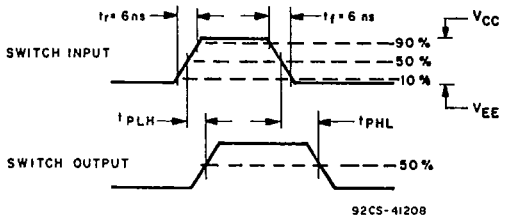
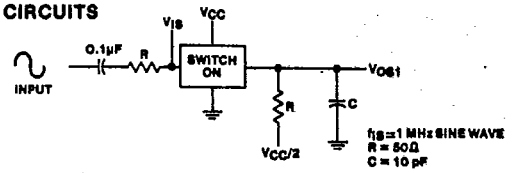


Fig. 11 - Switch propagation - delay times waveforms.



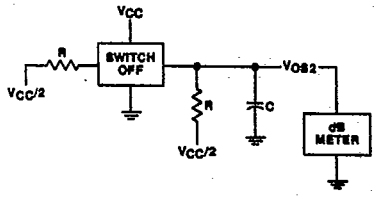


Fig. 7 - Crosstalk between two switches test circuit.

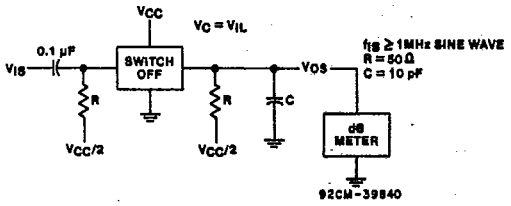


Fig. 10 - Switch off signal feedthrough.

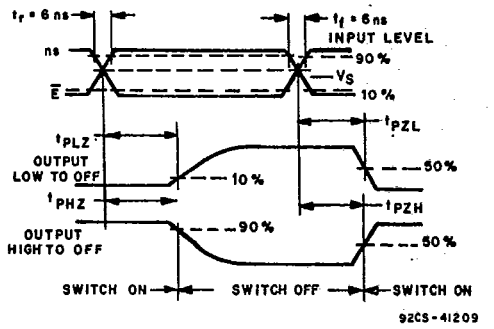


Fig. 12 - Switch turn-on and turn-off propagation delay times waveforms.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

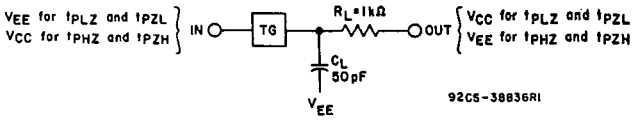


Fig. 13 - Switch on/off propagation delay time test circuit.

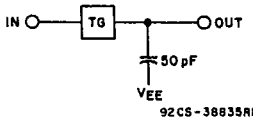


Fig. 14 - Switch-in to switch-out propagation delay time test circuit.

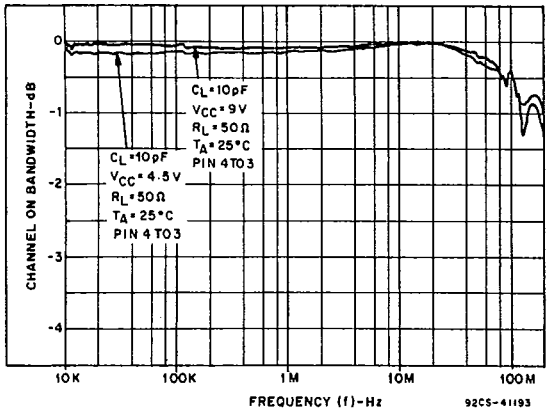


Fig. 15 - Switch frequency response.

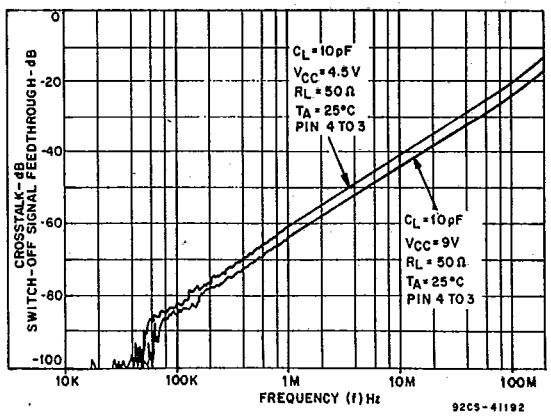


Fig. 16 - Switch-off signal feedthrough and crosstalk vs. frequency.