

JFET Input Operational Amplifiers

These low cost JFET input operational amplifiers combine two state-of-the-art analog technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The JFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices.

Input Offset Voltage of 5.0 mV Max (LF347B)

• Low Input Bias Current: 50 pA

 Low Input Noise Voltage: 16 nV/√Hz • Wide Gain Bandwidth: 4.0 MHz

• High Slew Rate: 13V/us

• Low Supply Current: 1.8 mA per Amplifier

High Input Impedance: 10¹² Ω

High Common Mode and Supply Voltage Rejection Ratios: 100 dB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	+18	V
	VEE	-18	
Differential Input Voltage	V _{ID}	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	V
Output Short Circuit Duration (Note 2)	t _{SC}	Continuous	
Power Dissipation at T _A = +25°C	P _D	900	mW
Derate above T _A =+25°C	1/ _{0JA}	10	mW/°C
Operating Ambient Temperature Range	T _A	0 to +70	°C
Operating Junction Temperature Range	T _J	115	°C
Storage Temperature Range	T _{stg}	- 65 to	°C
		+150	

NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is limited to the negative power supply.

2. Any amplifier output can be shorted to ground indefinitely. However, if more than one amplifier output is shorted simultaneously, maximum junction temperature rating may be exceeded.

LF347, B LF351 LF353

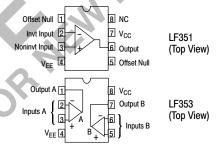
FAMILY OF JFET OPERATIONAL AMPLIFIERS



N SUFFIX PLASTIC PACKAGE **CASE 626**



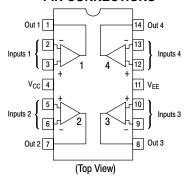
PIN CONNECTIONS





N SUFFIX PLASTIC PACKAGE CASE 646

PIN CONNECTIONS



ORDERING INFORMATION

Device	Function	Operating Temperature Range	Package
LF351D LF351N	Single Single	T _A = 0° to +70°C	SO-8 Plastic DIP
LF353D LF353N	Dual Dual		SO–8 Plastic DIP
LF347BN LF347N	Quad Quad		Plastic DIP Plastic DIP

LF347, B LF351 LF353

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V_{EE} = -15 V, T_A = 25°C, unless otherwise noted.)

			LF347B		LF347	7, LF351, I	LF353	
Characteristic	Symbol	Min	Тур	Max	Min	Тур	Max	Unit
Input Offset Voltage (R _S \leq 10 k, V _{CM} = 0) T _A = +25°C 0°C \leq T _A \leq +70°C	V _{IO}	- -	1.0	5.0 8.0	- -	5.0 –	10 13	mV
Avg. Temperature Coefficient of Input Offset Voltage $R_S \le 10 \text{ k}, \ 0^{\circ}\text{C} \le T_A \le +70^{\circ}\text{C}$	$\Delta V_{IO}/\Delta T$	_	10	_	_	10	_	μV/°C
Input Offset Current ($V_{CM} = 0$, Note 3) $T_A = +25^{\circ}C$ $0^{\circ}C \le T_A \le +70^{\circ}C$	I _{IO}	_ _	25 -	100 4.0	-	25 -	100 4.0	pA nA
Input Bias Current ($V_{CM} = 0$, Note 3) $T_A = +25^{\circ}C$ $0^{\circ}C \le T_A \le +70^{\circ}C$	I _{IB}	- -	50 -	200 8.0	- -	50 -	200 8.0	pA nA
Input Resistance	rį	_	10 ¹²	_	_	10 ¹²		Ω
Common Mode Input Voltage Range	V _{ICR}	±11	+15 -12	_	±11	+15 -12		V
Large–Signal Voltage Gain ($V_O = \pm 10 \text{ V}$, $R_L = 2.0 \text{ k}$) $T_A = +25^{\circ}\text{C}$ $0^{\circ}\text{C} \le T_A \le +70^{\circ}\text{C}$	A _{VOL}	50 25	100	2	25 15	100 -	_ _	V/mV
Output Voltage Swing (R _L = 10 k)	Vo	±12	±14	-	±12	±14	_	V
Common Mode Rejection (R _S ≤ 10 k)	CMR	80	100	-	70	100	_	dB
Supply Voltage Rejection (R _S ≤ 10 k)	PSRR	80	100	(2)	70	100	-	dB
Supply Current LF347 LF351 LF353	ID	<u>-</u>	7.2 - -) ₁₁ - -	- - -	7.2 1.8 3.6	11 3.4 6.5	mA
Short Circuit Current	I _{SC}	-	25	_	_	25	-	mA
Slew Rate (A _V = +1)	SR		13	_	_	13	-	V/μs
Gain-Bandwidth Product	BWp		4.0	_	_	4.0	_	MHz
Equivalent Input Noise Voltage $(R_S = 100 \Omega, f = 1000 Hz)$	e _n	_	24	_	-	24	-	nV/√Hz
Equivalent Input Noise Current (f = 1000 Hz)	i _n	-	0.01	_	_	0.01	_	pA/√Hz
Channel Separation (LF347, LF353) 1.0 Hz ≤ f ≤ 20 kHz (Input Referred)	_	-	-120	-	-	-120	-	dB

For Typical Characteristic Performance Curves, refer to MC34001, 34002, 34004 data sheet.

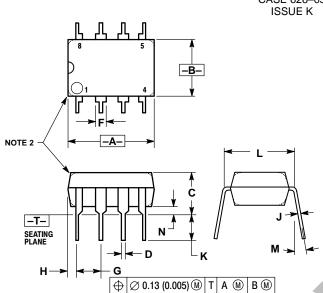
OEVICE NO

NOTE: 3. Input bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature. To maintain junction temperatures as close to ambient as is possible, pulse techniques are utilized during test.

OUTLINE DIMENSIONS

N SUFFIX

PLASTIC PACKAGE CASE 626-05

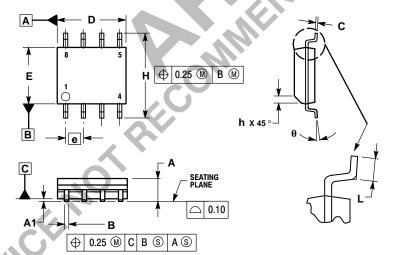


NOTES:

- (OLES: 1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL. 2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS). 3. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	9.40	10.16	0.370	0.400	
В	6.10	6.60	0.240	0.260	
O	3.94	4.45	0.155	0.175	
D	0.38	0.51	0.015	0.020	
F	1.02	1.78	0.040	0.070	
G	2.54 BSC		0.100 BSC		
Ŧ	0.76	1.27	0.030	0.050	
_	0.20	0.30	0.008	0.012	
K	2.92	3.43	0.115	0.135	
L	7.62 BSC		0.300 BSC		
M		10°		10°	
N	0.76	1.01	0.030	0.040	





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. DIMENSIONS ARE IN MILLIMETERS.
- 3. DIMENSION D AND E DO NOT INCLUDE MOLD
- DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS				
DIM	MIN	MAX			
Α	1.35	1.75			
A1	0.10	0.25			
В	0.35	0.49			
С	0.18	0.25			
D	4.80	5.00			
E	3.80	4.00			
е	1.27	BSC			
Н	5.80	6.20			
h	0.25	0.50			
L	0.40	1.25			
θ	0°	7°			

LF347, B LF351 LF353

OUTLINE DIMENSIONS

NOTES:

- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE
 POSITION AT SEATING PLANE AT MAXIMUM
 MATERIAL CONDITION.
- 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- 4. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.715	0.770	18.16	19.56	
В	0.240	0.260	6.10	6.60	
С	0.145	0.185	3.69	4.69	
D	0.015	0.021	0.38	0.53	
F	0.040	0.070	1.02	1.78	
G	0.100 BSC		2.54 BSC		
Н	0.052	0.095	1.32	2.41	
ſ	0.008	0.015	0.20	0.38	
K	0.115	0.135	2.92	3.43	
L	0.300 BSC		7.62 BSC		
M	٥°	10°	0°	10°	
N	0.015	0.039	0.39	1.01	

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