

M62362P/FP

R03DS0044EJ0300 Rev.3.00 Jun 03, 2011

1280 Resolution 3ch Multiplying D/A Converter

Description

The M62362P is an integrated circuit semiconductor of CMOS structured with 3 channels of built-in 1280 step resolution (equivalent 10.3-bit) multiplication type D/A converters.

The 3-wire serial interface method and it is able to cascading serial use with Do terminal.

The device is suited for use in high accuracy automatic adjustment combination with microcomputer.

Features

- Digital data transfer method: 3-wire serial data transfer method
- High resolution Resolution is more over 10-bit and error is less than ±1 LSB
- Capable of 4 quadrant multiplication
- Short setting time
- With reset terminal

Recommended Operating Condition

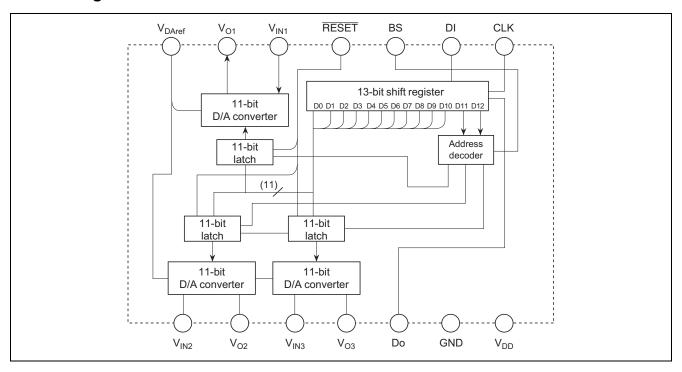
Digital section supply voltage: $V_{DD} = 5 \text{ V} \pm 10\%$

Application

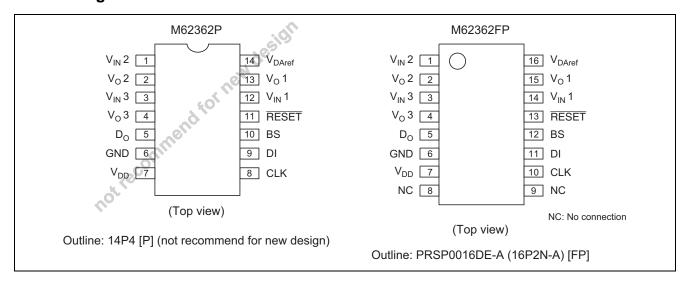
Signal gain control of display-monitor or CTV. Conversion from digital control data to analog control data for home-use and industrial equipment.

Automatic adjustment by combination with EEPROM and microcomputer. (Replacement of conventional half-fixed)

Block Diagram



Pin Arrangement

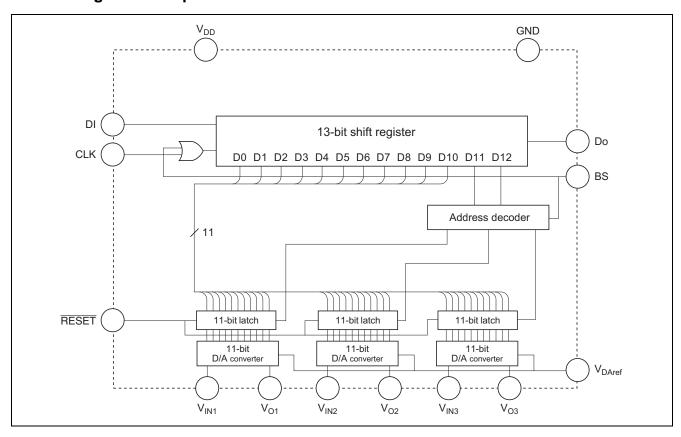


Pin Description

Pin No.	Pin Name	Function					
9 (11)	DI	Serial data input terminal					
5	Do	Serial data output terminal					
8 (10)	CLK	Serial clock input terminal					
10 (12)	BS	When BS terminal level is "H" latch circuit data is load					
11 (13)	RESET	When RESET terminal level is "L", all D/A output terminal became "L"					
13 (15)	V _{O1}	1280 resolution D/A output					
2	V _{O2}						
4	V _{O3}						
7	V_{DD}	Power supply terminal					
6	GND	GND terminal					
1	V _{IN2}	D/A converter input terminal					
3	V _{IN3}						
12 (14)	V _{IN1}						
14 (16)	V _{DAref}	D/A converter reference voltage input terminal					

Note: (): M62362FP

Block Diagram for Explanation of Terminals



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{DD}	-0.3 to +7.0	V
Digital input voltage (DI, CLK, BS)	V _{IND}	-0.3 to +7.0	V
Input voltage	V _{IN}	-0.3 to V _{DD} + 0.3	V
Output voltage	Vo	-0.3 to V _{DD} + 0.3	V
D/A reference voltage	V _{DAref}	-0.3 to V _{DD} + 0.3	V
Operating temperature	Topr	-20 to +85	°C
Storage temperature	Tstg	-40 to +125	°C

Electrical Characteristics

<Digital Part>

 $(V_{DD},\,V_{IN}=+5\,\,V\pm10\%,\,V_{DD}\geq V_{IN},\,GND=V_{DAref}=0\,\,V,\,Ta=-20\,\,to\,\,+85^{\circ}C,\,unless\,\,otherwise\,\,noted.)$

			Limits			
Item	Symbol	Min	Тур	Max	Unit	Conditions
Supply voltage	V_{DD}	4.5	5.0	5.5	V	
Input leak current	I _{ILK}	-10	1	10	μΑ	$V_{IN} = 0$ to V_{DD}
Input low voltage	V _{IL}	_	1	$0.2\ V_{DD}$	V	
Input high voltage	V _{IH}	0.8 V _{DD}	1	1	V	
Output low voltage	V _{OL}	_	1	0.4	V	I _{OL} = 2.5 mA
Output high voltage	V _{OH}	$V_{DD} - 0.4$	_	_	V	I _{OH} = -400 μA

<Analog Part>

 $(V_{DD},\,V_{IN}=+5\,\,V\pm10\%,\,V_{DD}\geq V_{IN},\,GND=V_{DAref}=0\,\,V,\,Ta=-20\,\,to\,\,+85^{\circ}C,\,unless\,\,otherwise\,\,noted.)$

				Limits			
Item		Symbol	Min	Тур	Max	Unit	Conditions
Input voltage		V _{IN}	0	_	V_{DD}	V	
Out	tput voltage	Vo	0	_	V_{DD}	V	$V_{IN} = 0$ to V_{DD}
Inp	ut current	I _{IN}	_	0.75	1.5	mA	$V_{IN} = 5 \text{ V}, V_{DAref} = 0 \text{ V}$
							Proportional to (V _{IN} – V _{DAref})
D/A	reference source current	I _{DAref}	-4.5	-2.25	_	mA	$V_{IN1} = V_{IN2} = V_{IN3} = 5 V,$
							$V_{DAref} = 0 V$
							Proportional to (V _{IN} – V _{DAref})
D/A	output sink or source	lo	-1.0	_	1.0	μA/LSB	
cur	rent						
Out	tput impedance	Ro	_	1.8	3.6	kΩ	Constant for all D/A output mode
Resolution		RES	_	1280	_	STEP	
5	Differential nonlinearity	DNL	-1	_	1	LSB	
Nonlinearity Nonlinearity		NL	-0.6	_	0.6	%FS	
Nonlinearity for channels		ΔNL	-0.4	_	0.4	%FS	

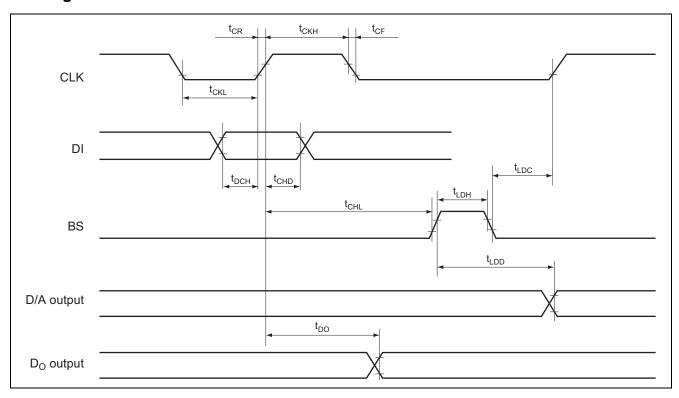
Note: Polarity of current, (+) is sink into IC and (-) is source from IC.

AC Characteristics

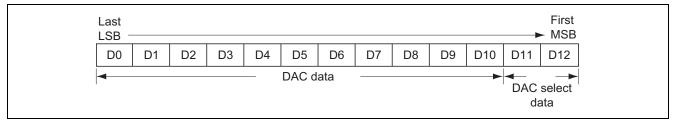
(V_DD, V_IN = +5 V \pm 10%, V_DD \geq V_IN, GND = V_DAref = 0 V, Ta = -20 to +85°C)

		Limits				
Item	Symbol	Min	Тур	Max	Unit	Conditions
Clock "L" pulse width	t _{CKL}	200	_	_	ns	
Clock "H" pulse width	t _{CKH}	200	_	_	ns	
Clock rise time	t _{CR}	_	_	200	ns	
Clock fall time	t _{CF}	_	_	200	ns	
Data setup time	t _{DCH}	60	_	_	ns	
Data hold time	t _{CHD}	100	_	_	ns	
LD setup time	t _{CHL}	200	_	_	ns	
LD hold time	t _{LDC}	100	_	_	ns	
LD "H" pulse width	t _{LDH}	100	_	_	ns	
Data output delay time	t _{DO}	70	_	350	ns	C _L ≤ 100 pF
Data output setting time	t _{LDD}	_	_	20	μS	No load
Input/output response time		_	_	5		f = 10 kHz

Timing Chart



Digital Data Format



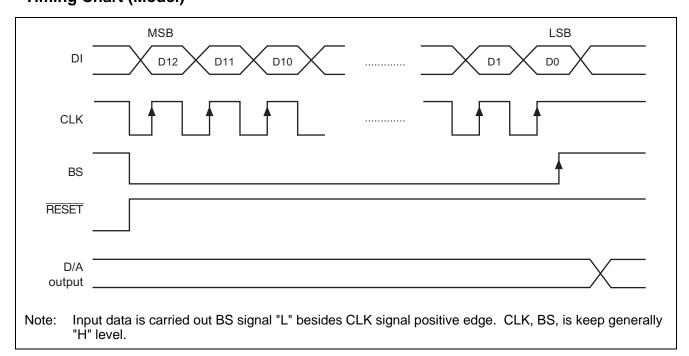
DAC Data

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D/A Output
0	0	0	0	0	0	0	0	0	0	0	V _{DAref}
1	0	0	0	0	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 1280 \times 1 + V_{DAref}$
0	1	0	0	0	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 1280 \times 2 + V_{DAref}$
1	1	0	0	0	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 1280 \times 3 + V_{DAref}$
:	:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	0	0	1	$(V_{IN} - V_{DAref}) / 1280 \times 1279 + V_{DAref}$
0	0	0	0	0	0	0	0	1	0	1	V _{IN}
:	:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	1	1	V _{IN}

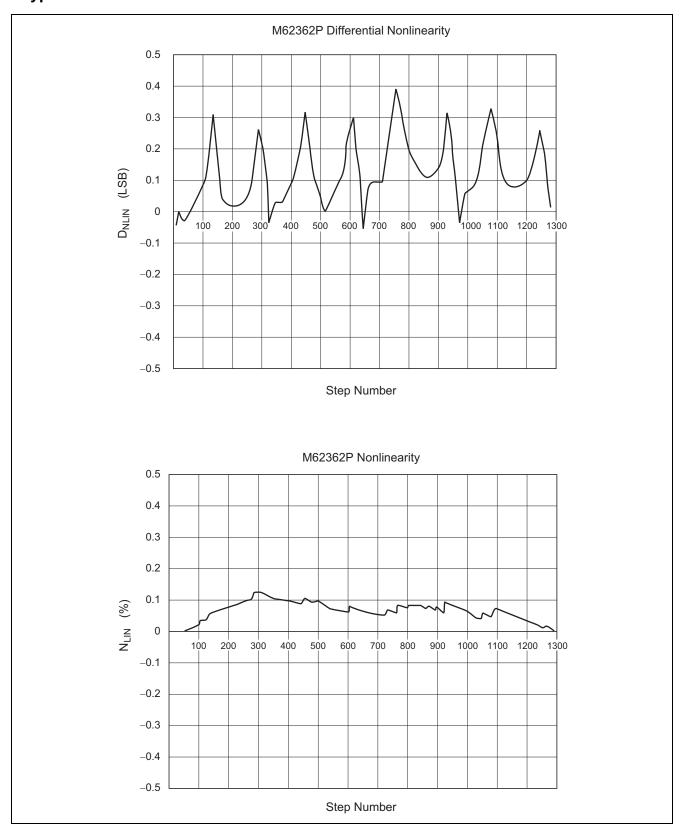
DAC Select Data

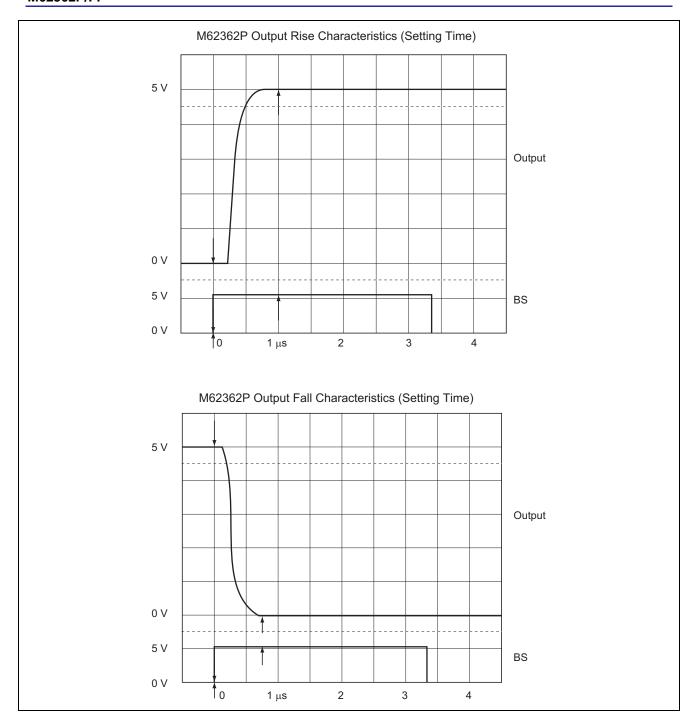
D11	D12	DAC Selection
0	0	Don't care
0	1	ch1
1	0	ch2
1	1	ch3

Timing Chart (Model)



Typical Characteristics

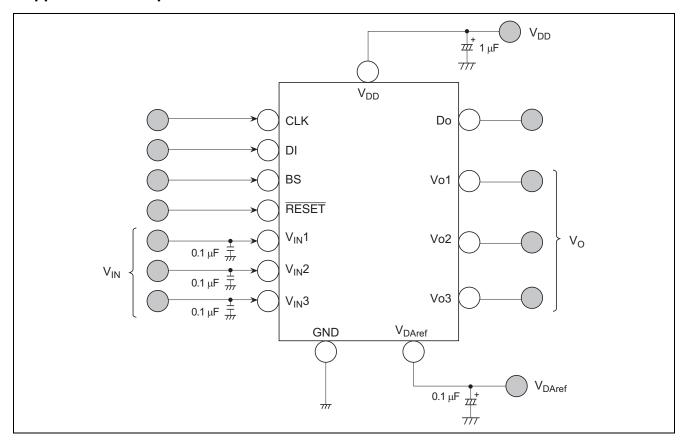




Precaution for Use

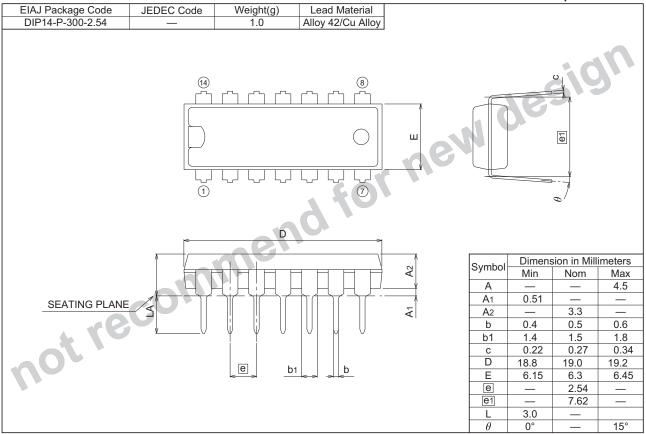
M62362 have 5 terminals these are input free voltage at use. $(V_{DD}, V_{IN1}, V_{IN2}, V_{IN3}, V_{DAref})$ If ripple and spike is input to these terminals, accuracy of conversion is down. So, when use this device, please connect capacitor among to each terminals and GND for stable operation.

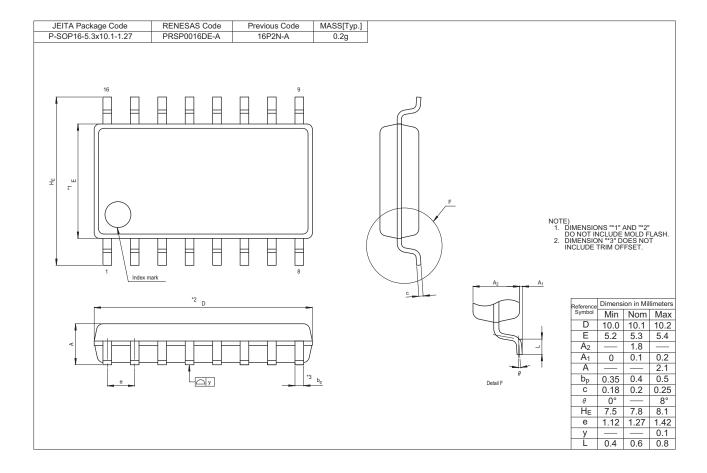
Application Example



Package Dimensions

14P4 Plastic 14pin 300mil DIP





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