LM2650 Synchronous Step-Down DC/DC Converter

Check for Samples: LM2650

FEATURES

- **Ultra High Efficiencies (95% possible)**
- **High Efficiency Over a 3A to Milliamperes Load Range**
- **Synchronous Switching of Internal NMOS Power FETs**
- **Wide Input Voltage Range (4.5V to 18V)**
- **Output Voltage Adjustable from 1.5V to 16V**
- **Automatic Low-Power Sleep Mode**
- **Logic-Controlled Micropower Shutdown (I_{QSD} ≤ 25 µA)**
- **Frequency Adjustable up to 300 kHz**
- **Frequency Synchronization with External Signal**
- **Programmable Soft-Start**
- **Short-Circuit Current Limiting**
- **Thermal Shutdown**
- **Available in 24-lead Small-Outline Package**

APPLICATIONS

- **Notebook and Palmtop Personal Computers**
- **Portable Data Terminals**
- **Modems**
- **Portable Instruments**
- **Global Positioning Devices (GPSs)**
- **Battery-Powered Digital Devices**

DESCRIPTION

The LM2650 is a step-down DC/DC converter featuring high efficiency over a 3A to milliamperes load range. This feature makes the LM2650 an ideal fit in battery-powered applications that demand long battery life in both run and standby modes.

The LM2650 also features a logic-controlled shutdown mode in which it draws at most 25µA from the input power supply.

The LM2650 employs a fixed-frequency pulse-width modulation (PWM) and synchronous rectification to achieve very high efficiencies. In many applications, efficiencies reach 95%+ for loads around 1A and exceed 90% for moderate to heavy loads from 0.2A to 2A.

A low-power hysteretic or "sleep" mode keeps efficiencies high at light loads. The LM2650 enters and exits sleep mode automatically as the load crosses "sleep in" and "sleep out" thresholds. The LM2650 provides nodes for programming both thresholds via external resistors. A logic input allows the user to override the automatic sleep feature and keep the LM2650 in PWM mode regardless of the load level.

An optional soft-start feature limits current surges from the input power supply at start up and provides a simple means of sequencing multiple power supplies.

Typical Application

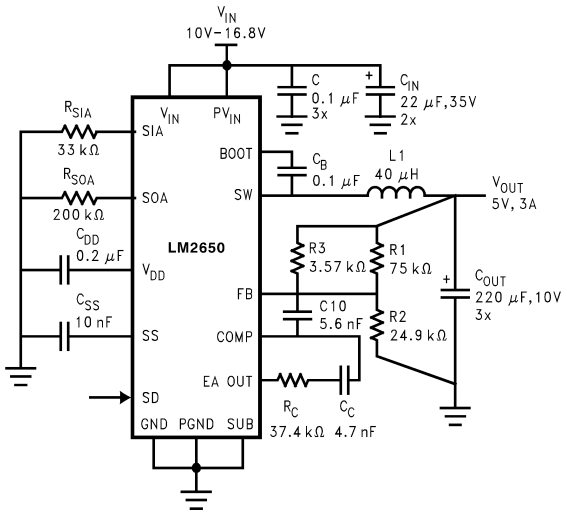


Figure 1. Converting a Four-Cell Li Ion Battery to 5V

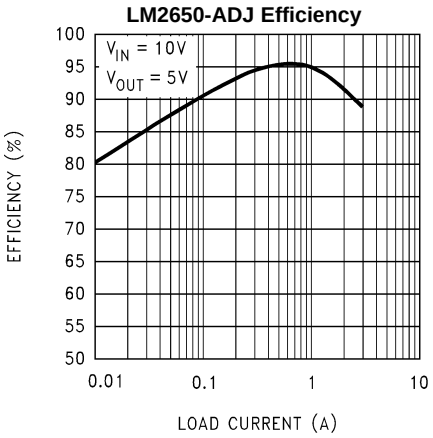


Figure 2.

Connection Diagram

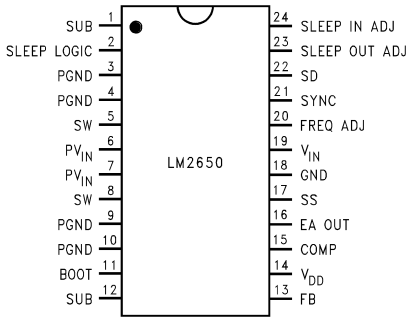


Figure 3. Top View
24-Lead Small Outline Package (DW)
See Package Number DW0024B

PIN DESCRIPTIONS(1)

Pins	Description
1, 12	**SUB**: These pins make electrical contact with the substrate of the die. Ground them. For best thermal performance, ground them to the same large, uninterrupted copper plane as the PGND pins.
2	**SLEEP LOGIC**: Use this logic input to select the conversion mode; low selects PWM, high selects sleep, and high impedance (open) permits the LM2650 to move freely and automatically between the modes, using PWM for moderate to heavy loads and sleep for light loads.
3, 4, 9, 10	**PGND**: The ground return of the power stage. The power stage consists of the two power switches Q1 and Q2, the gate drivers DH and DL, and the linear voltage regulators VRegH and VRegL. For best electrical and thermal performance, ground these pins to a large, uninterrupted copper plane.
5, 8	**SW**: The output node of the power stage. It swings from slightly below ground to slightly below the voltage to PV_{IN}. To minimize the effects of switching noise on nearby circuitry, keep all traces originating from SW short and to the point. Route all traces carrying signals well away from the SW traces.
6, 7	**PV_{IN}**: The positive supply rail of the power stage. Bypass each PV_{IN} pin to PGND with a 0.1 µF capacitor. Use capacitors having low ESL and low ESR, and locate them close to the IC.
11	**BOOT**: The positive supply rail of the high-side gate driver DH. Connect a 0.1 µF capacitor from this node to SW. Bootstrapping action creates a supply rail about 9V above that at PV_{IN}, and DH uses this rail to override the gate of the NMOS power FET Q1. Overriding ensures low $R_{DS(on)}$.
13	**FB**: The feedback input.
14	**V_{DD}**: An internal regulator steps the input voltage down to a 4V rail used by the signal-level circuitry. V_{DD} is the output node of this regulator. Bypass V_{DD} to GND close to the IC with a 0.2 µF capacitor.
15	**COMP**: The inverting input of the error amplifier EA.
16	**EA OUT**: The output node of the error amplifier EA.
17	**SS**: The soft start node. Connect a capacitor from SS to GND.
18	**GND**: The ground return of the signal-level circuitry.
19	**V_{IN}**: The positive supply rail of the internal 4V regulator. Bypass V_{IN} to GND close to the IC with a 0.1 µF capacitor.
20	**FREQ ADJ**: The LM2650 switches at a nominal 90 kHz. Connect a resistor between FREQ ADJ and GND to adjust the frequency up from the nominal. Use the graph under Typical performance Characteristics to select the resistor.
21	**SYNC**: The synchronization input. If the switching frequency is to be synchronized with an external clock signal, apply the clock signal here. Ground if not used.
22	**SD**: Use this logic input to control shutdown; pull low for operation, high for shutdown.
23	**SLEEP OUT ADJ (SOA)**: The value of the resistor connected between SIA and ground programs the sleep-in threshold. Higher values program lower thresholds.
24	**SLEEP IN ADJ (SIA)**: The value of the resistor connected between SIA and ground programs the sleep-in threshold. Higher values program lower thresholds.

(1) Refer to the Block Diagrams.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

(All voltages are referenced to the PGND and GND pins.)		
DC Voltage at PV_{IN} and V_{IN}		20V
DC Voltage at SD, SLEEP LOGIC and SYNC		15V
DC current into SW		±7.5A
Junction Temperature		Limited by the IC
DC Power Dissipation[3]		1.28W
Storage Temperature		−65°C to +150°C
Soldering Time, Temperature[4]	Wave (4 seconds)	260°C
	Infrared (10 seconds)	240°C
	Vapor Phase (75 seconds)	219°C
ESD Susceptibility[5]		1.3 kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which the device operates correctly. Operating ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) This rating is calculated using the formula $P_{DCmax} = (T_{Jmax} - T_A) / \theta_{JA}$, where P_{DCmax} is the absolute maximum power dissipation, T_{Jmax} is the maximum junction temperature, and θ_{JA} is the junction ot ambient thermal resistance of the package. The P_{DCmax} rating of 1.28W results from substituting 170°C, 70°C and 78°C/W for T_{Jmax}, T_A and θ_{JA} respectively. A $\theta_{JA}$of 78°C represents the worst condition of no heat sinking of the DW0024B small-outline package. Heat sinking allows the safe dissipation of more power. See Application Notes on thermal management. The LM2650 actively limits its junction temperature to about 170°C.
(4) For detailed information on soldering plastic small-outline packages, refer to the Packaging Databook published by Texas Instruments.
(5) ESD is applied using the human-body model, a 100pF capacitor discharged through a 1.5kΩ resistor.

Operating Ratings[1]

Supply Voltage Range (PV_{IN} and V_{IN})	4.5V to 18V
Junction Temperature Range	−40°C to +125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which the device operates correctly. Operating ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics.

Electrical Characteristics

V_{PVIN} = 15V, $V_{SLEEP\ LOGIC}$ = 0V and V_{SD} = 0V unless superseded under **Conditions**. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25°C. Limits appearing in **boldface** type apply over the full junction temperature range shown under **Operating Ratings**.

Symbol	Parameter	Conditions	Typ[1]	Limit[2]	Units
V_{OUT}	Output Voltage	R1 = 75 kΩ, 1%, R2 = 25 kΩ, 1%, 7.5V ≤ V_{PVIN} ≤ 18V 0.12A ≤ I_{LOAD} ≤ 3A	5.00	 4.80/**4.75** 5.20/**5.25**	V V(min) V(max)
η1	System Efficiency	I_{LOAD} = 1A, T_A = 25°C, F_{OSC} Not Adjusted	94		%
η2	System Efficiency	I_{LOAD} = 3A, T_A = 25°C, F_{OSC} Not Adjusted	89		%
V_{REF}	Reference Voltage	$V_{SLEEPLOGIC}$ = 3V[3]	1.25	1.281/**1.294** 1.219/**1.206**	V(min) V(max)
I_Q	Quiescent Current in PWM mode	$V_{FB} = V_{REF}$ −20mV[4]	4.0	 6.50/**7.0**	mA mA(max)
I_{QS}	Quiescent Current in Sleep mode	$IV_{FB} = V_{REF}$ −20mV, $V_{SLEEPLOGIC}$ = 3V[4]	850	 1.35/**1.60**	µA mA(max)

(1) A typical is the center of characterization data taken at $T_A = T_J$ = 25°C.
(2) Tested at $T_A = T_J$ = 125°C and statistical correlation for room temperature and cold limits.
(3) V_{REF} is measured at SLEEP OUT ADJ.
(4) Quiescent current is the total current flowing into the P_{VIN} and V_{IN} pins. I_Q includes the current used to drive the gates of the two NMOS power FETs at the nominal switching frequency. I_{QS} includes no such current.

Electrical Characteristics (continued)

V_{PVIN} = 15V, $V_{SLEEP\ LOGIC}$ = 0V and V_{SD} = 0V unless superseded under **Conditions**. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25°C. Limits appearing in **boldface** type apply over the full junction temperature range shown under **Operating Ratings**.

Symbol	Parameter	Conditions	Typ[1]	Limit[2]	Units
I_{QSD}	Quiescent Current in Shutdown mode	V_{SD} = 3V[5]	9	20/**25**	µA µA(max)
$R_{DS(on)}$ HS	DC On-Resistance Drain-to-Source of the High-Side Power Switch	I_{DS} = 1A, $V_{SLEEPLOGIC}$ = 3V, V_{FB} = 3V, V_{BOOT} = 24V	130	170/**245**	mΩ mΩ(max)
$R_{DS(on)}$ LS	DC On-Resistance Drain-to-Source of the Low-Side Power Switch	I_{DS} = 1A, V_{FB} = 3V	125	175/**245**	mΩ mΩ(max)
$I_{L\ HS}$	Leakage current of the High-Side Power Switch	V_{PVIN} = 18V, V_{SW} = 0V, V_{SD} = 3V	100	**10**	nA µA(max)
$I_{L\ LS}$	Leakage current of the Low-Side Power Switch	V_{PVIN} = 18V, V_{SW} = 18V, V_{SD} = 3V	95	**210**	µA µA(max)
I_{LIMIT}	Active Current Limit of the High-Side Power Switch	V_{PVIN} = 15V, V_{BOOT} = 24V, V_{FB} = 3V, $V_{SLEEPLOGIC}$ = 3V,	5.5	**3.5** **7.5**	A A(min) A(max)
F_{OSC}	Oscillator Frequency	$V_{FB} = V_{REF}$ −20 mV	90	80/**75** 100/**105**	kHz kHz(min) kHz(max)
F_{MAX}	Maximum Oscillator Frequency	$I_{FREQ\ ADJ}$ = 100µA,[6] $V_{FB} = V_{REF}$ −20 mV	315	270/**260** 360/**370**	kHz kHz(min) kHz(max)
D_{MAX}	Maximum Duty Cycle	$V_{FB} = V_{REF}$ −20 mV, F_{OSC} Not Adjusted	97	94/**93**	% %(min)
D_{MIN}	Minimum Duty Cycle	$V_{FB} = V_{REF}$ +50 mV, F_{OSC} Not Adjusted	2.8	**5**	% %(min)
V_{DD}	Internal Rail Voltage	I_{VDD} = 1 mA	4.0	3.6/**3.4** 4.2/**4.3**	V V(min) V(max)
V_{BOOT}	Bootstrap Regulator Voltage (VRegH)	I_{BOOT} = 1 mA	7.5	6.5/**6.0**	V V(min)
I_{SS}	Soft Start Current		10	13.5/**20.0**	µA µA(max)
V_{HYST}	Hysteresis of the Sleep Comparator (C2 Figure 16)	$V_{SLEEPLOGIC}$ = 3V	30	**10** **50**	mV mV(min) mV(max)
	V_{IL} of SD			**0.95**	V(max)
	V_{IH} of SD			**2.10**	V(min)
	V_{IL} of SLEEP LOGIC			**0.9**	V(max)
	V_{IH} of SLEEP LOGIC			**2.0**	V(min)
	V_{IL} of SYNC			**0.50**	V(max)
	V_{IH} of SYNC			**1.45**	V(min)
T_{SD}	T_J for Thermal Shutdown		170		°C

(5) Quiescent current is the total current flowing into the P_{VIN} and V_{IN} pins. I_Q includes the current used to drive the gates of the two NMOS power FETs at the nominal switching frequency. I_{QS} includes no such current.

(6) Pulling 100µA out of FREQ ADJ simulates adjusting the oscillator frequency with a 12.5 kΩ resistor connected from FREQ ADJ to GND. The sleep mode cannot be used at switching frequencies above 250 kHz.

Typical Performance Characteristics

I_{QSD} vs Input Voltage

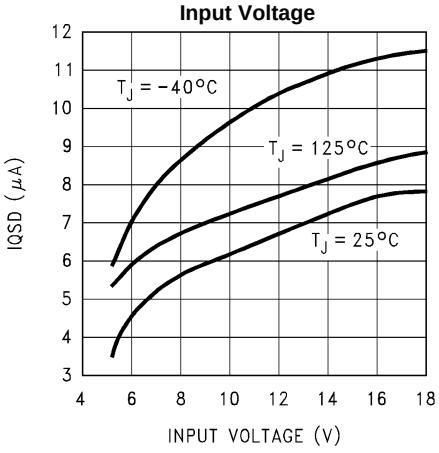


Figure 4.

I_{QS} vs Input Voltage

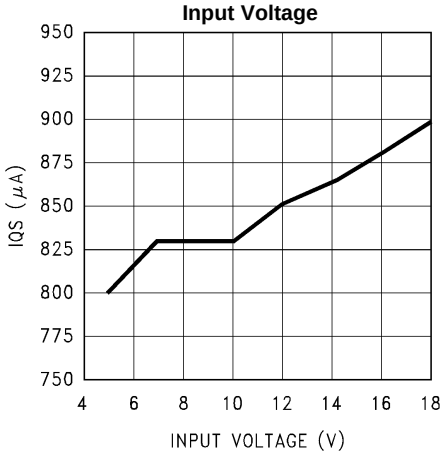


Figure 5.

I_Q vs Input Voltage

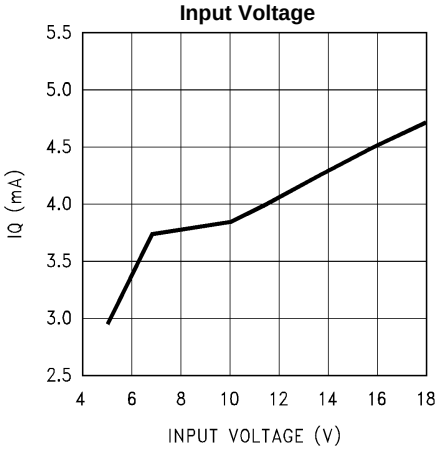


Figure 6.

I_Q vs Oscillator Frequency

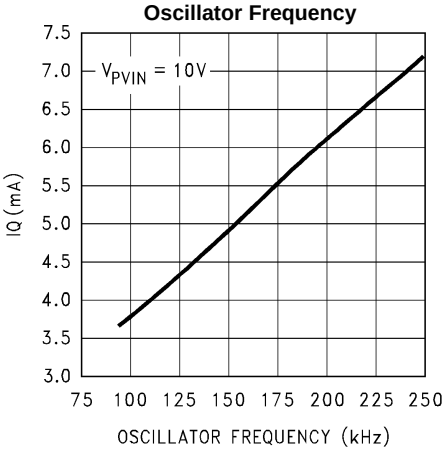


Figure 7.

$R_{DS(on)}$ Low-Side vs Input Voltage

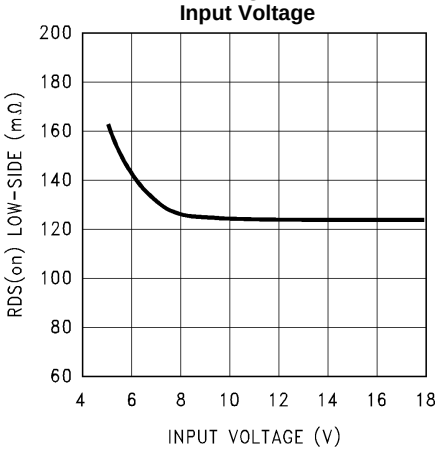


Figure 8.

$R_{DS(on)}$ High-Side vs Input Voltage

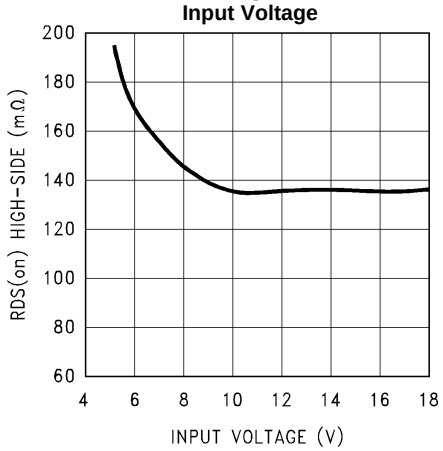


Figure 9.

Typical Performance Characteristics (continued)

$R_{DS(on)}$ Low-Side vs Junction Temperature

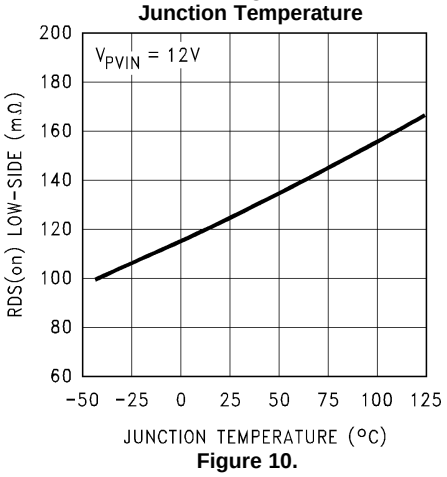


Figure 10.

$R_{DS(on)}$ High-Side vs Junction Temperature

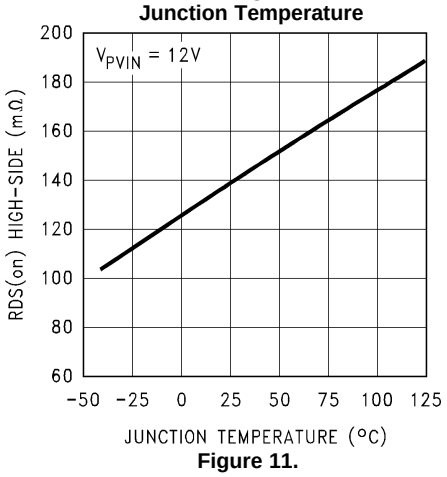


Figure 11.

Oscillator Frequency vs Junction Temperature

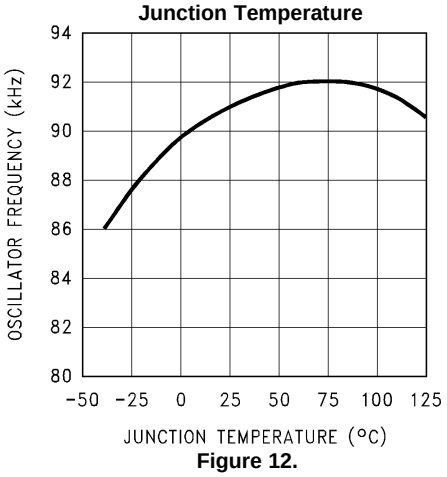


Figure 12.

Oscillator Frequency vs Adjusting Resistor

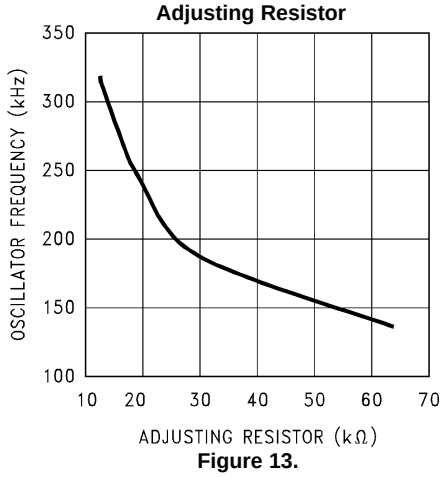


Figure 13.

Current Limit vs Junction Temperature

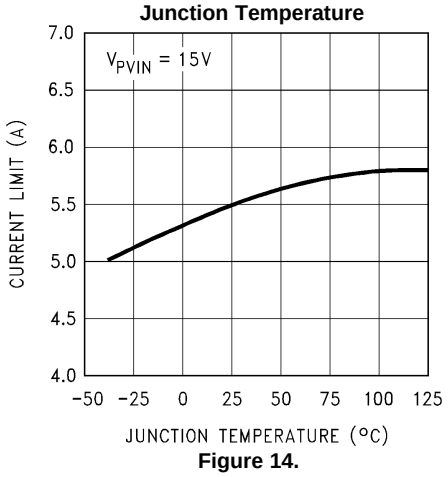


Figure 14.

Block Diagrams

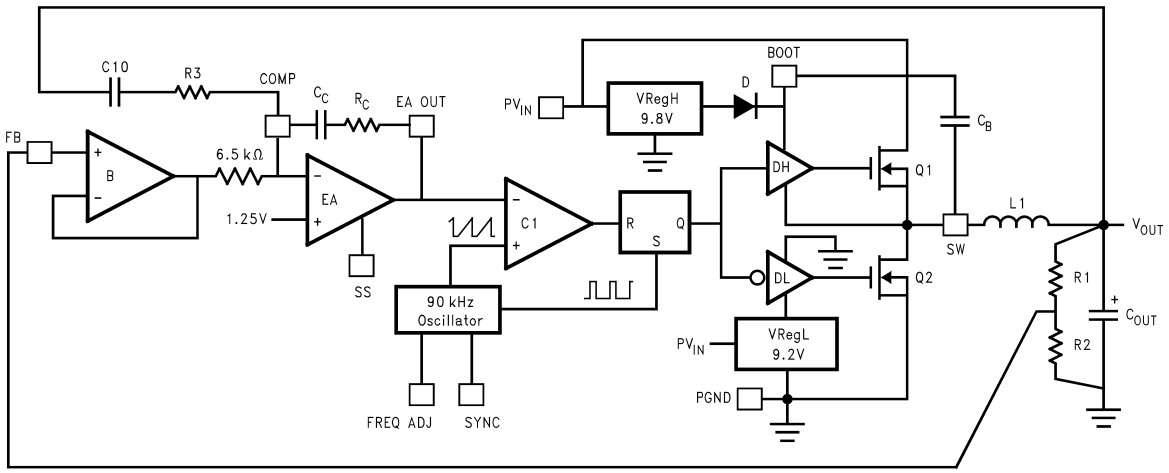


Figure 15. The PWM Circuit with External Components in a Closed Control Loop

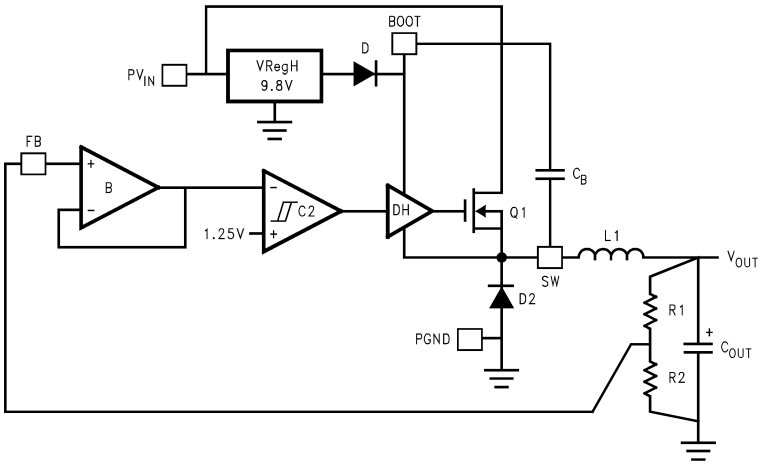


Figure 16. The Hysteretic or "Sleep" Circuit with External Components in a Closed Control Loop

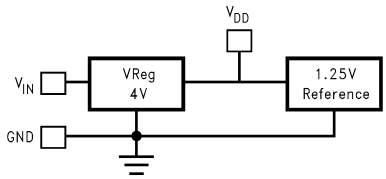


Figure 17. The Internal Voltage Regulator and Voltage Reference used by Both the PWM and Hysteretic Circuits

OPERATION

OVERVIEW

The LM2650 uses two step-down conversion modes: fixed-frquency pulse-width modulation (PWM) and hysteretic. It moves freely and automatically between them, using PWM for moderate to heavy loads and hysteretic for light loads.

For clarity, separate block diagrams for each conversion mode have been included. See Figure 15 and Figure 16. Blocks used in both modes appear in both diagrams with the same label. For example, both modes use the input buffer B. To keep the diagrams simple, most power supply rails have been omitted. R3, C10, R_C, C_C, C_B, L1, R1, R2, and C_{OUT} are outside the IC.

THE PWM CIRCUIT (Figure 15)

The PWM is a fixed-frequency, voltage-mode pulse-width modulator. It consists of four functional blocks: an input buffer, an error amplifier, a modulator, and a power stage.

1. The input buffer B: B is a voltage follower. A fraction of the output voltage is fed back to its noninverting input FB. Circumventing B by using the COMP input as the feedback input will cause the IC to malfunction.
2. The error amplifier EA: EA is a voltage amplifier. It subtracts the feedback voltage from the 1.25V reference and amplifies the difference to produce an error voltage for the control loop. For the purpose of loop compensation, EA is typically configured as an integrator. In this configuration, a capacitor C_C and a resistor R_C are connected in series between the inverting input COMP and the output terminal EA OUT. The capacitor and the internal 6.5kΩ resistor create a pole, while the capacitor and series resistor create a zero.
3. The modulator: The modulator is the heart of the PWM circuit. It consists of the 90 kHz oscillator, the voltage comparator C1, and output logic represented here as a simple SR latch.
   - The modulator generates a continuous stream of rectangular, signal-level. It generates the pulses at a fixed frequency, and it modulates or varies their widths in response to variations in the error voltage. The pulses appear at Q, the output of the SR latch. An increase in the error voltage results in a proportional increase in the pulse widths, and, conversely, a decrease in the error voltage results in a proportional decrease in the pulse widths.
   - The oscillator produces a 90 kHz sawtooth that ramps between 1V and 2V. At the beginning of each ramp, the oscillator sets the SR latch sending Q high. As the ramp voltage surpasses the error voltage, C1 resets the SR latch sending Q low. An increase in the error voltage increases the time between the setting and the resetting of the SR latch which , in turn, results in an equal increase in pulse widths: that is, an equal increase in the time Q spends high in each cycle. A decrease in the error voltage has the opposite effect on the pulse widths as it decreases the time between the setting and resetting of the SR latch.
4. The power stage: The power stage puts some punch between the output of the modulator by translating the stream of signal-level pulses generated by the modulator into a stream of power pulses that swing from ground up to the input voltage while sinking and sourcing as much as 3.5A. The power stage consists of two gate drivers DH and DL, two linear voltage regulators VRegH and VRegL, and two NMOS power FETs Q1 and Q2.
   - The power pulses appear at the SW mode. When Q goes high, DL drives the gate of Q2 low turning Q23 off. While Q2 turns off, the SW potential may remain at just below ground as the body diode of Q2 conducts what was previously reverse current (source-to-drain) in Q2, or the SW potential may swing up to just above the input voltage as the body diode of Q1 conducts what was previously forward current (drain-to-source) in Q2. About 50 ns after Q goes high, DH drives the gate of Q1 high turning Q1 on. If the task remains, Q1 pulls the SW potential up, if not, Q1 simply takes over the conduction responsibility from its own body diode. When Q goes low, the inverse action occurs resulting in the SW potential swinging from the input voltage to the ground. The 50 ns delay between one switch beginning to turn off and the other switch beginning to turn on prevents the switches from "shooting through" directly from the input supply to the ground.

– The PWM circuit drives the pulse stream into the low-pass filter made up of L1 and C_{OUT}. The filter passed the DC component of the stream and attenuates the AC components. The output of the filter is the DC voltage V_{OUT} superimposed with a small ripple voltage. Since the DC component of any periodic waveforms the average value of the waveform, V_{OUT} can be found using:

$$V_{OUT} = \frac{1}{T} \times \int_0^T v(t)dt. \quad (1)$$

– Here T is the switching period in seconds V(t) is the pulse stream. Under DC steady-state conditions, (1) yields

$$V_{OUT} = V_{IN} \times \frac{t_{ON}}{T} = V_{IN} \times D. \quad (2)$$

– Here V_{IN} is the input voltage, and therefore the height of the pulses, in volts, is the width of the pulses in seconds, and D is the ratio of t_{ON} to T, the duty or the duty cycle.

– The output voltage is programmed using the resistive divider made up for R1 and R2,

$$V_{OUT} = 1.25 \times \left(1 + \frac{R1}{R2}\right). \quad (3)$$

– As Q1 turns on, its source voltage swings up to just below the input voltage. The LM2650 uses a simple technique called "bootstrapping" to pull the positive supply rail of DH (at BOOT) up along with the source voltage of Q1, but to a voltage above the input voltage. Because the source of Q1 and the positive supply rail of DH make the same voltage swing together, DH maintains the positive gate-to-source voltage required to turn Q1 on. Q12 plays an active role in pulling the supply rail of DH up and is therefore said to pull itself up by its "bootstraps", thus the name of the technique and of the BOOT pin.

– In the typical application, a capacitor CB is connected outside the IC between the BOOT and SW pins. When Q2 is on, the input supply charges CB through VRegH and the internal diode D.

THE HYSTERETIC CIRCUIT AND LOOP (Figure 16)

Except for C2, the hysteretic circuit borrows all its circuit blocks from the PWM circuit.

The hysteretic comparator C2 is a voltage comparator with built-in hysteresis V_{HYST} of typically 30mV centered at 1.25V.

The diode D2 is the body diode of Q2. The hysteretic circuit uses D2 as a rectifier instead of switching Q2 as a synchronous rectifier.

When the load current drops below the prescribed sleep-in threshold, the LM2650 shuts down the PWM loop and starts up the hysteretic loop. The hysteretic loop supports light loads more efficiently because it uses less power to support its own operation; it uses less bias power because it's a simpler loop having less circuit blocks to bias, and it switches slower, so it incurs lower switching losses.

The hysteretic control loop does not switch at a constant frequency. Instead, it monitors V_{OUT} and switches only when V_{OUT} reaches either side of a narrow window centered on the desired output voltage. C2 directs the switching based on its reading of the feedback voltage. Switching in this manner yields a regulated voltage consisting of the desired output voltage and an AC ripple voltage. The magnitude of the AC component can be approximated using

$$V_{OUT\_PP} = V_{HYST} \times \frac{(R1 + R2)}{R2}. \quad (4)$$

For example, with V_{OUT} set to 5V, V_{OUT_PP} is approximately 120mV,

$$V_{OUT\_PP} = 0.03 \times \frac{(75 + 24.9)}{24.9} = 120\,mV. \quad (5)$$

When it starts up, the hysteretic loop turns Q1 on. While Q1 is on, the input power supply charges C_{OUT} and supplies current to the load. Current from the supply reaches C and the load via the series path provided by Q1 and L1. As the feedback voltage just surpasses the upper hysteretic threshold of C2, the output of C2 changes from high to low, and HD responds by pulling the gate of Q1 down turning Q1 off. As Q1 turns off, L1 generates a negative-going voltage transient that D2 clamps at just below ground. D2 remains on only briefly as the current in L1 runs out. While both Q1 and D2 are off, C_{OUT} alone supplies current to the load. As the feedback voltage just surpasses the lower hysteretic threshold of C2, the output of C2 changes states from low to high, and DH responds by pulling the gate of Q1 up turning Q1 on and starting the hysteretic cycle over.

Note that as the load current decreases, it takes increasingly longer periods for the load current to discharge C_{OUT} through the hysteretic window, and as the load current increases, the periods become even shorter. It can be seen from the above observation that the switching frequency of the hysteretic loop varies as the load varies. The switching frequency can be approximated using

$$f = \frac{I}{(C_{OUT} \times V_{OUT\_PP})}. \quad (6)$$

Here f is the switching frequency in hertz, I is the load current in amperes, C_{OUT} is the value of the capacitor in farads, and V_{OUT_PP} is the magnitude of the AC ripple voltage in volts. Typical switching frequencies range anywhere from a few hertz for very light loads to a few thousand hertz for light loads bordering on the moderate level.

Application Circuits

Figure 18 is a schematic of the typical application circuit. use the component values shown in the figure and those contained in Table 1 to build a 5V, 3A, or 3.3V, 3A step-down DC/DC converter. As with the design of any DC/DC converter, the design of these circuits involved tradeoffs between efficiency, size, and cost. Here more weight was given to efficiency than to size as evidenced by the low switching frequency which keeps switching losses low but pushes the value and size of the inductor up.

From a smaller circuit, use the component values shown in Figure 18 and those contained in Table 3. These circuits trade slightly higher switching losses for a much smaller inductor. Note, Figure 18 does not show R_{FA}, the resistor required to adjust the switching frequency from 90 kHz up to 200 kHz. Connect R_{FA} between the FREQ ADJ pin and ground.

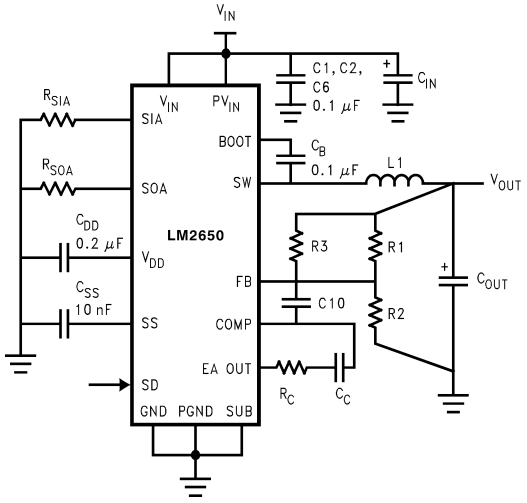


Figure 18. The Typical 90 kHz Application Circuit

Table 1. Components for the Typical 90 kHz Application Circuit

Input Voltage	**7V to 18V IN**	
Applicable Cell Stacks	8 to 12 Cell NiCd or NiMh, 3 to 4 Cell Li Ion, 8 to 11 Cell Alkaline, 6 Cell Lead Acid	
Output	**5V, 3A Out**	**3.3V, 3A out**
Input Capacitor C_{IN}	2 x 22 µF, 35V AVX TPS Series or Sprague 593D Series	2 x 22 µF, 35V AVX TPS Series or Sprague 593D Series
Inductor L1	40µH (See Table 2)	33µH (See Table 2)
Output Capacitor C_{OUT}	3x220 µF, 10V AVX TPS Series or Sprague 593D Series	3x220 µF, 10V AVX TPS Series or Sprague 593D Series
Feedback Resistors R1 and R2	R1 = 75kΩ, 1%, R2 = 24.9kΩ, 1%,	R1 = 41.2kΩ, 1%, R2 = 24.9kΩ, 1%,
Compensation Components R_C, C_C, R_3, and C_{10}	R_C = 37.4 kΩ, C_C = 4.7 nF, R_3 = 3.57 kΩ, C_{10} = 5.6 nF	R_C = 23.2 kΩ, C_C = 8.2 nF, R_3 = 2.0 kΩ, C_{10} = 10 nF
Sleep Resistors R_{SIA} and R_{SOA}	R_{SIA} = 33 kΩ, R_{SOA} = 200 kΩ	R_{SIA} = 39 kΩ, R_{SOA} = 130 kΩ

Table 2. Toroidal Inductors Using Cores from MICROMETALS, INC.

	Core Number	Core Material	Wire Gauge	Number of Strands	Number of Turns
15µH	T38	−52	AWG # 23	1	21
20µH	T38	−52	AWG # 23	1	25
33µH	T50	−52	AWG # 21	1	41
40µH	T50 (B)	−18	AWG # 21	1	41

Table 3. Components for Typical 200 kHz Applications

Input Voltage	**7V to 18V IN**	
Applicable Cell Stacks	8 to 12 Cell NiCd or NiMh, 3 to 4 Cell Li Ion, 8 to 11 Cell Alkaline, 6 Cell Lead Acid	
Output	**5V, 3A Out**	**3.3V, 3A out**
Input Capacitor C_{IN}	2 x 22 µF, 35V AVX TPS Series or Sprague 593D Series	2 x 22 µF, 35V AVX TPS Series or Sprague 593D Series
Inductor L1	20µH (See Table 2)	15µH (See Table 2)
Output Capacitor C_{OUT}	3x220 µF, 10V AVX TPS Series or Sprague 593D Series	3x220 µF, 10V AVX TPS Series or Sprague 593D Series
Feedback Resistors R1 and R2	R1 = 75kΩ, 1%, R2 = 24.9kΩ, 1%,	R1 = 41.2kΩ, 1%, R2 = 24.9kΩ, 1%,
Compensation Components R_C, C_C, R_3, and C_{10}	R_C = 53.6 kΩ, C_C = 2.7 nF, R_3 = 4.02 kΩ, C_{10} = 4.7 nF	R_C = 33.2 kΩ, C_C = 3.9 nF, R_3 = 3.01 kΩ, C_{10} = 6.8 nF
Sleep Resistors R_{SIA} and R_{SOA}	R_{SIA} = 33 kΩ, R_{SOA} = 200 kΩ	R_{SIA} = 47 kΩ, R_{SOA} = 91 kΩ
Frequency Adjusting Resistor R_{FA}	R_{FA} = 24.9 kΩ	R_{FA} = 24.9 kΩ

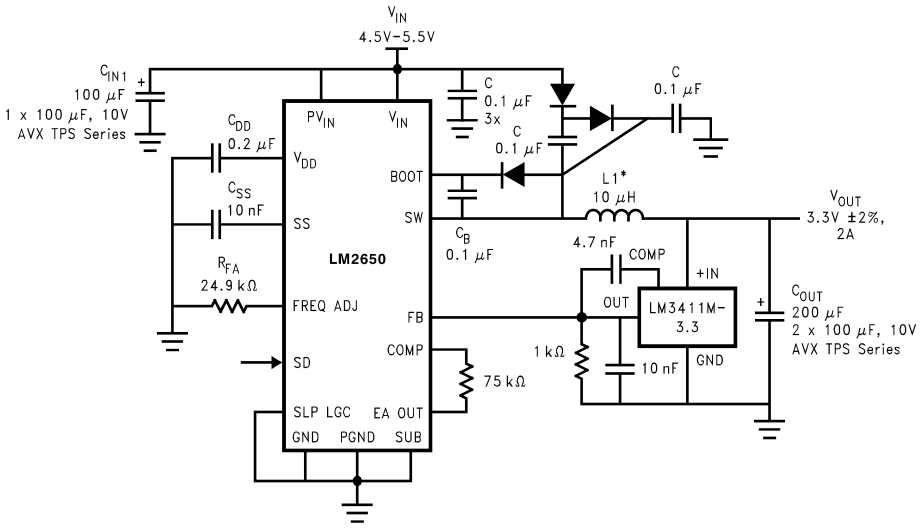


Figure 19. An Efficient, 2% Accurate 5V to 3.3V Converter

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2650M-ADJ/NOPB	ACTIVE	SOIC	DW	24	30	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	LM2650M -ADJ	Samples
LM2650MX-ADJ/NOPB	ACTIVE	SOIC	DW	24	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	LM2650M -ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

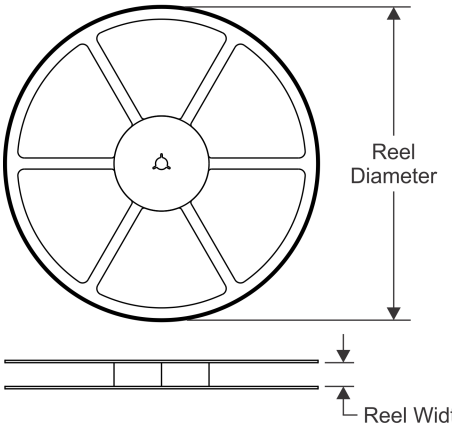
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

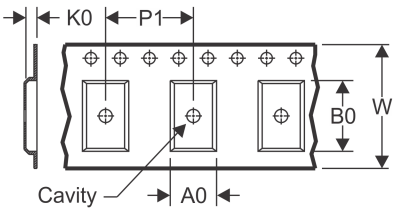
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

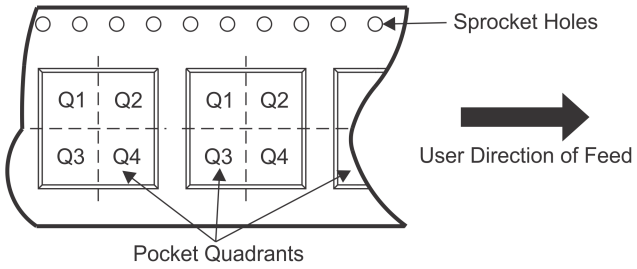


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

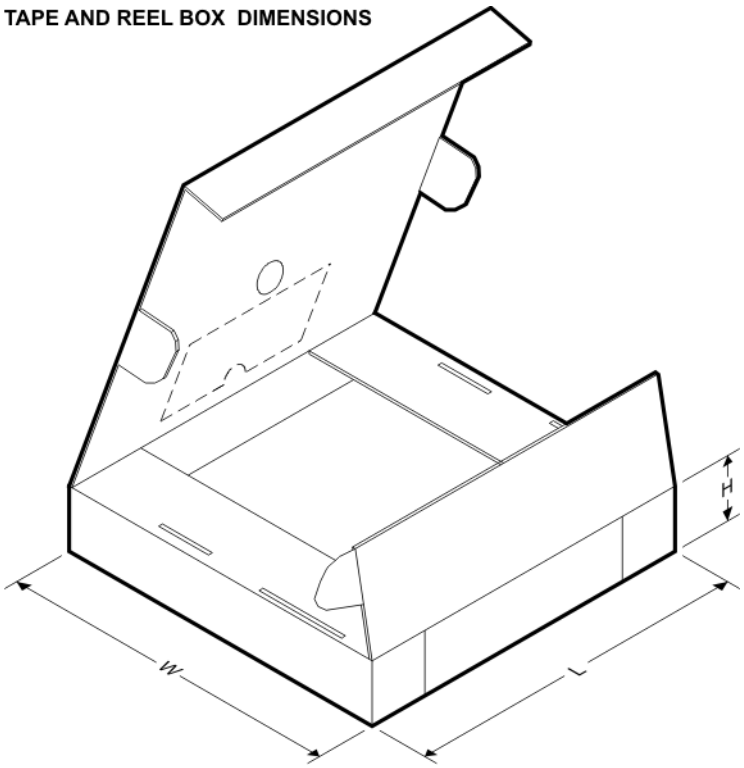
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2650MX-ADJ/NOPB	SOIC	DW	24	1000	330.0	24.4	10.8	15.9	3.2	12.0	24.0	Q1

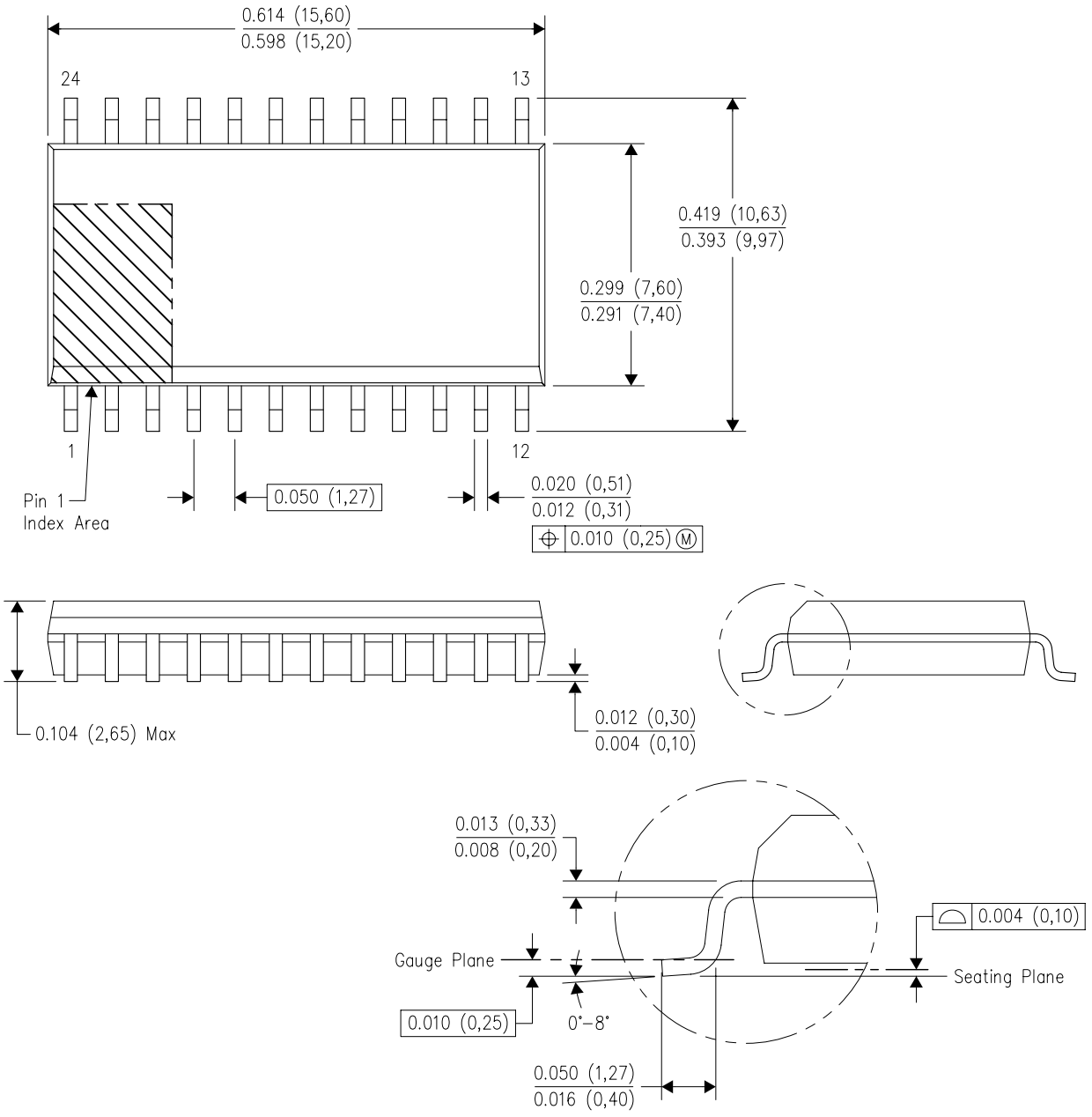
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2650MX-ADJ/NOPB	SOIC	DW	24	1000	367.0	367.0	45.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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