# **DAC-01**

# 6-BIT VOLTAGE-OUTPUT D/A CONVERTER

### Precision Monolithics Inc.

### **FEATURES**

- Standard Power Supplies ..... ± 12V to ± 18V
- TTL Compatible Logic Levels
- MIL-STD-883 Class B Processing Available From Stock
- Available in Die Form

### ORDERING INFORMATION<sup>†</sup>

	14-PIN HERMETIC DIP		
FULL TEMP. N.L. LSB	MILITARY TEMP.	COMMERCIAL TEMP.	
± 1/8	DAC01Y*		
± 1/4	DAC01BY*	DAC01CY	
	DAC01FY**	DAC01HY**	
± 1/2	<del></del>	DAC01DY	

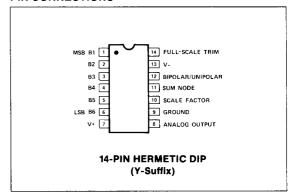
- For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
- \*\* Unipolar only -- all others unipolar or bipolar.
- † Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

### **GENERAL DESCRIPTION**

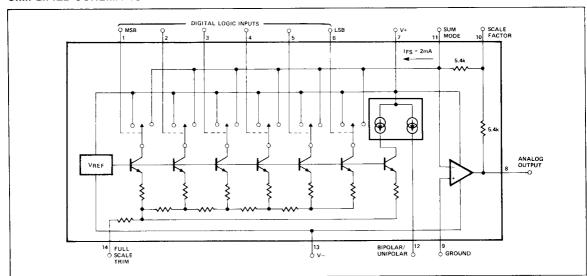
The DAC-01 is a complete monolithic 6-bit digital-to-analog converter. The device contains current steering logic, cur-

rent sources, a diffused resistor ladder network, precision voltage reference and fast summing op amp on one chip. Monolithic construction provides low power consumption and high reliability. Wide power supply range, three output voltage options, and three input code options assure flexibility for a wide variety of applications. A seventh bit may also be added for greater resolution. Introduced in 1970, the DAC-01 is still the fastest, lowest power, most accurate 6-bit complete monolithic DAC available. The DAC-01 is ideal for CRT deflection circuits, servo positioning controls, digitally programmed power supplies and pulse generators, modem and telephone system digitizing and demodulation circuits, digital filters, and 6-bit A/D converters.

### PIN CONNECTIONS



### SIMPLIFIED SCHEMATIC





# **ABSOLUTE MAXIMUM RATINGS (Note 2)**

· · · · · · · · · · · · · · · · · · ·	(14010 Z)
Operating Temperature	` '
DAC-01, DAC-01B, DAC-01F	55°C to +125°C
DAC-01C, DAC-01H, DAC-01D	0°C to +70°C
Junction Temperature (T)	65°C to +150°C
V+ Supply Voltage to Ground	0 to +18V
V- Supply Voltage to Ground	0 to -18V
Logic Input to Ground	0.7 to +6V
Storage Temperature	65°C to +150°C
Lead Temperature (Soldering, 60 sec) .	+300°C

Output Short-Circuit Duration (Note 2)Indefinite					
PACKAGE TYPE	Θ <sub>jA</sub> (Note 3)	Θ <sub>IC</sub>	UNITS		
8-Pin Hermetic DIP (Y)	108	16	°C/W		

#### NOTES:

- Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
- Θ<sub>|A</sub> is specified for worst case mounting conditions, i.e., Θ<sub>|A</sub> is specified for device in socket for CerDIP package.

# **ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15 V$ and over the rated operating temperature range, unless otherwise noted.

PARAMETER	SYMBOL	DAC-01*	DAC-01B*	DAC-01F	DAC-01C	DAC-01H	DAC-01D	UNITS
Output Options		Unipolar Bipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	
Temperature Range	T <sub>A</sub>	-55/+125	-55/+125	-55/+125	0/+70	0/+70	0/+70	°C
Nonlinearity 25° C/Maximum	NL	±0.40	±0.40	± 0.40	±0.40	±0.40	± 0.78	%FS
Nonlinearity Over Temperature — Maximum	NL	± 0.45	± 0.45	±0.45	±0.45	±0.45	±0.78	%FS
Full-Scale Tempco — Maximum	T <sub>C</sub>	±80	±120	±80	± 160	±160	±160	ppm/°C
Unipolar Zero-Scale Output Voltage — Maximum (Notes 1, 2	V <sub>ZS</sub>	25	25	40	25	40	50	mV

<sup>\*</sup> Processed to MIL-STD-883 only.

# **ELECTRICAL CHARACTERISTICS** for all DAC-01 grades, $V_S = \pm 15V$ and over the rated operating temperature range unless otherwise noted.

		DAC-01				
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Unipolar Full Range Output Voltage (Note 3)		$2k\Omega$ load, logic $\leq$ 0.8V, short pin 13 to pin 14. Short pin 12 to Ground and pin 10 to pin 11.	+10.0		+11.75	V
Bipolar Output Voltage (Note 3) ±5 Volt Range		2kΩ load, short pin 11 to pin 12. Short pin 13 to pin 14, short pin 10 to pin 11.				
Ü	V <sub>FR+</sub>	Logic Inputs ≤ 0.8V	+4.93	_	+5.94	
±10 Volt Range	V <sub>FR</sub> -	Logic Inputs ≥ 2.0V Open pin 10	-5.94	_	-4.93	V
	$V_{FR+}$	Logic Inputs ≤ 0.8V	+9.86	-	+11.89	
	V <sub>FR</sub> -	Logic Inputs ≥ 2.0V	-11.89		-9.86	٧
Bipolar Offset Voltage (Note 1		±5 Volt Range		±40	±70	
±1/2 (  V <sub>FR+</sub>   -   V <sub>FS-</sub>   )		±10 Volt Range	_	±80	±140	mV
Resolution			6		_	Bits
Logic Input "0"	V <sub>INL</sub>		_		0.8	V
Logic Input "1"	V <sub>INH</sub>		2	_	_	V
Logic Input Current, Each Input	I <sub>IN</sub>		_	±2	±8	μА
Power Supply Sensitivity	P <sub>SS</sub>	±12V ≤ V <sub>S</sub> ≤ ±18V V <sub>FS</sub> ≈ 10.0V		± 0.01	±0.15	%V <sub>FS</sub> /V
Power Consumption	P <sub>d</sub>	No Load		200	250	mW
Supply Current	1+	$V^{+} = +15V$	_	_	7.3	
Supply Current	1-	V" = -15V Logic Inputs ≤ 0.8V	_		9.3	mA
Setting Time to ±1/2 LSB Note 4	t <sub>S</sub>	$2.0 \text{V} \leq \text{Logic Level} \leq 0.8 \text{V T}_{\text{A}} = 25^{\circ}  \text{C}$	_	1.5	3	μS

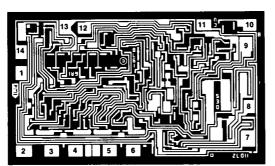
### NOTES:

- Zero-scale or bipolar offset voltage can be trimmed to zero volts or to the exact one's or two's complement condition with an external resistor network to pin 11.
- 2. Logic input voltage  $\geq$  2.0V.

- 3. Full-scale is adjustable to precisely 10V for unipolar operation and 10V or 20V peak-to-peak bipolar operation with an external 500 $\Omega$  potentiometer from pin 14 to V-.
- 4. Guaranteed by design.



## **DICE CHARACTERISTICS**



DIE SIZE  $0.093 \times 0.055$  inch, 5115 sq. mils  $(2.36 \times 1.40$  mm, 3.30 sq. mm)

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

- 1. B1 (MSB)
- 2. B2
- 3. B3
- 4. B4
- 5. B5
- 6. B6 (LSB)
- 7. V+
- 8. ANALOG OUTPUT
- 9. GROUND
- 10. SCALE FACTOR
- 11. SUM NODE
- 12. BIPOLAR/UNIPOLAR
- 13. V-
- 14. FULL-SCALE TRIM

# WAFER TEST LIMITS at $T_A = 25$ °C.

	CVMPO	CONDITIONS	DAC-01N BIPOLAR AND UNIPOLAR LIMIT	DAC-01G BIPOLAR AND UNIPOLAR LIMIT	UNITS
PARAMETER Nonlinearity	SYMBOL NL	V <sub>S</sub> = ±15V	1/4	1/2	L.S.B. MAX
Zero-Scale Voltage	V <sub>zs</sub>	V <sub>S</sub> = ±15V	25	35	mV MAX

# **WAFER TEST LIMITS** at $V_S = \pm 15V$ , $T_A = 25$ °C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-01 LIMIT	UNITS
Unipolar Full-Scale Output Voltage (All Models)	V <sub>FR</sub>	2kΩ Load, Logic ≤ 0.8V, Short V− to Full-Scale Trim, Unipolar/ Bipolar to Ground, and Scale Factor to Sum Node	10.00 11.75	V MIN V MAX
voluge (viii)		2kΩ Load, Short Sum Node to Unipolar/Bipolar. Short V- to Full-Scale Trim and Scale Factor to Sum Node.		
Bipolar Output Voltage	$V_{FR+}$	Logic Inputs ≤ 0.8V	+4.93	V MIN
±5 Volt Range	$V_{FR-}$	Logic Inputs ≥ 2.0V	-5.94	V MAX
± 10 Volt Range		Open-Scale Factor		
	V <sub>FR+</sub>	Logic Inputs ≤ 0.8V	+9.78	V MIN
	$V_{FR-}$	Logic Inputs ≥ 2.0V	-11.89	V MAX
Bipolar Offset Voltage		±5 Volt Range	±1/2	LSB MAX
±1/2 (IV <sub>FR+</sub> I - IV <sub>FR-</sub> I)		±10 Volt Range		
Resolution			6	Bits MAX
Logic Input "0"	V <sub>INL</sub>		0.8	V MAX
Logic Input "1"	V <sub>INH</sub>		2	V MIN
Logic Input Current, Each Input	Vov		±8	μΑ MAX
Power Supply Rejection	PSR	$\pm 12V \le V_S \le \pm 18V$ , $V_S = 10.0V$	0.15	%FS/V MAX
Power Consumption	P <sub>d</sub>	No Load	250	mW MAX

#### NOTE:

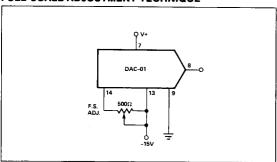
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

# TYPICAL ELECTRICAL CHARACTERISTICS at 25°C.

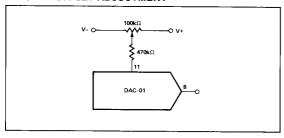
PARAMETER	SYMBOL	CONDITIONS	DAC-01N TYPICAL	DAC-01G TYPICAL	UNITS
Settling Time	t <sub>S</sub>	To ± 1/2 LSB	1.5	1.5	μs
Full-Scale Tempco	TCV <sub>FS</sub>	V <sub>S</sub> = ±15V	60	90	ppm/°C

## **BASIC CIRCUIT CONNECTIONS**

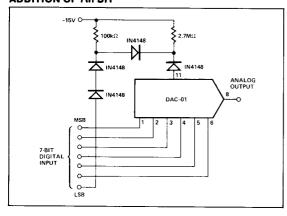
#### **FULL-SCALE ADJUSTMENT TECHNIQUE**



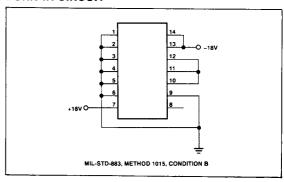
# OPTIONAL ZERO-SCALE OR BIPOLAR OFFSET ADJUSTMENT



## **ADDITION OF 7th BIT**



### **BURN-IN CIRCUIT**



### **APPLICATIONS INFORMATION**

#### INPUT CODES

The DAC-01 uses standard complementary binary coding for unipolar operation (all inputs logic high produces zero output voltage). One's complement coding may be implemented by shorting pin 11 to pin 12 and inverting the MSB (all other bits are not inverted). Complementary offset binary coding may be implemented by shorting pin 11 to pin 12, and injecting approximately  $5\mu A$  into pin 11 (which is at ground potential) by using the "optional Zero-Scale or bipolar offset adjustment" circuit. Two's complement code is achieved when the MSB for complementary offset binary is inverted.

### **FULL-SCALE ADJUST**

A 500 $\Omega$  pot from pin 14 to V- can be used to adjust the Full-Scale output voltage to exactly 10 volts in unipolar mode or 10 to 20 volts peak-to-peak in bipolar mode. If no pot is used, connect pin 14 to V-.

### **SCALE FACTOR**

For  $\pm$  10 volts or  $\pm$ 5 volt outputs, short pin 10 to pin 11 (adjusts the feedback resistor around the output amplifier). For  $\pm$  10 volt output, leave pin 10 open. Intermediate output voltages may be obtained by placing a pot between pin 10 and pin 11. This will, however, seriously degrade the Full-Scale temperature coefficient due to the mismatch between the  $\pm$ 1150ppm/°C tempco of the diffused resistors and the pot tempco.

### **CAPACITIVE LOADS**

When driving capacitive loads greater than 50pF in Unipolar mode or 30pF in Bipolar mode a 100pF capacitor may be placed from pin 11 to ground for added stability.

# **LOWER RESOLUTION APPLICATIONS**

When less than 6 bits of resolution is required, connect unused bits to a voltage level greater than +2.0 volts. The +5 volt logic supply is adequate.