Low Power, High Precision Operational Amplifier

OP97

FEATURES

Low supply current: 600 µA maximum
OP07 type performance
Offset voltage: 20 µV maximum
Offset voltage drift: 0.6 µV/°C maximum
Very low bias current
25°C: 100 pA maximum
−55°C to +125°C: 250 pA maximum
High common-mode rejection: 114 dB minimum
Extended industrial temperature range: −40°C to +85°C

PIN CONNECTIONS

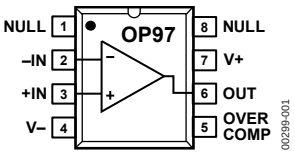

Figure 1. 8-Lead PDIP (P Suffix)
8-Lead SOIC (S Suffix)

GENERAL DESCRIPTION

The OP97 is a low power alternative to the industry-standard OP07 precision amplifier. The OP97 maintains the standards of performance set by the OP07 while utilizing only 600 µA supply current, less than 1/6 that of an OP07. Offset voltage is an ultralow 25 µV, and drift over temperature is below 0.6 µV/°C. External offset trimming is not required in the majority of circuits.

Improvements have been made over OP07 specifications in several areas. Notable is bias current, which remains below 250 pA over the full military temperature range. The OP97 is ideal for use in precision long-term integrators or sample-and-hold circuits that must operate at elevated temperatures.

Common-mode rejection and power supply rejection are also improved with the OP97, at 114 dB minimum over wider ranges of common-mode or supply voltage. Outstanding PSR, a supply range specified from ±2.25 V to ±20 V, and the minimal power requirements of the OP97 combine to make the OP97 a preferred device for portable and battery-powered instruments.

The OP97 conforms to the OP07 pinout, with the null potentiometer connected between Pin 1 and Pin 8 with the wiper to V+. The OP97 upgrades circuit designs using AD725, OP05, OP07, OP12, and PM1012 type amplifiers. It may replace 741-type amplifiers in circuits without nulling or where the nulling circuitry has been removed.

Rev. G
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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 1.

			OP97E			OP97F			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS									
Input Offset Voltage	V_{OS}			10	25		30	75	µV
Long-Term Offset Voltage Stability	ΔV_{OS}/Time			0.3			0.3		µV/month
Input Offset Current	I_{OS}			30	100		30	150	pA
Input Bias Current	I_B			±30	±100		±30	±150	pA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz		0.5			0.5		µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz[1]		17	30		17	30	nV/√Hz
		f_O = 1000 Hz[2]		14	22		14	22	nV/√Hz
Input Noise Current Density	i_n	f_O = 10 Hz		20			20		fA/√Hz
Large Signal Voltage Gain	A_{VO}	V_O = ±10 V; R_L = 2 kΩ	300	2000		200	2000		V/mV
Common-Mode Rejection	CMR	V_{CM} = ±13.5 V	114	132		110	132		dB
Input Voltage Range[3]	IVR		±13.5	±14.0		±13.5	±14.0		V
OUTPUT CHARACTERISTICS									
Output Voltage Swing	V_O	R_L = 10 kΩ	±13	±14		±13	±14		V
Differential Input Resistance[4]	R_{IN}		30			30			MΩ
POWER SUPPLY									
Power Supply Rejection	PSR	V_S = ±2 V to ±20 V	114	132		110	132		dB
Supply Current	I_{SY}			380	600		380	600	µA
Supply Voltage	V_S	Operating range	±2	±15	±20	±2	±15	±20	V
DYNAMIC PERFORMANCE									
Slew Rate	SR		0.1	0.2		0.1	0.2		V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = 1	0.4	0.9		0.4	0.9		MHz

[1] 10 Hz noise voltage density is sample tested. Devices 100% tested for noise are available on request.
[2] Sample tested.
[3] Guaranteed by CMR test.
[4] Guaranteed by design.

V_S = ±15 V, V_{CM} = 0 V, −40°C ≤ T_A ≤ +85°C for the OP97E/OP97F, unless otherwise noted.

Table 2.

			OP97E			OP97F			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage	V_{OS}			25	60		60	200	µV
Average Temperature	TCV_{OS}	S suffix		0.2	0.6		0.3	2.0	µV/°C
Coefficient of V_{OS}							0.3		
Input Offset Current	I_{OS}			60	250		80	750	pA
Average Temperature	TCI_{OS}			0.4	2.5		0.6	7.5	pA/°C
Coefficient of I_{OS}									
Input Bias Current	I_B			±60	±250		±80	±750	pA
Average Temperature									
Coefficient of I_B	TCI_B			0.4	2.5		0.6	7.5	pA/°C
Large Signal Voltage Gain	A_{VO}	V_O = 10 V; R_L = 2 kΩ	200	1000		150	1000		V/mV
Common-Mode Rejection	CMR	V_{CM} = ±13.5 V	108	128		108	128		dB
Power Supply Rejection	PSR	V_S = ±2.5 V to ±20 V	108	126		108	128		dB
Input Voltage Range[1]	IVR		±13.5	±14.0		±13.5	±14.0		V
Output Voltage Swing	V_O	R_L = 10 kΩ	±13	±14		±13	±14		V
Slew Rate	SR		0.05	0.15		0.05	0.15		V/µs
Supply Current	I_{SY}			400	800		400	800	µA
Supply Voltage	V_S	Operating range	±2.5	±15	±20	±2.5	±15	±20	V

[1] Guaranteed by CMR test.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	±20 V
Input Voltage[1]	±20 V
Differential Input Voltage[2]	±1 V
Differential Input Current[2]	±10 mA
Output Short-Circuit Duration	Indefinite
Operating Temperature Range OP97E, OP97F (P, S)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.

[2] The inputs of the OP97 are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. Differential input voltages greater than 1 V cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead PDIP (P Suffix)	103	43	°C/W
8-Lead SOIC (S Suffix)	158	43	°C/W

[1] θ_{JA} is specified for worst-case mounting conditions, that is, θ_{JA} is specified for device in socket for PDIP package; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

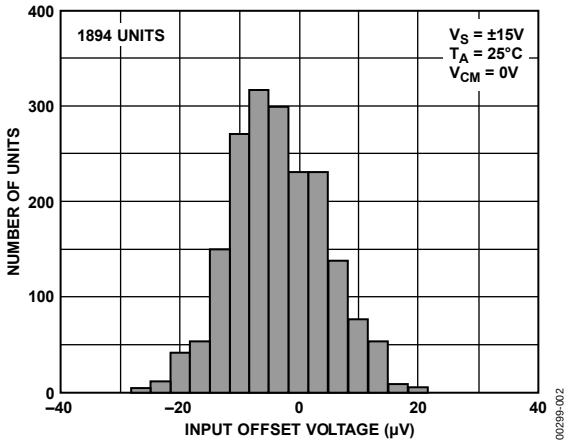


Figure 2. Typical Distribution of Input Offset Voltage

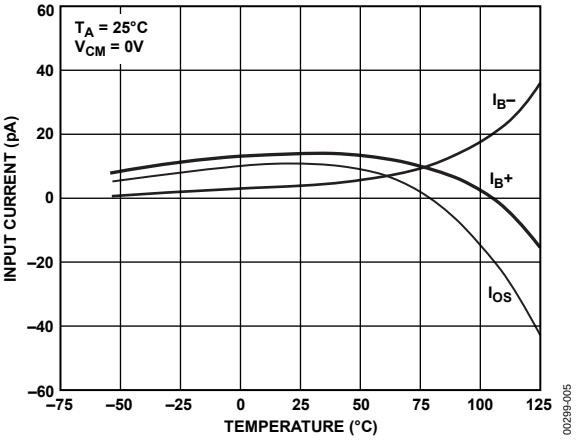


Figure 5. Input Bias, Offset Current vs. Temperature

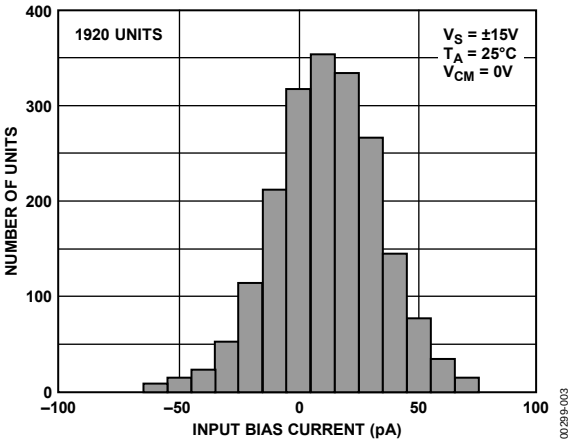


Figure 3. Typical Distribution of Input Bias Current

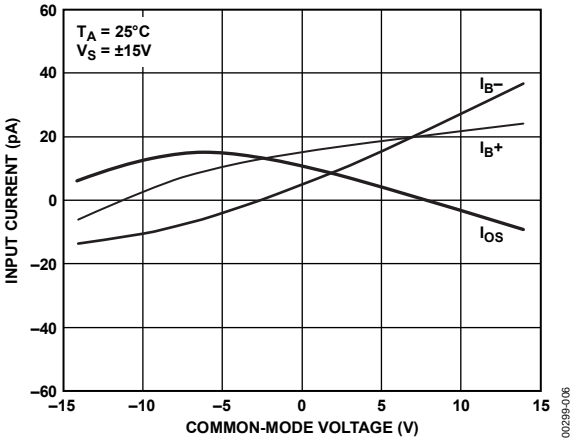


Figure 6. Input Bias, Offset Current vs. Common-Mode Voltage

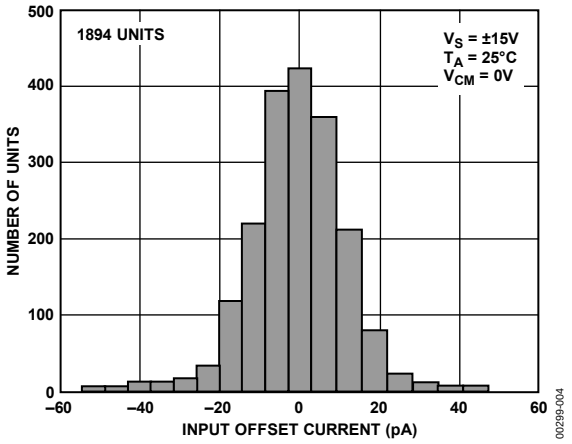


Figure 4. Typical Distribution of Input Offset Current

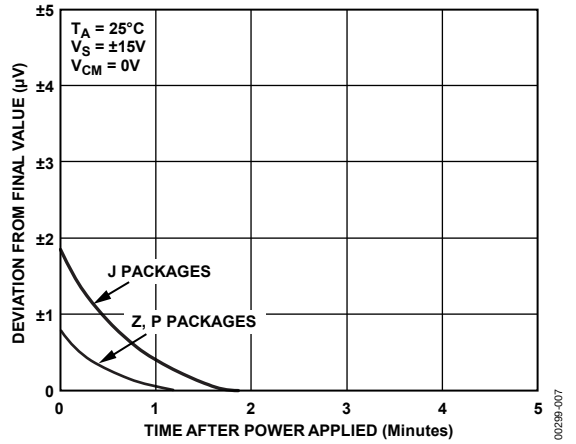


Figure 7. Input Offset Voltage Warmup Drift

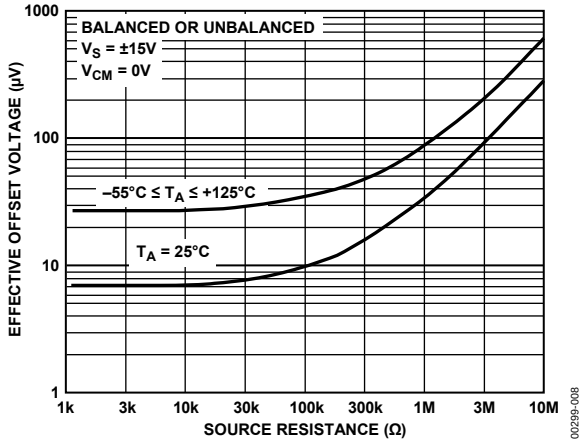


Figure 8. Effective Offset Voltage vs. Source Resistance

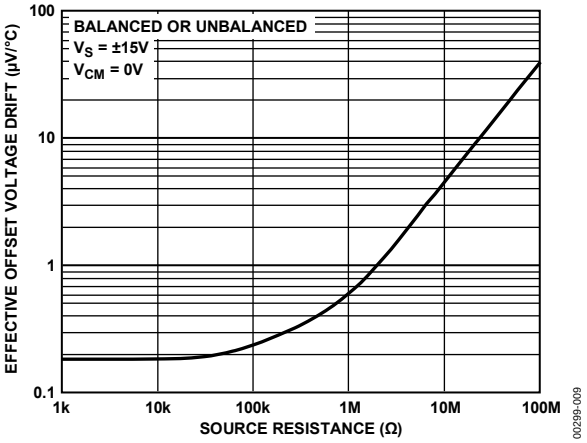


Figure 9. Effective TCV_{OS} vs. Source Resistance

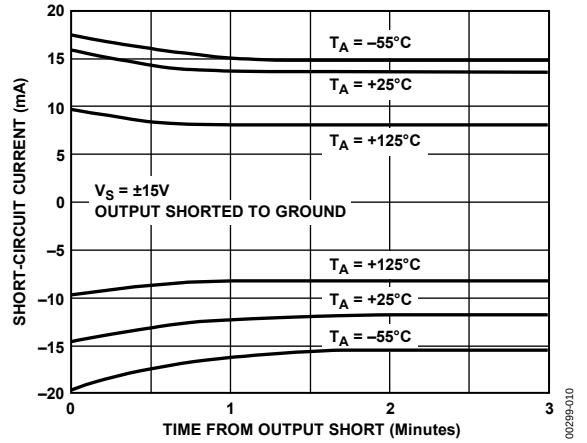


Figure 10. Short-Circuit Current vs. Time, Temperature

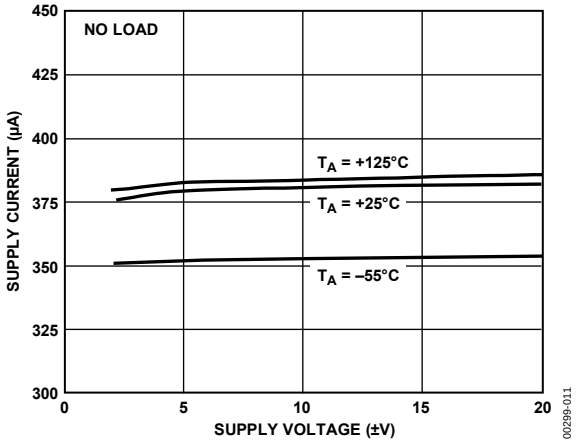


Figure 11. Supply Current vs. Supply Voltage

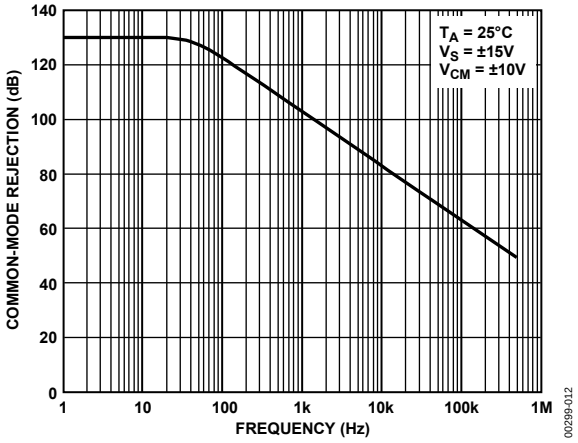


Figure 12. Common-Mode Rejection vs. Frequency

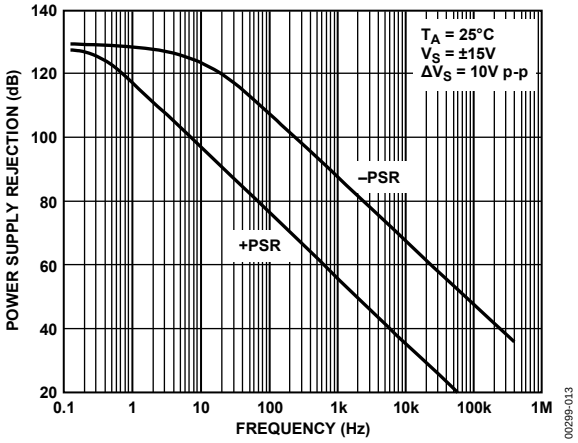


Figure 13. Power Supply Rejection vs. Frequency

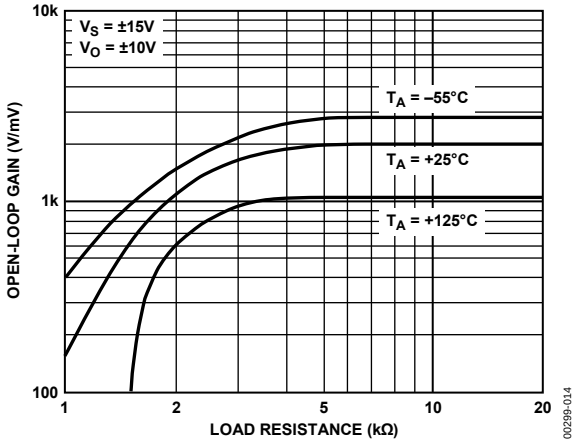


Figure 14. Open-Loop Gain vs. Load Resistance

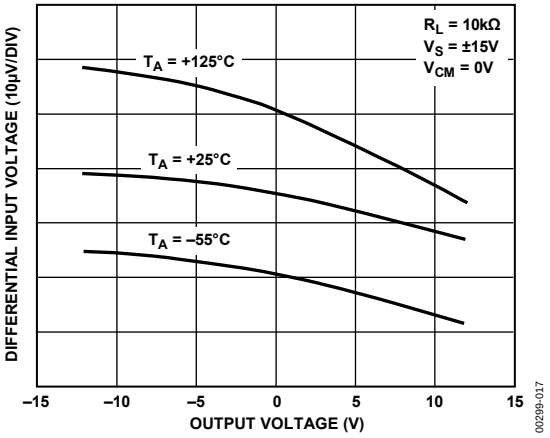


Figure 17. Open-Loop Gain Linearity

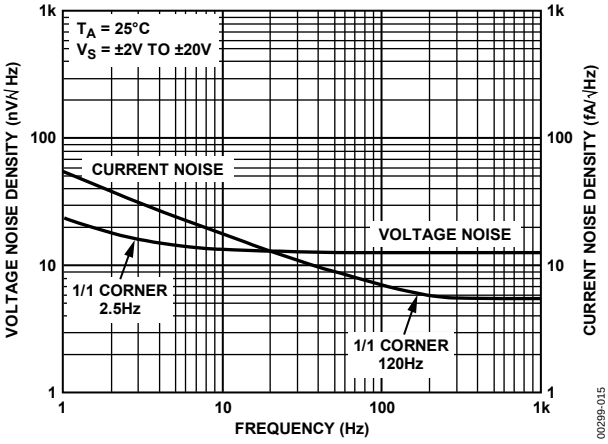


Figure 15. Noise Density vs. Frequency

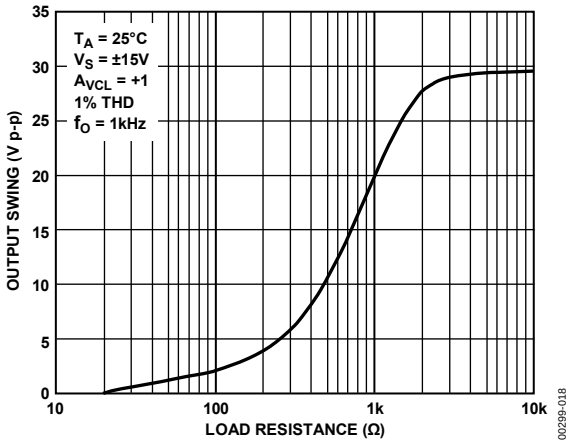


Figure 18. Maximum Output Swing vs. Load Resistance

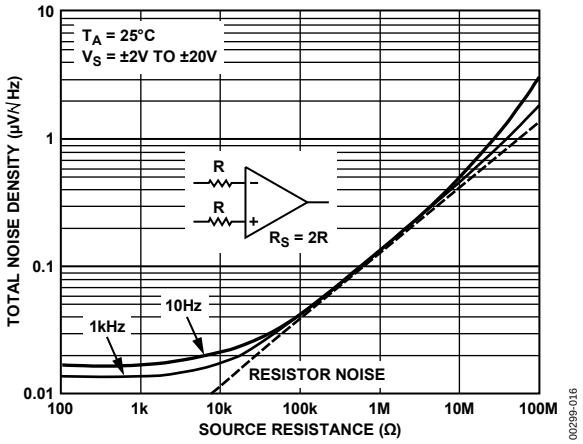


Figure 16. Total Noise Density vs. Source Resistance

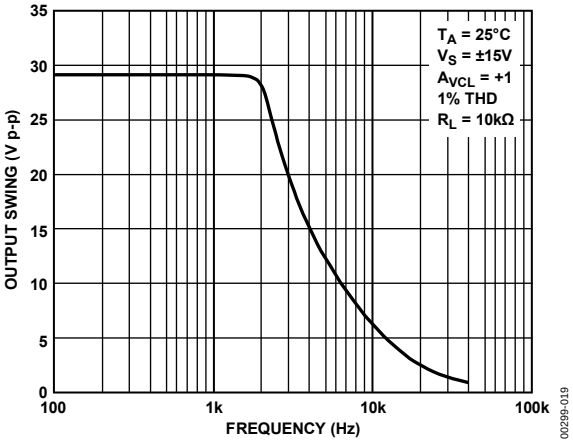


Figure 19. Maximum Output Swing vs. Frequency

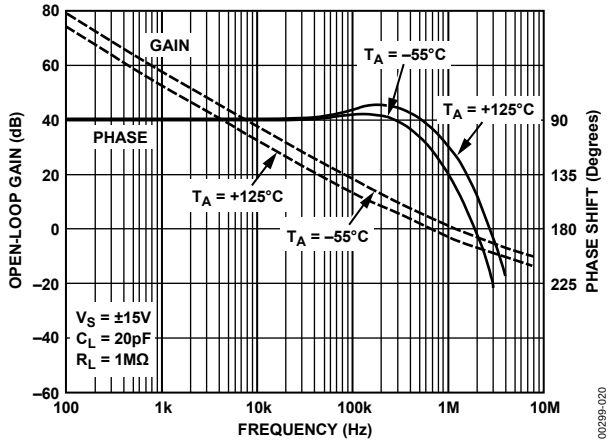


Figure 20. Open-Loop Gain, Phase vs. Frequency (C_{OC} = 0 pF)

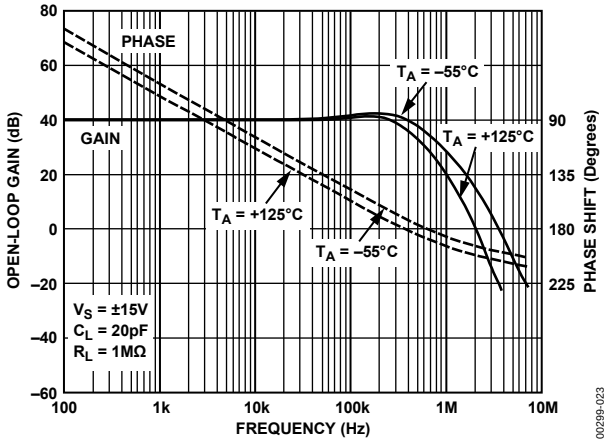


Figure 23. Open-Loop Gain, Phase vs. Frequency (C_{OC} = 100 pF)

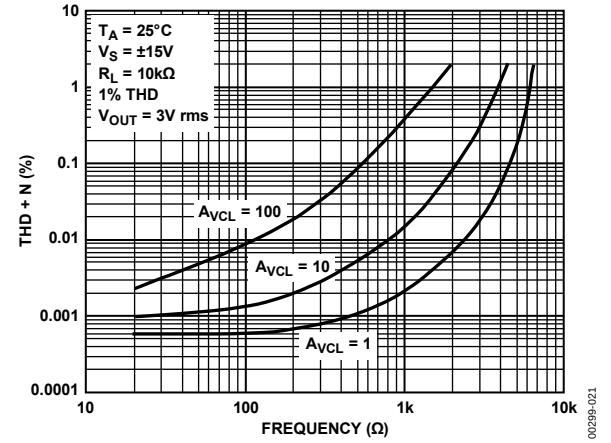


Figure 21. Total Harmonic Distortion Plus Noise vs. Frequency

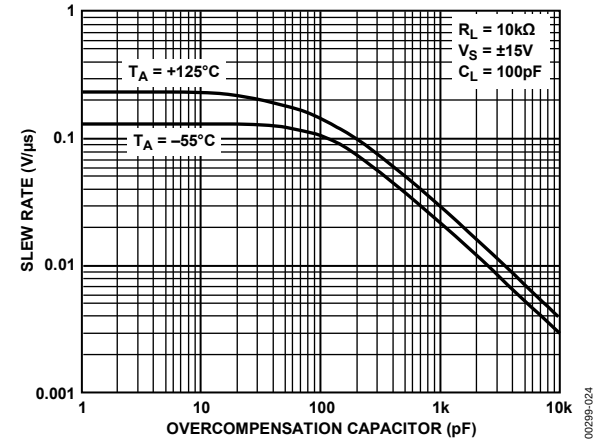


Figure 24. Slew Rate vs. Overcompensation

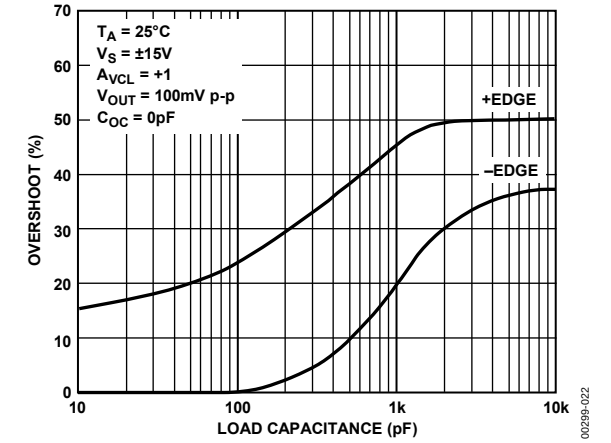


Figure 22. Small Signal Overshoot vs. Capacitive Load

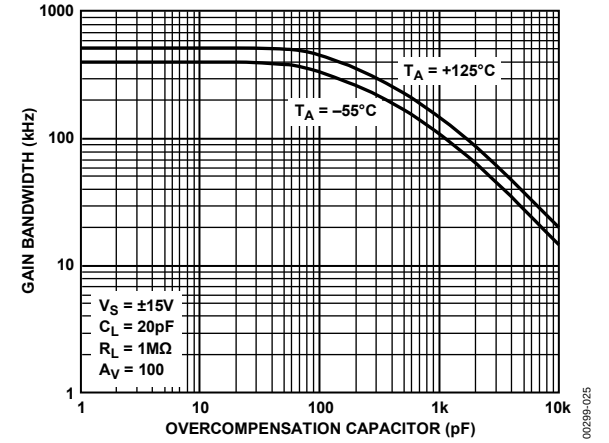


Figure 25. Gain Bandwidth Product vs. Overcompensation

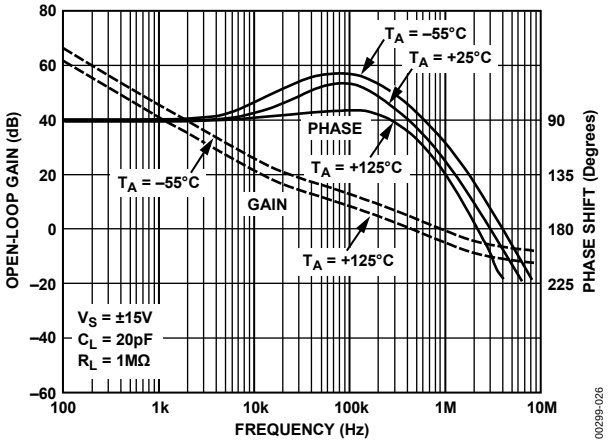


Figure 26. Open-Loop Gain, Phase vs. Frequency (C_{OC} = 1000 pF)

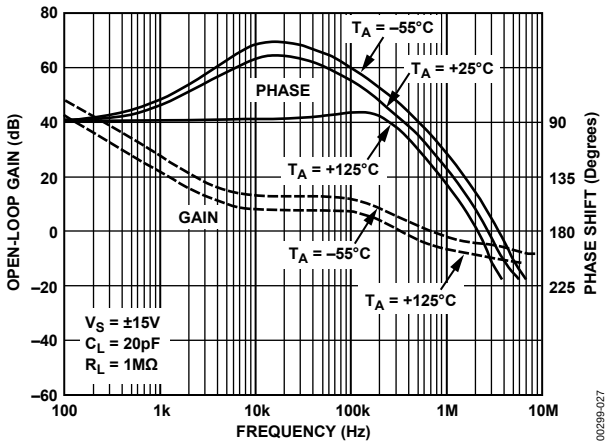


Figure 27. Open-Loop Gain, Phase vs. Frequency (C_{OC} = 10,000 pF)

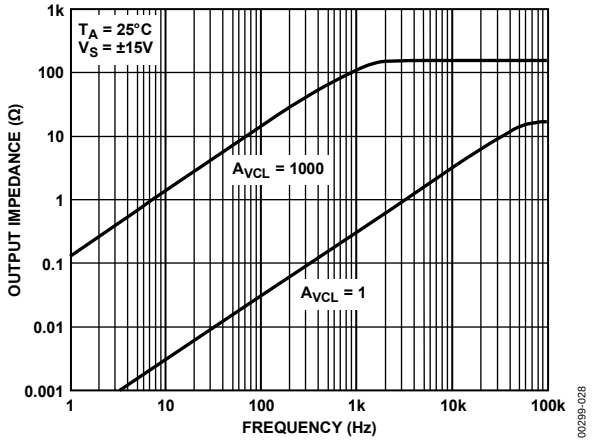


Figure 28. Closed-Loop Output Resistance vs. Frequency

APPLICATION INFORMATION

The OP97 is a low power alternative to the industry-standard precision op amp, the OP07. The OP97 can be substituted directly into OP07, OP77, AD725, and PM1012 sockets with improved performance and/or less power dissipation and can be inserted into sockets conforming to the 741 pinout if nulling circuitry is not used. Generally, nulling circuitry used with earlier generation amplifiers is rendered superfluous by the extremely low offset voltage of the OP97 and can be removed without compromising circuit performance.

Extremely low bias current over the full military temperature range makes the OP97 attractive for use in sample-and-hold amplifiers, peak detectors, and log amplifiers that must operate over a wide temperature range. Balancing input resistances is not necessary with the OP97. Offset voltage and TCV_{OS} are degraded only minimally by high source resistance, even when unbalanced.

The input pins of the OP97 are protected against large differential voltage by back-to-back diodes. Current-limiting resistors are not used to maintain low noise performance. If differential voltages above ±1 V are expected at the inputs, series resistors must be used to limit the current flow to a maximum of 10 mA. Common-mode voltages at the inputs are not restricted and may vary over the full range of the supply voltages used.

The OP97 requires very little operating headroom about the supply rails and is specified for operation with supplies as low as ±2 V. Typically, the common-mode range extends to within 1 V of either rail. The output typically swings to within 1 V of the rails when using a 10 kΩ load.

Offset nulling is achieved utilizing the same circuitry as an OP07. A potentiometer between 5 kΩ and 100 kΩ is connected between Pin 1 and Pin 8 with the wiper connected to the positive supply. The trim range is between 300 μV and 850 μV, depending upon the internal trimming of the device.

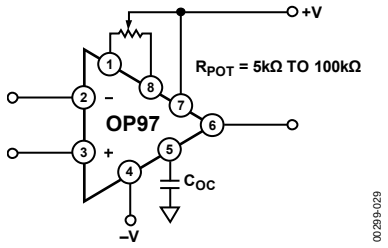


Figure 29. Optional Input Offset Voltage Nulling and Overcompensation Circuit

AC PERFORMANCE

The ac characteristics of the OP97 are highly stable over its full operating temperature range. Unity-gain small-signal response is shown in Figure 30. Extremely tolerant of capacitive loading on the output, the OP97 displays excellent response even with 1000 pF loads (see Figure 31). In large signal applications, the input protection diodes effectively short the input to the output during the transients if the amplifier is connected in the usual unity-gain configuration. The output enters short-circuit current limit, with the flow going through the protection diodes. Improved large signal transient response is obtained by using a feedback resistor between the output and the inverting input. Figure 32 shows the large-signal response of the OP97 in unity-gain with a 10 kΩ feedback resistor. The unity-gain follower circuit is shown in Figure 33.

The overcompensation pin (Pin 5) can be used to increase the phase margin of the OP97 or to decrease gain bandwidth product at gains greater than 10.

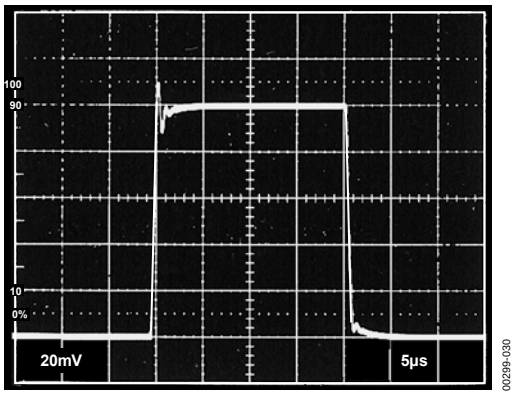


Figure 30. Small Signal Transient Response (C_{LOAD} = 100 pF, A_{VCL} = 1)

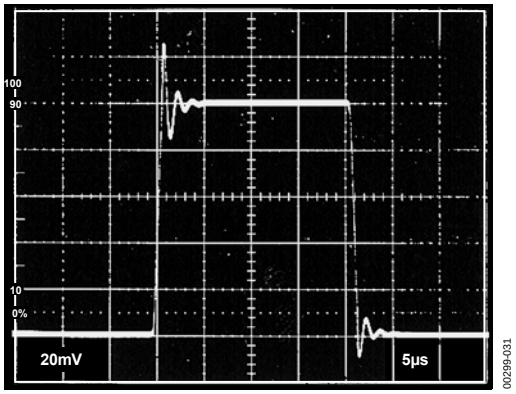


Figure 31. Small-Signal Transient Response (C_{LOAD} = 1000 pF, A_{VCL} = 1)

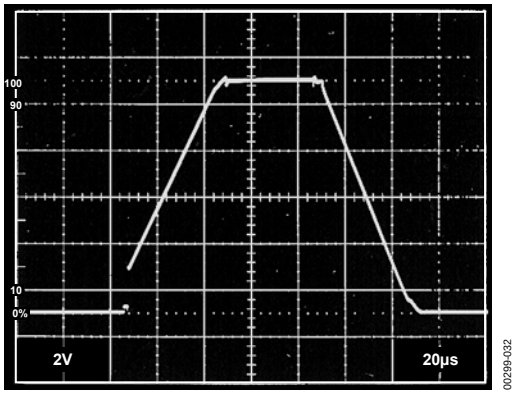


Figure 32. Large Signal Transient Response (A_{VCL} = 1)

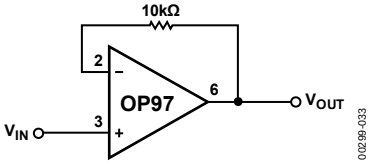


Figure 33. Unity-Gain Follower

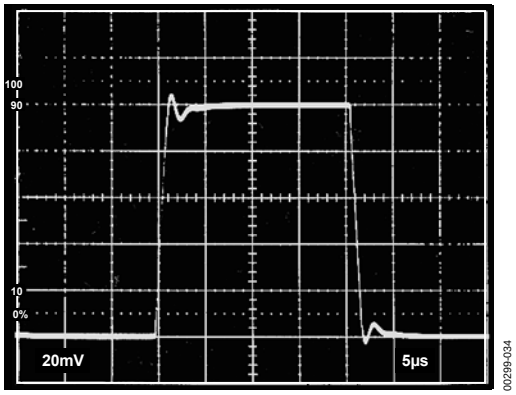


Figure 34. Small Signal Transient Response with Overcompensation (C_{LOAD} = 1000 pF, A_{VCL} = 1, C_{OC} = 220 pF)

GUARDING AND SHIELDING

To maintain the extremely high input impedances of the OP97, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PCB can have 100 pA of leakage currents between adjacent traces; therefore, use guard rings around the inputs. Guard traces are operated at a voltage close to that on the inputs, so that leakage currents are minimal. In noninverting applications, connect the guard ring to the common-mode voltage at the inverting input (Pin 2). In inverting applications, both inputs remain at ground, so that the guard trace should be grounded. Make guard traces on both sides of the circuit board.

High impedance circuitry is extremely susceptible to RF pickup, line frequency hum, and radiated noise from switching power supplies. Enclosing sensitive analog sections within grounded shields is generally necessary to prevent excessive noise pickup. Twisted-pair cable aid in rejection of line frequency hum.

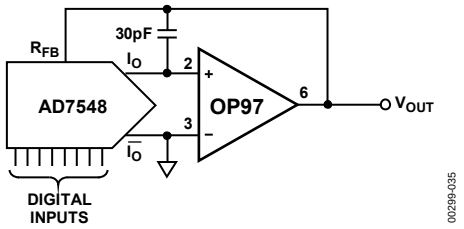


Figure 35. DAC Output Amplifier

The OP97 is an excellent choice as an output amplifier for higher resolution CMOS DACs. Its tightly trimmed offset voltage and minimal bias current result in virtually no degradation of linearity, even over wide temperature ranges.

Figure 36 shows a versatile monitor circuit that can typically sense current at any point between the ±15 V supplies. This makes it ideal for sensing current in applications such as full bridge drivers where bidirectional current is associated with large common-mode voltage changes. The 114 dB CMRR of the OP97 makes the contribution of the amplifier to common-mode error negligible, leaving only the error due to the resistor ratio inequality. Ideally, R2/R4 = R3/R5.

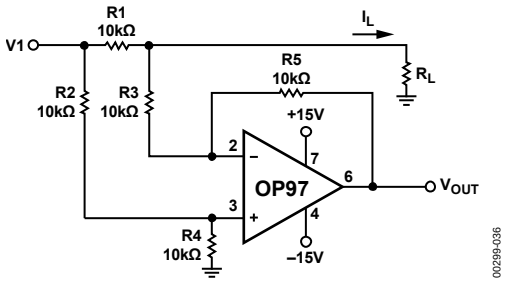


Figure 36. Current Monitor

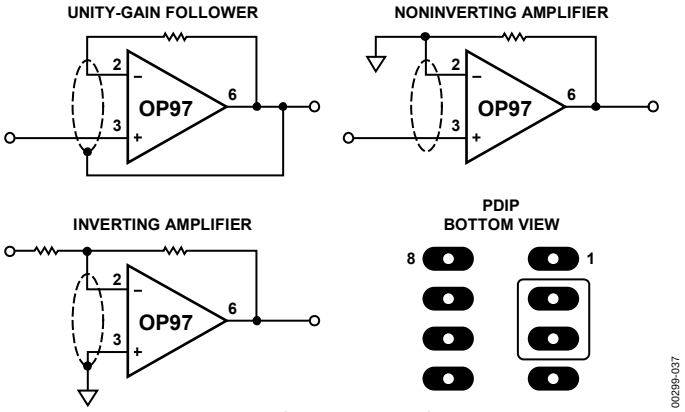


Figure 37. Guard Ring Layout and Connections

The digitally programmable gain amplifier shown in Figure 38 has 12-bit gain resolution with 10-bit gain linearity over the range of −1 to −1024. The low bias current of the OP97 maintains this linearity, while C1 limits the noise voltage bandwidth, allowing accurate measurement down to microvolt levels.

Table 5.

DIGITAL IN	GAIN (A_v)
4095	−1.00024
2048	−2
1024	−4
512	−8
256	−16
128	−32
64	−64
32	−128
16	−256
8	−512
4	−1024
2	−2048
1	−4096
0	Open Loop

Many high speed amplifiers suffer from less-than-perfect low frequency performance. A combination amplifier consisting of a high precision, slow device like the OP97 and a faster device such as the AD8610 results in uniformly accurate performance from dc to the high frequency limit of the AD8610, which has a gain-bandwidth product of 25 MHz. The circuit shown in Figure 39 accomplishes this, with the AD8610 providing high frequency amplification and the OP97 operating on low frequency signals and providing offset correction. Offset voltage and drift of the circuit are controlled by the OP97.

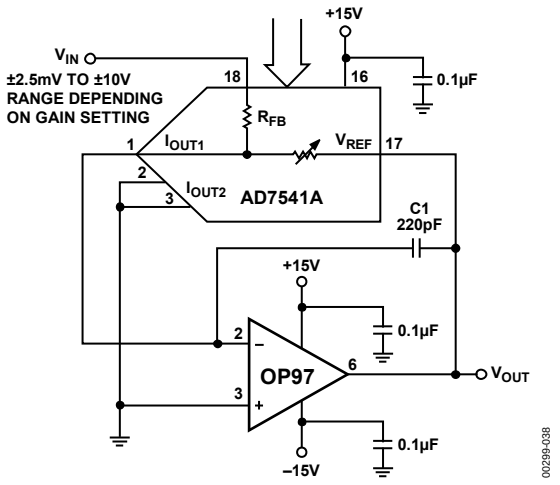


Figure 38. Precision Programmable Gain Amplifier

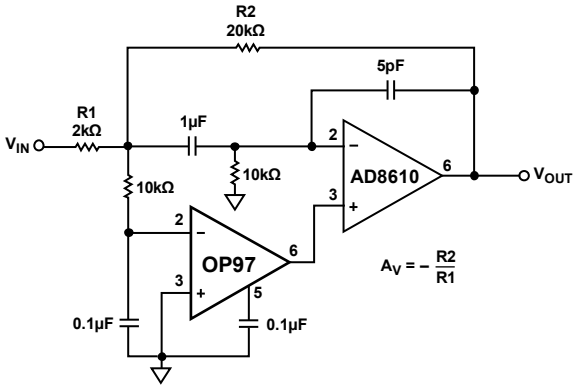


Figure 39. Combination High Speed, Precision Amplifier

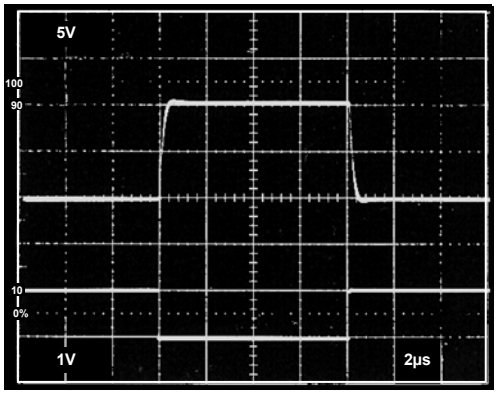
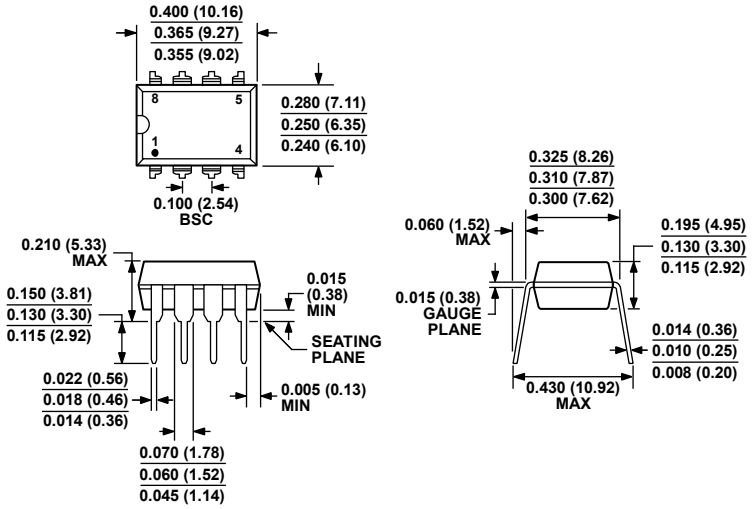


Figure 40. Combination Amplifier Transient Response

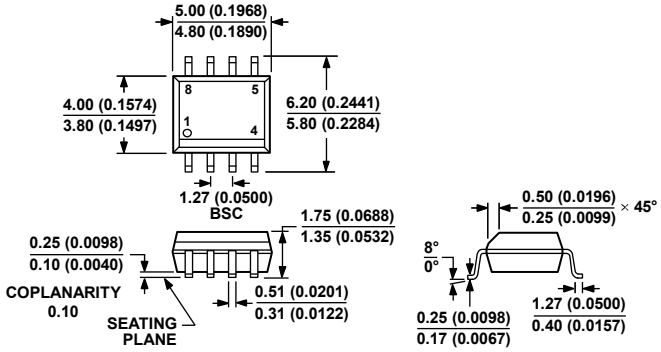
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 41. 8-Lead Plastic Dual In-Line Package [PDIP]
P-Suffix
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 42. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
S-Suffix
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP97EP	−40°C to +85°C	8-Lead PDIP	N-8
OP97EPZ[1]	−40°C to +85°C	8-Lead PDIP	N-8
OP97FP	−40°C to +85°C	8-Lead PDIP	N-8
OP97FPZ[1]	−40°C to +85°C	8-Lead PDIP	N-8
OP97FS	−40°C to +85°C	8-Lead SOIC_N	R-8
OP97FS-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
OP97FS-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8
OP97FSZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
OP97FSZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8
OP97FSZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.

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