Document Number: AFT26P100-4WS
Rev. 2, 3/2015

RoHS

RF Power LDMOS Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

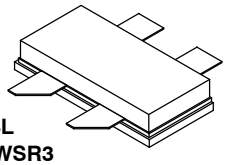
AFT26P100-4WSR3
AFT26P100-4WGSR3

2496–2690 MHz, 22 W AVG., 28 V
AIRFAST RF POWER LDMOS TRANSISTORS

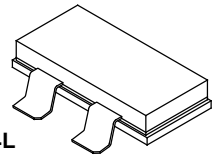
These 22 watt symmetrical Doherty RF power LDMOS transistors are designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2496 to 2690 MHz.

- Typical Doherty Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Volts, V_{GSA} = 0.4 Vdc, I_{DQB} = 344 mA, P_{out} = 22 Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.(1)

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2496 MHz	15.5	44.4	8.0	-32.3	-15
2590 MHz	16.1	43.5	7.8	-34.9	-14
2690 MHz	15.3	43.9	7.4	-35.0	-13



NI-780S-4L
AFT26P100-4WSR3



NI-780GS-4L
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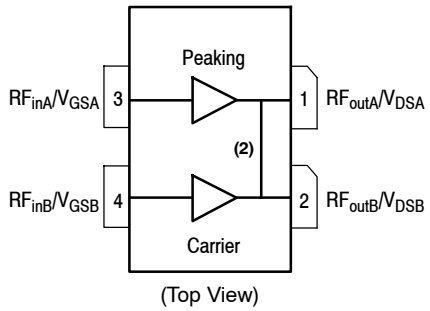


Figure 1. Pin Connections

2. Pin connections 1 and 2 are DC coupled and RF independent.

Features

- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Able to Withstand Extremely High Output VSWR and Broadband Operating Conditions
- In Tape and Reel. R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel.

1. All characterization data measured in characterization fixture with device soldered to heatsink.

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +125	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	195 2.60	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 77°C, 22 W CW, 28 Vdc, V_{GSA} = 0.7 Vdc, I_{DQB} = 200 mA, 2590 MHz	$R_{\theta JC}$	0.60	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	III

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (5) (V_{DS} = 10 Vdc, I_D = 140 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DB} = 200 mA, Measured in Functional Test)	$V_{GSB(Q)}$	1.3	1.8	2.1	Vdc
Drain-Source On-Voltage (4) (V_{GS} = 6 Vdc, I_D = 1.4 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

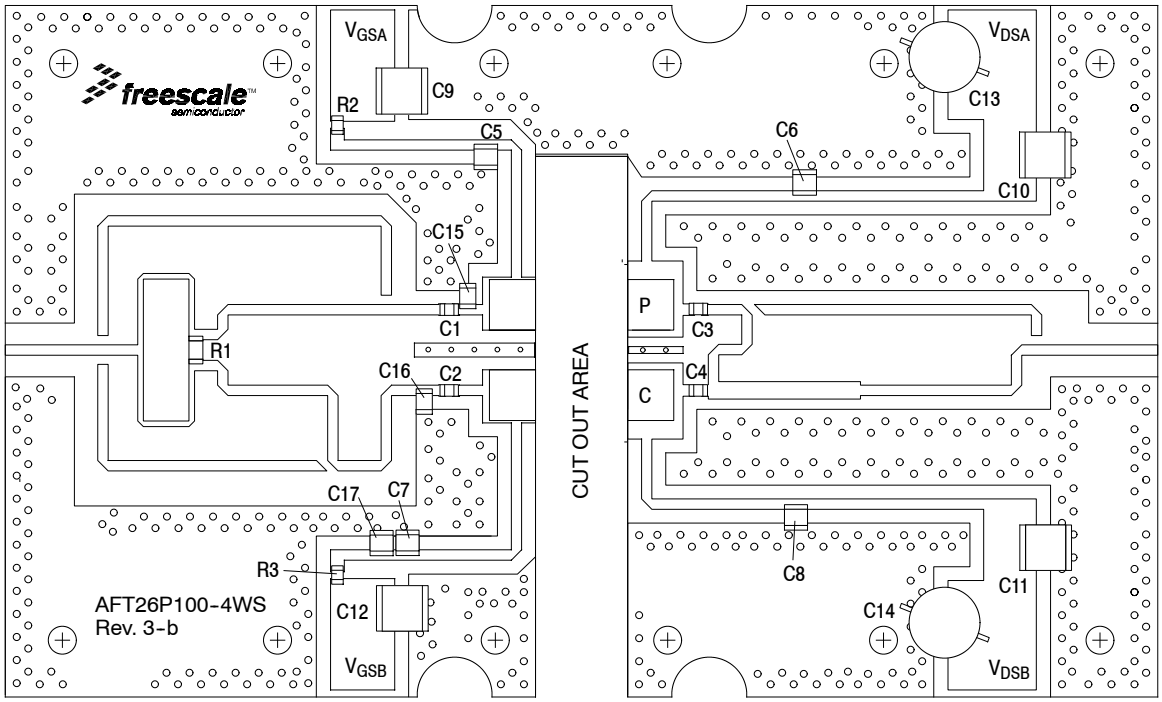
1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Measurement made with both sides of the transistor tied together.
5. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2,3,4) (In Freescale Doherty Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, V_{GSA} = 0.7 Vdc, I_{DQB} = 200 mA, P_{out} = 22 W Avg., f = 2690 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	14.4	15.1	17.4	dB
Drain Efficiency	η_D	39.0	41.0	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.8	7.4	—	dB
Adjacent Channel Power Ratio	ACPR	—	-33.8	-30.0	dBc
Input Return Loss	IRL	—	-17	-10	dB
Load Mismatch (In Freescale Production Test Fixture, 50 ohm system) I_{DQB} = 200 mA, f = 2590 MHz					
VSWR 10:1 at 32 Vdc, 125 W CW Output Power (3 dB Input Overdrive from 100 W CW Rated Power)	No Device Degradation				
Typical Performances (3,5) (In Freescale Doherty Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, V_{GSA} = 0.4 Vdc, I_{DQB} = 344 mA, 2496-2690 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	87	—	W
P_{out} @ 3 dB Compression Point (6)	P3dB	—	125	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2496-2690 MHz frequency range)	Φ	—	18	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	150	—	MHz
Gain Flatness in 194 MHz Bandwidth @ P_{out} = 22 W Avg.	G_F	—	0.2	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.01	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C) (7)	ΔP1dB	—	0.01	—	dB/°C

1. V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
2. Part internally matched both on input and output.
3. Measurement made with device in a symmetrical Doherty configuration.
4. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GS) parts.
5. All characterization data measured in characterization fixture with device soldered to heatsink.
6. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
7. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.

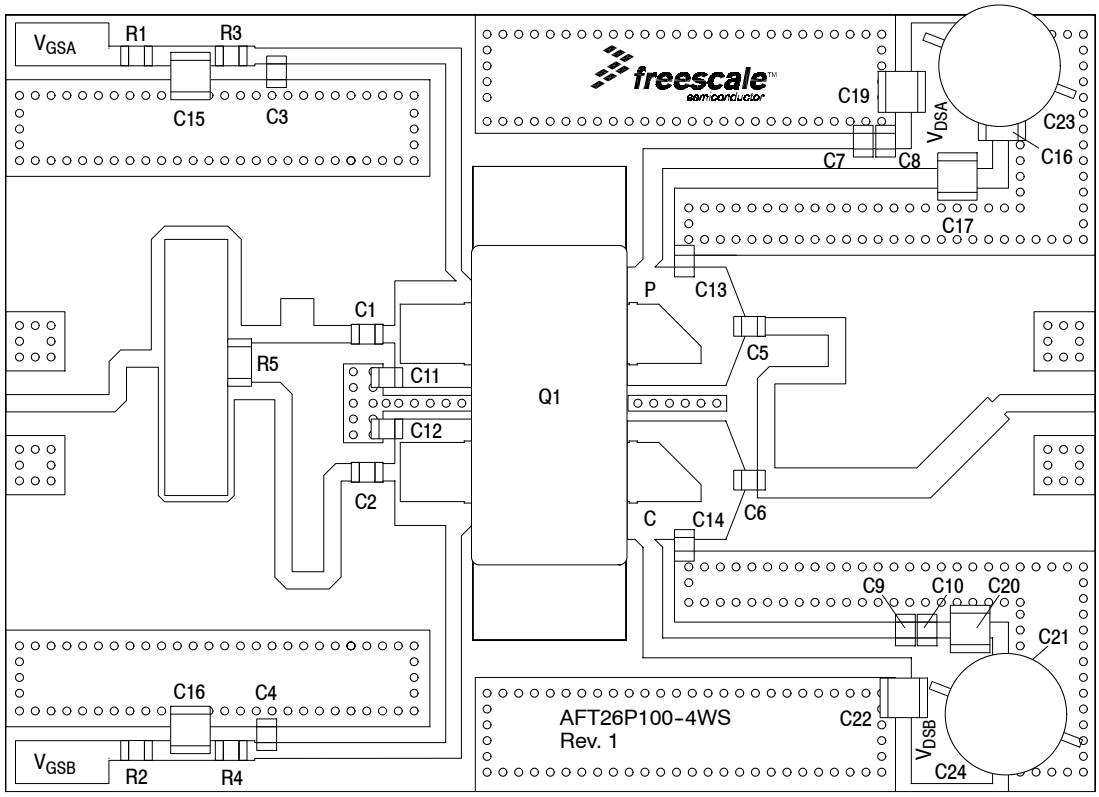


NOTE: V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.

Figure 2. AFT26P100-4WSR3 Production Test Circuit Component Layout

Table 5. AFT26P100-4WSR3 Production Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	8.2 pF Chip Capacitors	ATC600F8R2BT250XT	ATC
C3	6.8 pF Chip Capacitor	ATC600F6R8BT250XT	ATC
C4	4.3 pF Chip Capacitor	ATC600F4R3BT250XT	ATC
C5, C6, C7, C8, C17	4.3 pF Chip Capacitors	ATC100B4R3CT500XT	ATC
C9, C10, C11, C12	10 μF Chip Capacitors	GRM55DR61H106KA88L	Murata
C13, C14	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
C15	0.5 pF Chip Capacitor	ATC800B0R5BT500XT	ATC
C16	0.3 pF Chip Capacitor	ATC800B0R3BT500XT	ATC
R1	100 Ω, 1/4 W Chip Resistor	CRCW1206100RFKEA	Vishay
R2, R3	5.1 Ω, 1/10 W Chip Resistors	CRCW08055R10JNEA	Vishay
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers



NOTE 1: All characterization data measured in characterization fixture with device soldered to heatsink.
NOTE 2: V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.

Figure 3. AFT26P100-4WSR3 Characterization Test Circuit Component Layout

Table 6. AFT26P100-4WSR3 Characterization Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10	6.8 pF Chip Capacitors	ATC600F6R8BT250XT	ATC
C11, C12, C13, C14	0.2 pF Chip Capacitors	ATC600F0R2BT250XT	ATC
C15, C16, C17, C18, C19, C20, C21, C22	10 μF, 50 V Chip Capacitors	GRM32ER61H106KA12L	Murata
C23, C24	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
Q1	RF Power LDMOS Transistor	AFT26P100-4WSR3	Freescale
R1, R2	0 Ω, 1 A Chip Jumpers	CWCR08050000Z0EA	Vishay
R3, R4	5.1 Ω, 1/8 W Chip Resistors	CRCW08055R10JNEA	Vishay
R5	100 Ω, 1/4 W Chip Resistor	CRCW1206100RFKEA	Vishay
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers

TYPICAL CHARACTERISTICS (1)

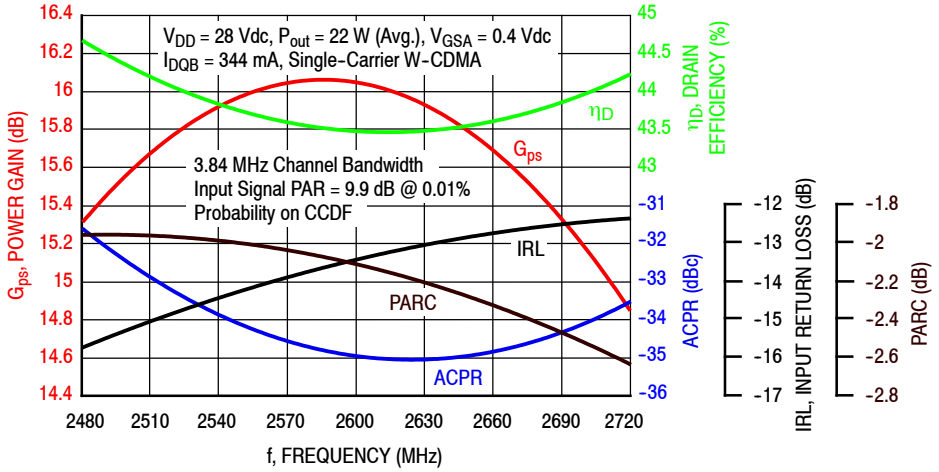


Figure 4. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 22 Watts Avg.

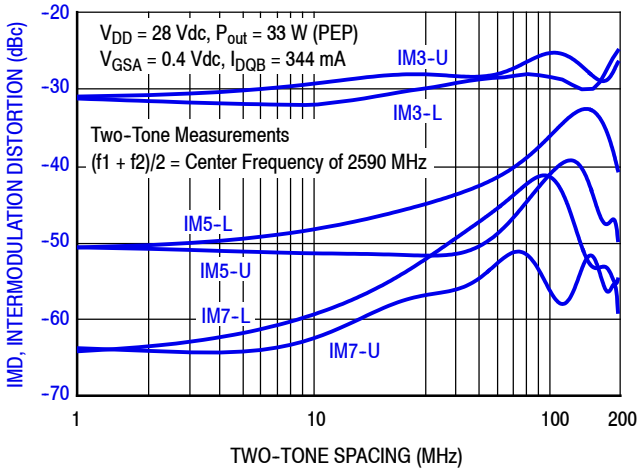


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

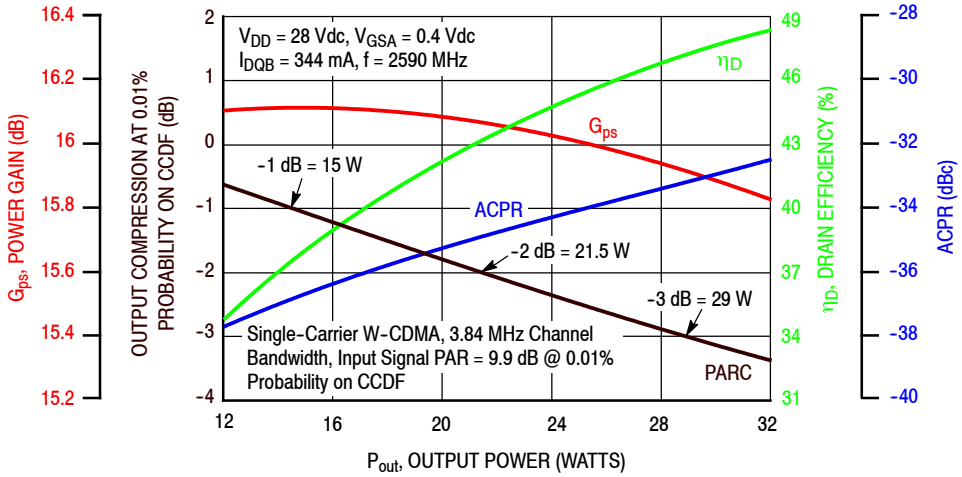


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

1. All characterization data measured in characterization fixture with device soldered to heatsink.

TYPICAL CHARACTERISTICS (1)

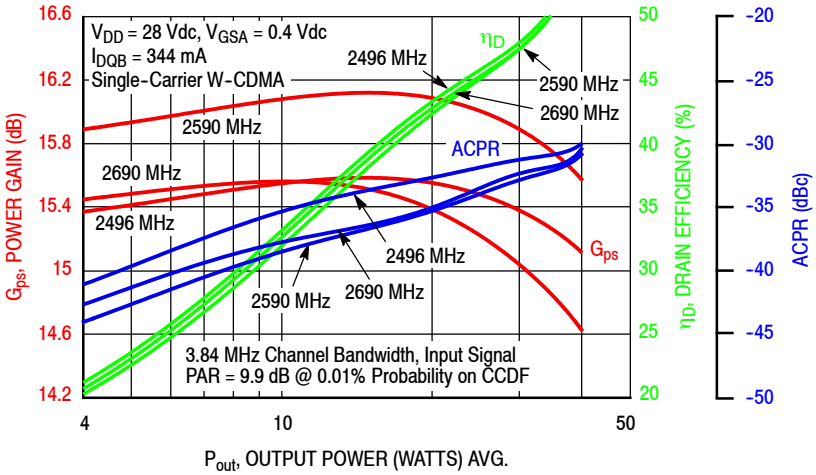


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

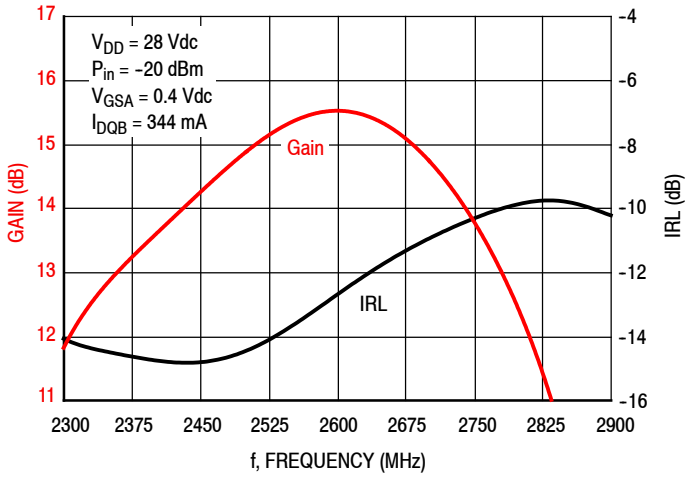


Figure 8. Broadband Frequency Response

1. All characterization data measured in characterization fixture with device soldered to heatsink.

V_{DD} = 28 Vdc, I_{DQA} = 189 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2500	4.37 – j13.8	5.84 + j14.7	3.19 – j9.50	16.3	48.7	73	53.8	–13
2600	7.22 – j15.5	9.54 + j16.6	3.35 – j9.78	16.7	48.6	73	54.9	–12
2690	13.2 – j15.4	15.2 + j17.0	3.40 – j10.5	16.5	48.8	76	55.8	–11

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2500	4.37 – j13.8	5.71 + j15.8	3.19 – j9.84	14.2	49.4	87	54.9	–20
2600	7.22 – j15.5	10.4 + j18.5	3.35 – j10.4	14.4	49.4	87	54.8	–18
2690	13.2 – j15.4	17.9 + j18.8	3.40 – j10.9	14.4	49.5	89	56.1	–16

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 9. Single Side Load Pull Performance — Maximum Power Tuning

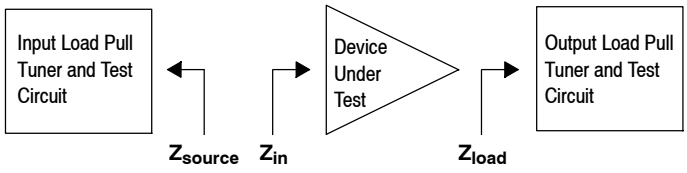
V_{DD} = 28 Vdc, I_{DQA} = 189 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2500	4.37 – j13.8	5.16 + j14.8	6.14 – j6.97	18.5	47.1	51	62.9	–20
2600	7.22 – j15.5	8.57 + j17.1	5.28 – j7.45	18.6	47.4	54	62.1	–18
2690	13.2 – j15.4	13.9 + j18.4	4.69 – j7.79	18.4	47.5	57	63.7	–17

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2500	4.37 – j13.8	5.04 + j15.8	5.63 – j7.56	16.2	48.1	65	62.6	–28
2600	7.22 – j15.5	9.18 + j18.8	4.99 – j7.91	16.3	48.3	67	61.9	–25
2690	13.2 – j15.4	16.3 + j20.4	4.60 – j8.25	16.2	48.4	69	63.5	–24

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 10. Single Side Load Pull Performance — Maximum Drain Efficiency Tuning



P1dB - TYPICAL LOAD PULL CONTOURS — 2600 MHz

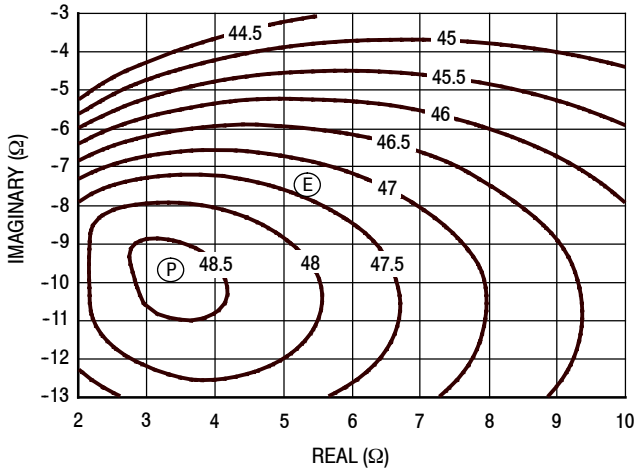


Figure 11. P1dB Load Pull Output Power Contours (dBm)

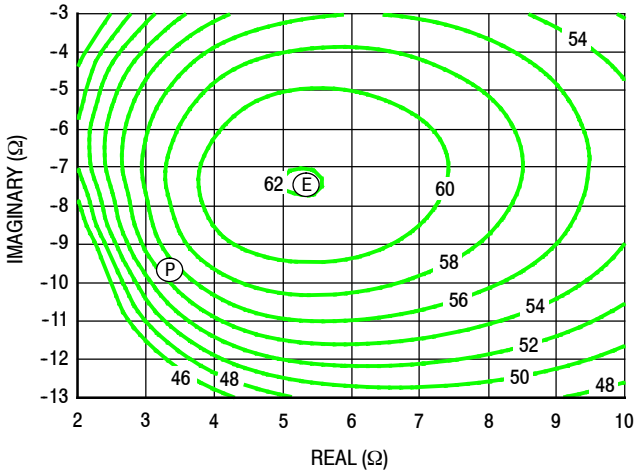


Figure 12. P1dB Load Pull Efficiency Contours (%)

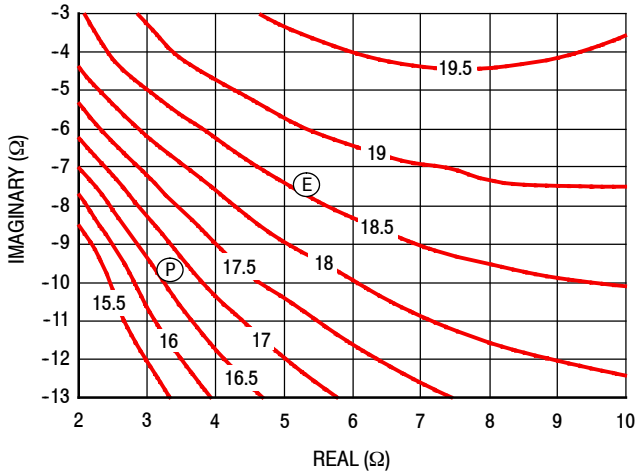


Figure 13. P1dB Load Pull Gain Contours (dB)

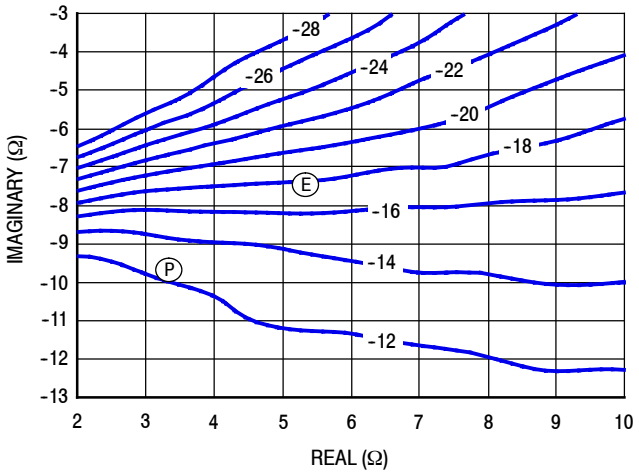


Figure 14. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 2600 MHz

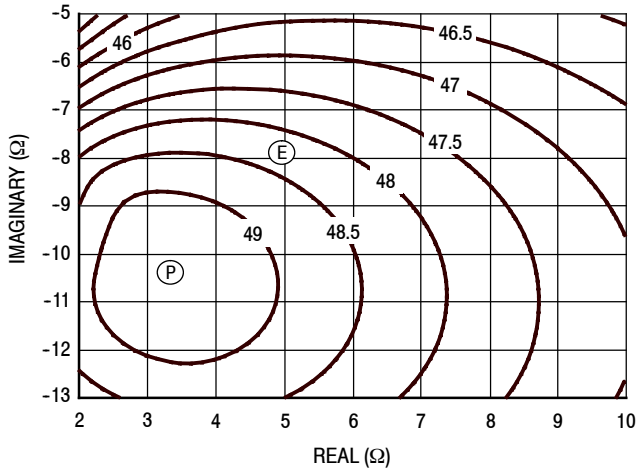


Figure 15. P3dB Load Pull Output Power Contours (dBm)

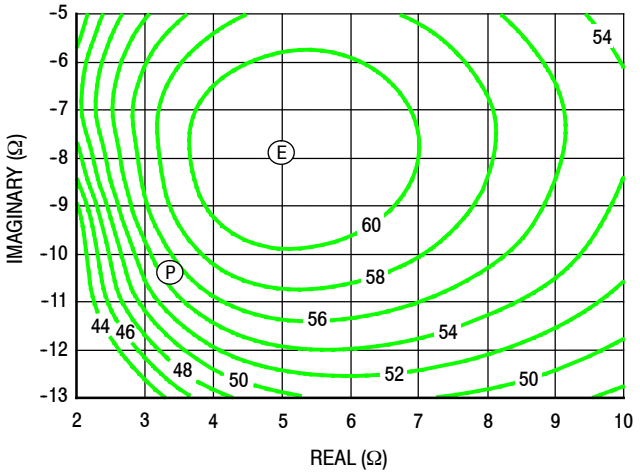


Figure 16. P3dB Load Pull Efficiency Contours (%)

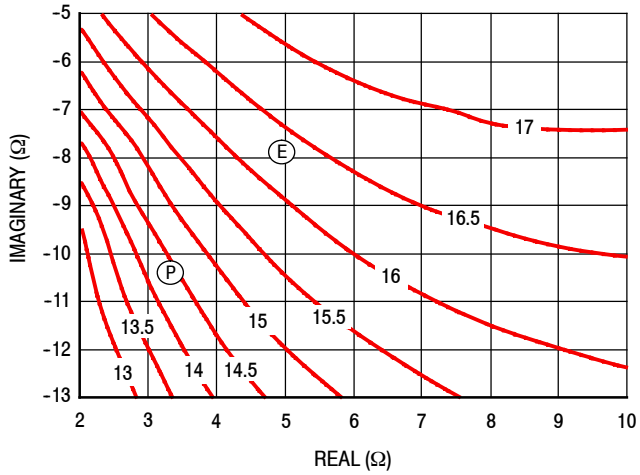


Figure 17. P3dB Load Pull Gain Contours (dB)

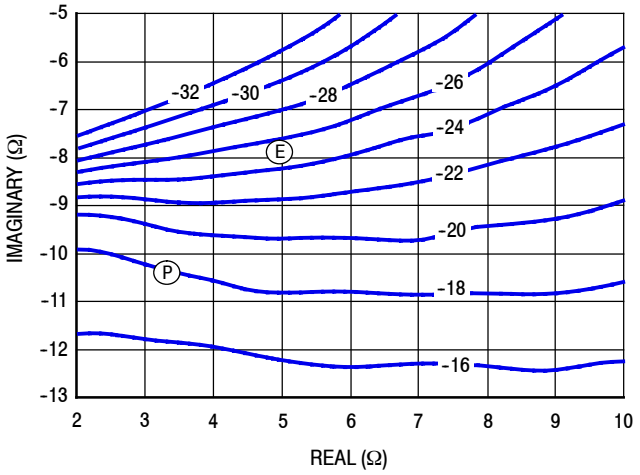


Figure 18. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

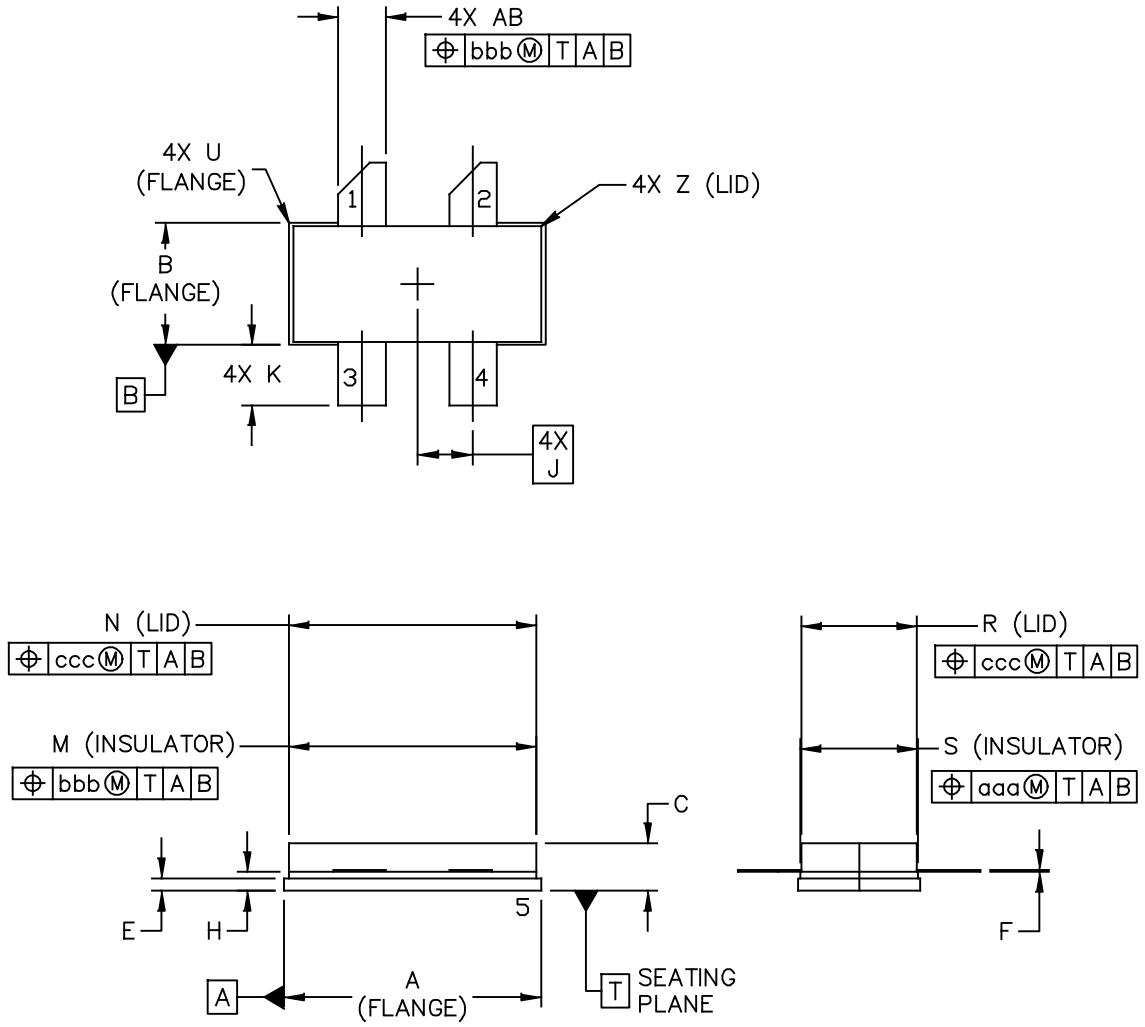
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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TITLE: NI 780S–4	DOCUMENT NO: 98ASA10718D	REV: A
	CASE NUMBER: 465H–02	27 MAR 2007
	STANDARD: NON–JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.805	.815	20.45	20.7	U		.040		1.02
B	.380	.390	9.65	9.91	Z		.030		0.76
C	.125	.170	3.18	4.32	AB	.145	.155	3.68	3.94
E	.035	.045	0.89	1.14					
F	.003	.006	0.08	0.15	aaa		.005		0.127
H	.057	.067	1.45	1.7	bbb		.010		0.254
J	.175 BSC		4.44 BSC		ccc		.015		0.381
K	.170	.210	4.32	5.33					
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.52					

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TITLE: NI 780S–4

DOCUMENT NO: 98ASA10718D | REV: A

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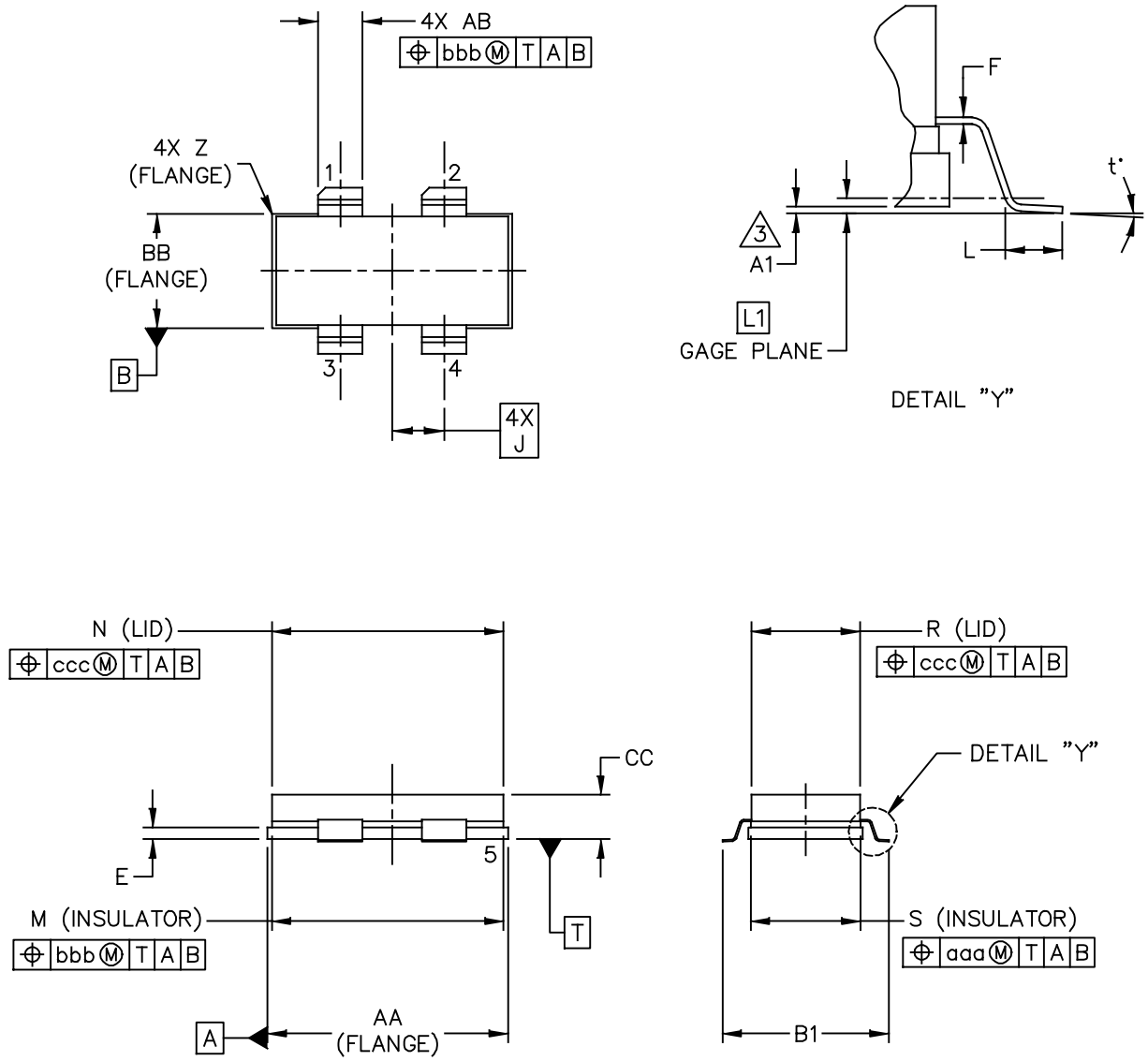
STANDARD: NON–JEDEC



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	STANDARD: NON-JEDEC	
	05 SEP 2013	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH.

3. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM T. THE POSITIVE VALUE IMPLIES THAT THE PACKAGE BOTTOM IS HIGHER THAN THE LEAD BOTTOM.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	Z	R.000	R.040	R0.00	R1.02
A1	.002	.008	0.05	0.20	AB	.145	.155	3.68	3.94
BB	.380	.390	9.65	9.91	t°	0°	8°	0°	8°
B1	.546	.562	13.87	14.27	aaa		.005		0.13
CC	.125	.170	3.18	4.32	bbb		.010		0.25
E	.035	.045	0.89	1.14	ccc		.015		0.38
F	.003	.006	0.08	0.15					
L	.038	.046	0.97	1.17					
L1	.010 BSC		0.25 BSC						
J	.175 BSC		4.44 BSC						
M	.774	.786	19.66	19.96					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.53					

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE:

NI–780GS–4L

DOCUMENT NO: 98ASA00238D REV: B

STANDARD: NON–JEDEC

05 SEP 2013

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to Software & Tools on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2013	• Initial Release of Data Sheet
1	Aug. 2013	• Fig. 3, AFT26P100–4WSR3 Characterization Test Circuit Component Layout, updated to include soldered down device in the layout drawing, p. 5 • Table 6, AFT26P100–4WSR3 Characterization Test Circuit Component Designations and Values, updated to include soldered down Freescale device, p. 5
2	Mar. 2015	• Added part number AFT26P100–4WGSR3, p. 1 • Added NI–780GS–4L package isometric, p. 1, and Mechanical Outline, pp. 13–14

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